S70GL-P MirrorBit™ Flash

S70GL02GP
2 Gigabit, 3.0 Volt-only Page Mode Flash Memory featuring 90 nm MirrorBit Process Technology

Data Sheet *(Advance Information)*

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S70GL-P MirrorBit™ Flash Family

S70GL02GP
2 Gigabit, 3.0 Volt-only Page Mode Flash Memory featuring 90 nm MirrorBit Process Technology

Data Sheet *(Advance Information)*

General Description

The Spansion S70GL02GP 2 Gigabit Mirrorbit™ Flash memory device is fabricated on 90 nm process technology. This device offers a fast page access time of 25 ns with a corresponding random access time of 120 ns. It features a Write Buffer that allows a maximum of 32 words/64 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes the device an ideal product for today's embedded applications that require higher density, better performance and lower power consumption.

Distinctive Characteristics

- **Two 1024 Megabit (S29GL01GP) in a single 64-ball Fortified-BGA package (see publication S29GL-P_00 for full specifications)**
- **Single 3V read/program/erase (2.7-3.6 V)**
- **Enhanced VersatileI/O™ control**
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- **90 nm MirrorBit process technology**
- **8-word/16-byte page read buffer**
- **32-word/64-byte write buffer reduces overall programming time for multiple-word updates**
- **Secured Silicon Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number
  - Can be programmed and locked at the factory or by the customer
- **Uniform 64Kword/128KByte Sector Architecture**
  - S70GL02GP: two thousand forty-eight sectors
- **100,000 erase cycles per sector typical**
- **20-year data retention typical**
- **Offered Packages**
  - 64-ball Fortified BGA
- **Suspend and Resume commands for Program and Erase operations**
- **Write operation status bits indicate program and erase operation completion**
- **Unlock Bypass Program command to reduce programming time**
- **Support for CFI (Common Flash Interface)**
- **Persistent and Password methods of Advanced Sector Protection**
- **WP#/ACC input**
  - Accelerates programming time (when V_{ACC} is applied) for greater throughput during system production
  - Protects first or last sector of each die, regardless of sector protection settings
- **Hardware reset input (RESET#) resets device**
- **Ready/Busy# output (RY/BY#) detects program or erase cycle completion**

Performance Characteristics

Max. Read Access Times (ns)*			
	2 Gb		
Parameter	**V1**	**V2**	**V3**
Random Access Time (t_{ACC})	110	120	130
Page Access Time (t_{PACC})	25	25	25
CE# Access Time (t_{CE})	110	120	130
OE# Access Time (t_{OE})	25	25	30

** Access times are dependent on V_{CC} and V_{IO} operating ranges. See Ordering Information page for further details.*
V1: V_{CC} = 3.0–3.6 V. V2: V_{CC} = V_{IO} = 2.7–3.6 V.
V3: V_{IO} = 1.65–V_{CC}, V_{CC} = 3 V.
*** Contact a sales representative for availability.*

Current Consumption (typical values)	
Random Access Read	30 mA
8-Word Page Read	1 mA
Program/Erase	50 mA
Standby	1 µA

Program & Erase Times (typical values)	
Single Word Programming	60 µs
Effective Write Buffer Programming (V_{CC}) Per Word	15 µs
Effective Write Buffer Programming (V_{ACC}) Per Word	15 µs
Sector Erase Time (64 Kword Sector)	0.5 s

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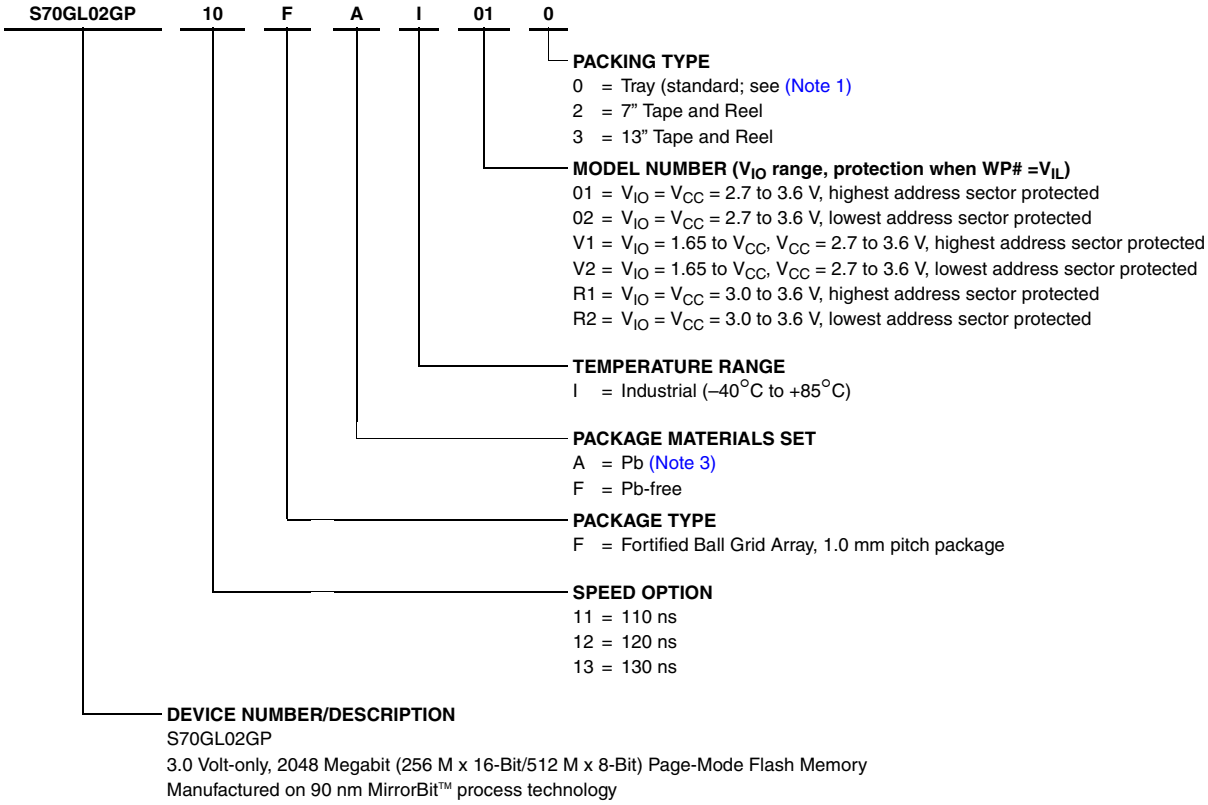
1. Ordering Information

The ordering part number is formed by a valid combination of the following:



S70GL02GP Valid Combinations					
Base Part Number	Speed (ns)	Package & Temperature	Model Number	Pack Type	Package Description
S70GL02GP	11	FAI , FFI (Note 3)	R1, R2	0, 2, 3 (Note 1)	LSE064 (Fortified BGA) (Note 2)
	12		01 (Note 3), 02		
	13		V1 (Note 3), V2		

Notes

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S70" and packing type designator from ordering part number.*
3. *Contact local sales representative for availability.*

1.1 Recommended Combinations

Recommended Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific recommended combinations and to check on newly released combinations.

2. Input/Output Descriptions & Logic Symbol

Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions

Symbol	Type	Description
A26–A0	Input	Address lines for GL02GP
DQ14–DQ0	I/O	Data input/output.
DQ15	I/O	DQ15: Data input/output in word mode . A-1: LSB address input in byte mode.
CE#	Input	Chip Enable.
OE#	Input	Output Enable.
WE#	Input	Write Enable.
V_{CC}	Supply	Device Power Supply.
V_{IO}	Supply	Versatile IO Input.
V_{SS}	Supply	Ground.
NC	No Connect	Not connected internally.
RY/BY#	Output	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively erasing or programming. At High Z, the device is in ready.
BYTE#	Input	Selects data bus width. At V_{IL}, the device is in byte configuration and data I/O pins DQ0-DQ7 are active. At V_{IH}, the device is in word configuration and data I/O pins DQ0-DQ15 are active.
RESET#	Input	Hardware Reset. Low = device resets and returns to reading array data.
WP#/ACC	Input	Write Protect/Acceleration Input. At V_{IL}, disables program and erase functions in the outermost sectors. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. Should be at V_{IH} for all other conditions.
RFU	Reserved	Reserved for future use.

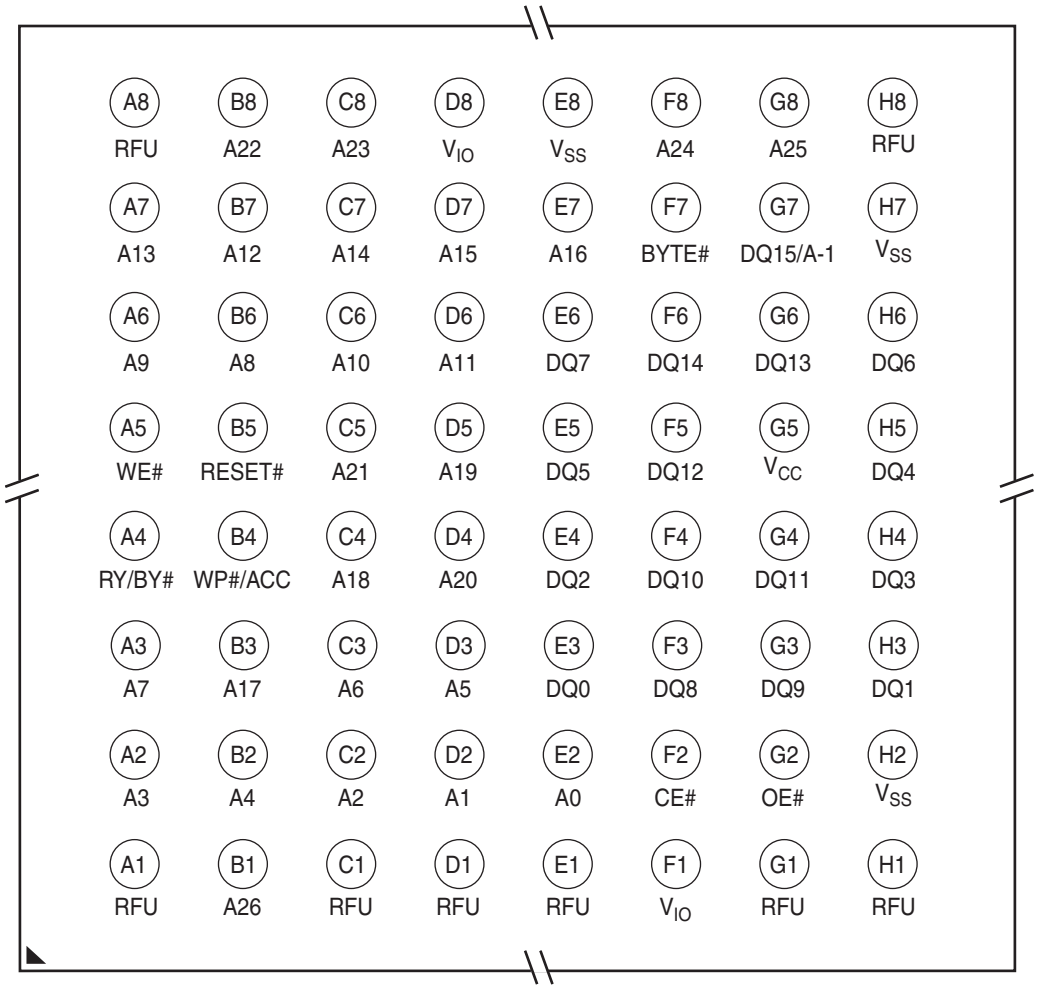
2.1 Special Handling Instructions for BGA Package

Special handling is required for Flash Memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning m ethods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

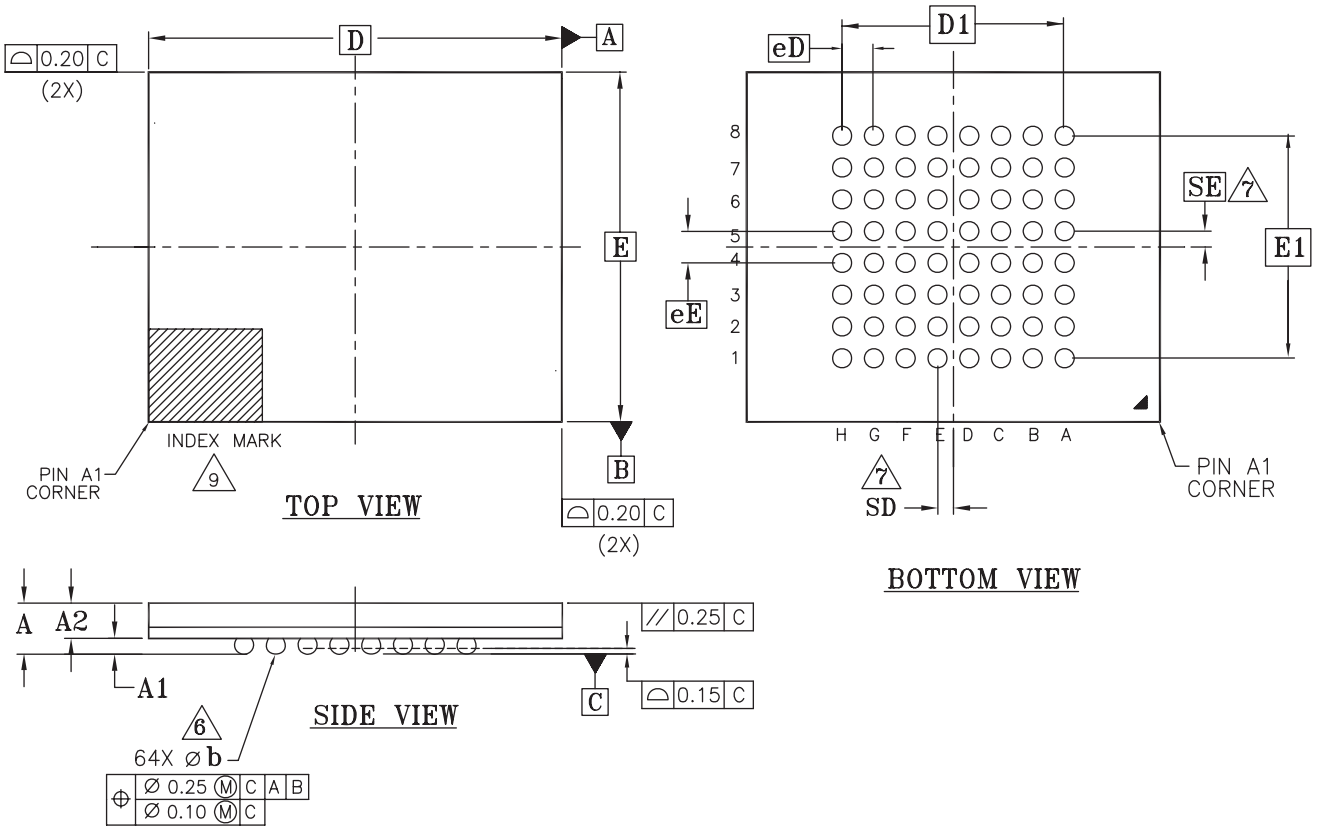
Figure 2.1 64-ball Fortified Ball Grid Array

64-ball Fortified BGA
Top View, Balls Facing Down



2.2 LSE064—64 ball Fortified Ball Grid Array, 13 x 11 mm

Figure 2.2 LSE064—64-ball Fortified Ball Grid Array (FBGA), 13 x 11 mm



PACKAGE	LSE 064			
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.40	---	---	BALL HEIGHT
A2	0.79	---	0.91	BODY THICKNESS
D		13.00 BSC.		BODY SIZE
E		11.00 BSC.		BODY SIZE
D1		7.00 BSC.		MATRIX FOOTPRINT
E1		7.00 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		64		BALL COUNT
Øb	0.50	0.60	0.70	BALL DIAMETER
eE		1.00 BSC.		BALL PITCH
eD		1.00 BSC		BALL PITCH
SD / SE		0.50 BSC.		SOLDER BALL PLACEMENT
		---		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3611 \ 16-038.15 \ 11.13.6

3. Memory Map

The S70GL02GP consist of uniform 64 Kword (128 Kb) sectors organized as shown in Table 3.1.

Table 3.1 S70GL02GP Sector & Memory Address Map

Uniform Sector Size	Sector Count	Sector Range	Address Range (16-bit)	Notes
64 Kword/128 Kb	2048	SA00	0000000h–000FFFFh	Sector Starting Address
		:	:	
		SA2047	7FF0000H–7FFFFFFh	Sector Ending Address

Note

This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001-SA1022) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 Kb sectors have the pattern xxx0000h-xxxFFFFh.

4. Autoselect

Table 4.1 provides the device identification codes for the S70GL02GP. For more information on the autoselect function, refer to the S29GL-P data sheet (pulication number S29GL-P_00).

Table 4.1 Autoselect Addresses in System

Description	Address	Read Data (word/byte mode)
Manufacturer ID	(Base) + 00h	xx01h/1h
Device ID, Word 1	(Base) + 01h	227Eh/7Eh
Device ID, Word 2	(Base) + 0Eh	2248h/48h
Device ID, Word 3	(Base) + 0Fh	2201h/01h
Secure Device Verify	(Base) + 03h	For S70GL02GPH: XX19h/19h = Not Factory Locked. XX99h/99h = Factory Locked. For S70GL02GPL: XX09h/09h = Not Factory Locked. XX89h/89h = Factory Locked.
Sector Protect Verify	(SA) + 02h	xx01h/01h = Locked, xx00h/00h = Unlocked

5. Erase And Programming Performance

Table 5.1 Erase And Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 5)
Chip Erase Time	S70GL02GP	1024	4096	sec	
Total Write Buffer Time (Note 3)		480		µs	Excludes system level overhead (Note 6)
Total Accelerated Write Buffer Programming Time (Note 3)		432		µs	
Chip Program Time (Note 4)	S70GL02GP	1968		sec	

Notes

1. *Typical program and erase times assume the following conditions: 25°C, 3.6 V V_{CC}, 10,000 cycles, checkerboard pattern.*
2. *Under worst case conditions of -40°C, V_{CC} = 3.0 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 32-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command.*

6. BGA Package Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	20	24	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	16	20	pF
RESET#, WP#/ACC	Separated Control Pin	$V_{IN} = 0$	84	90	pF
CE#	Separated Control Pin	$V_{IN} = 0$	44	50	pF

Notes

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

7. Common Flash Memory Interface

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI infomation at the addresses given in Tables 7.2–7.4). All reads outside of the CFI address range, returns non-valid data. Reads from other sectors are allowed, writes are not. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 7.2–7.4. The system must write the reset command to return the device to reading array data.

The following is a C source code example of using the CFI Entry and Exit functions. Refer to the *Spansion Low Level Driver User's Guide* (available on www.spansion.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: CFI Entry command */
  *( (UINT16 *)base_addr + 0x55 ) = 0x0098;   /* write CFI entry command         */

/* Example: CFI Exit command  */
  *( (UINT16 *)base_addr + 0x000 ) = 0x00F0;   /* write cfi exit command          */
```

For further information, please refer to the CFI Specification (see JEDEC publications JEP137-A and JESD68.01and CFI Publication 100). Please contact your sales office for copies of these documents.

Table 7.1 CFI Query Identification String

Addresses (x16)	Addresses (x8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7.2 System Interface String

Addresses (x16)	Addresses (x8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 mV
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 mV
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0006h	Typical timeout per single byte/word write 2^N µs
20h	40h	0006h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	0013h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0003h	Max. timeout for byte/word write 2^N times typical
24h	48h	0005h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0003h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0002h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 7.3 Device Geometry Definition

Addresses (x16)	Addresses (x8)	Data	Description
27h	4Eh	001Bh	Device Size = 2^N byte 1Bh = 1 Gb
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0006h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0001h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00xxh 000xh 0000h 000xh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) 00FFh, 0003h, 0000h, 0002h =1 Gb 00FFh, 0001h, 0000h, 0002h = 512 Mb 00FFh, 0000h, 0000h, 0002h = 256 Mb 007Fh, 0000h, 0000h, 0002h = 128 Mb
31h 32h 33h 34h	60h 64h 66h 68h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 7.4 Primary Vendor-Specific Extended Query

Addresses (x16)	Addresses (x8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0014h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0101b = 90 nm MirrorBit
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0008h	Sector Protect/Unprotect scheme 0008h = Advanced Sector Protection
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	00xxh	WP# Protection 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

8. Revision Summary

Section	Description
Revision A0 (December 4, 2006)	
	Initial Release.

Colophon

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