

HM6788 Series

Maintenance Only

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

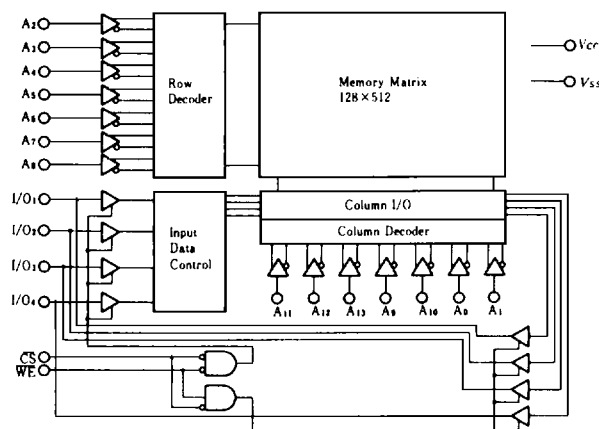
FEATURES

- Super Fast Access Time : 25/30ns (max.)
- Low power Operation
Operating: 230mW (typ), Standby: 10mW (typ)
- +5V Single Supply
- Completely Static Memory –
No Clock or Timing Strobe required
- Balanced Read and Write Cycle Time
- Fully TTL compatible Input and Output

ORDERING INFORMATION

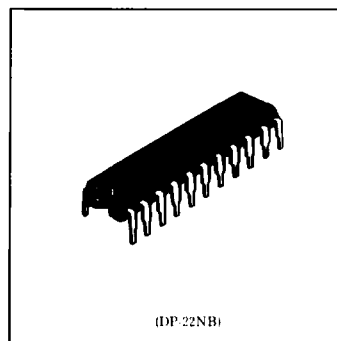
Type No.	Access Time	Package
HM6788P-25	25ns	300 mil 22 pin Plastic DIP
HM6788P-30	30ns	

BLOCK DIAGRAM

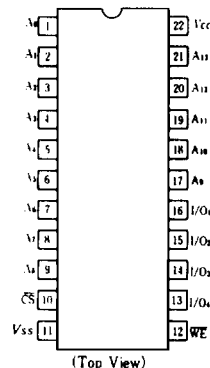


ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	$T_{stg}(bias)$	-10 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C



PIN ARRANGEMENT



HITACHI

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■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.5^{*1}	—	0.8	V

(Note) *1. -3.0V with 20ns pulse width.■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = 5.5\text{V}$, $V_{IH} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_I/D = 0\text{mA}$	—	—	80	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $V_{IS} \leq 0.2\text{V}$ or $V_{IS} \geq V_{CC} - 0.2\text{V}$	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8\text{mA}$	—	—	0.5	V
Output High Voltage	V_{OH}	$I_{OH} = -4\text{mA}$	2.4	—	—	V

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0$ to $+70^{\circ}\text{C}$, unless otherwise noted)

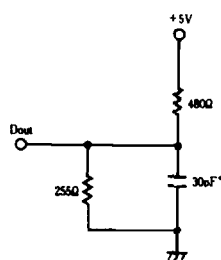
● AC Test Conditions

Input pulse levels: V_{SS} to 3.0V

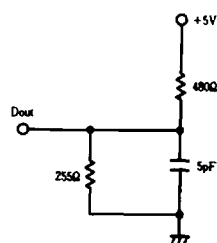
Input rise and fall time: 4ns

Input and Output reference levels: 1.5V

Output Load: See Figure



Output Load A



* Including scope and jig.

Output Load B
(1CHZ, 1WHZ, 1CLZ, 1OW)

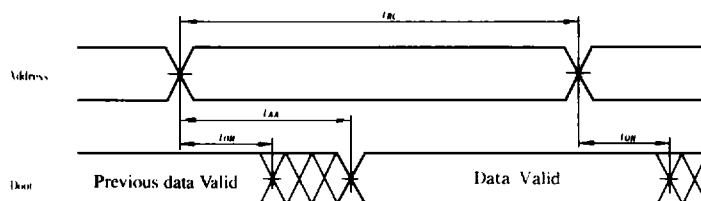
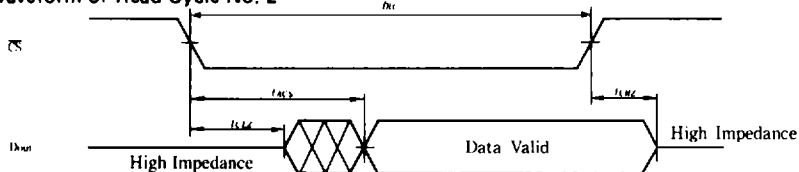
● READ CYCLE

Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Address Access Time	t_{AA}	—	25	—	30	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	ns
Chip Selection to Output in Low Z	t_{CLZ}^{*2}	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ}^{*2}	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time ^{*1}	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time ^{*1}	t_{PD}	—	20	—	30	ns
Input Voltage Rise/Fall Time ^{*3}	t_r	—	150	—	150	ns

Notes) *1. This parameter is sampled and not 100% tested.

*2. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

*3. If t_r becomes more than 150ns, there is possibility of function fail.
please contact your nearest Hitachi Sales Dept. regarding specification.

● Timing waveform of Read Cycle No. 1^{*1,*2}● Timing waveform of Read Cycle No. 2^{*1,*3}

Note) *1. $\overline{WE} = V_{IH}$

*2. $\overline{CS} = V_{IL}$

*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

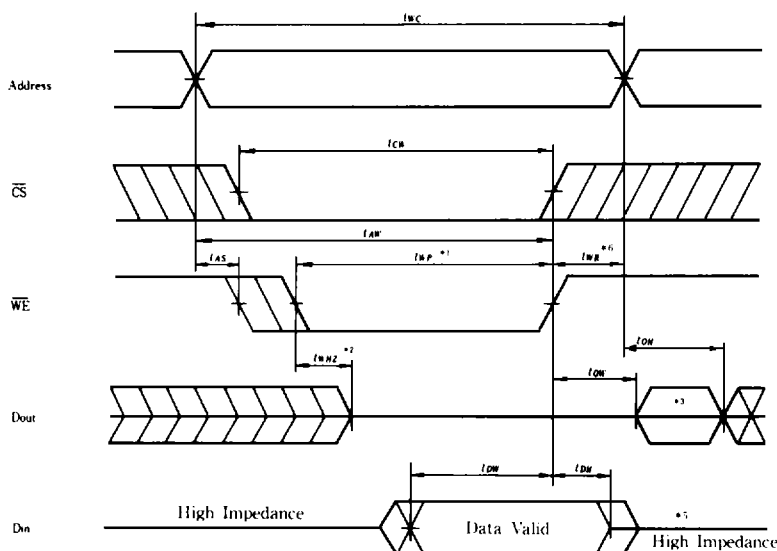
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	20	—	25	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	20	—	25	—	ns
Write Pulse Width	t_{WP}	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High Z	t_{WHZ}^{*1}	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	—	15	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Output Active from End of Write	t_{OW}^{*1}	0	—	0	—	ns

*1. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B).

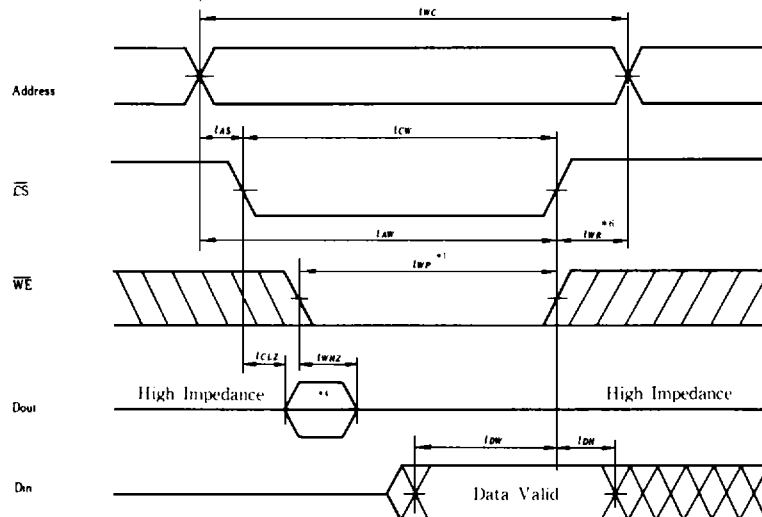
This parameter is sampled and not 100% tested.



● Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



● Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



- Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
 *2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 *3. D_{out} is the same phase of write data of this write cycle.
 *4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
 *5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 *6. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IS}	—	—	6.0	$V_{IS} = 0\text{V}$
Input-Output Capacitance	$C_{I/O}$	—	—	8.0	$V_{OI} = 0\text{V}$

Note) This parameter is sampled and not 100% tested

