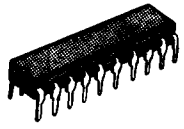
HM6168H-45, HM6168H-55, HM6168H-70, HM6168HP-45, HM6168HP-55, HM6168HP-70

4096-word×4-bit High Speed Static CMOS RAM

■FEATURES

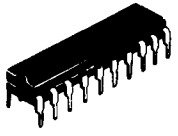
- High Speed: Fast Access Time 45/55/70 ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
  100μW typ. (Standby), 200mW typ. (Operation)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs

HM6168H-45/55/70



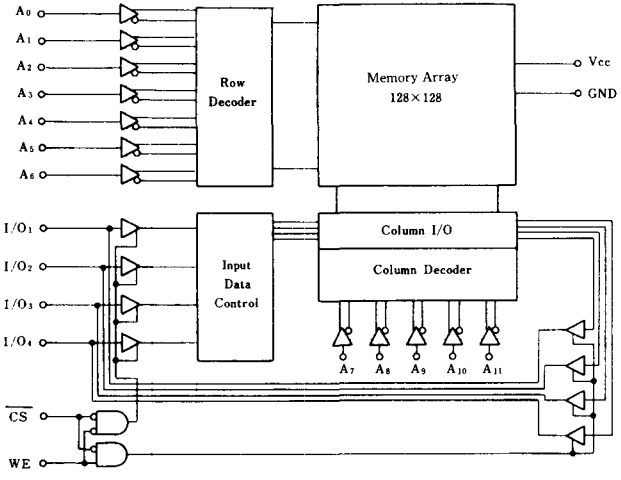
(DG-20)

HM6168HP-45/55/70



(DP-20)

■FUNCTIONAL BLOCK DIAGRAM

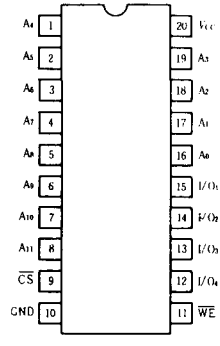


■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC = −0.5V

■PIN ARRANGEMENT



(Top View)

HITACHI

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to + 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*	–	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to + 70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Imput Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	40	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	–	0.02	2.0	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	–	–	V

Note: Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

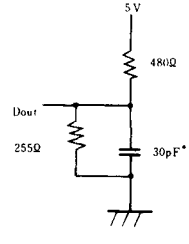
■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

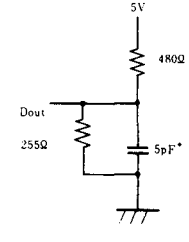
■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to + 70°C, unless otherwise noted.)

• AC TEST CONDITION

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figure



Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

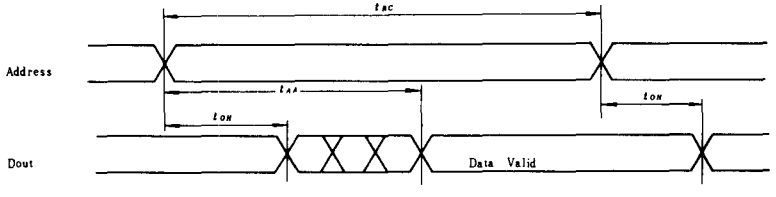
* Including scope and jig.

• READ CYCLE

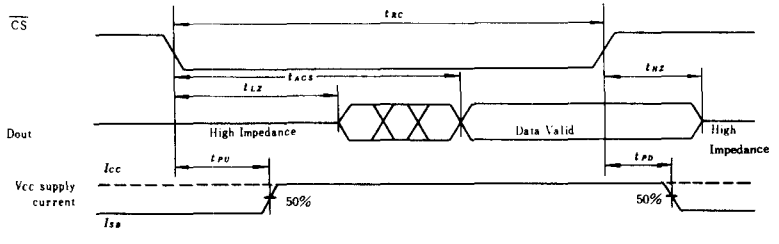
Item	Symbol	HM6168H/P-45		HM6168H/P-55		HM6168H/P-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns
Address Access Time	t_{AA}	–	45	–	55	–	70	ns
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns
Chip Selection to Output in Low Z*	t_{LZ}	20	–	20	–	20	–	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	–	30	ns

* Transition is measured ±500mV for high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1[(1), (2)]



• TIMING WAVEFORM OF READ CYCLE NO. 2[(1), (3)]



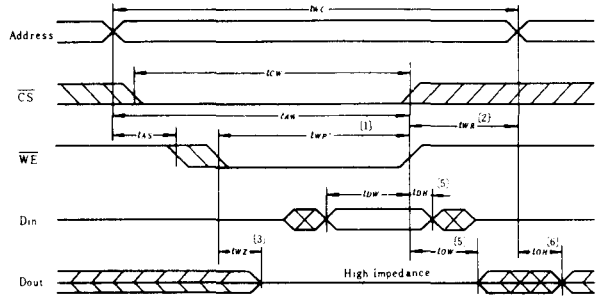
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE

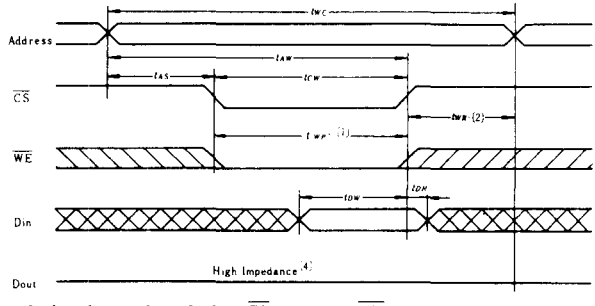
Item	Symbol	HM6168H/P-45		HM6168H/P-55		HM6168H/P-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns
Chip Selection to End of Write	t_{CW}	40	–	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	40	–	50	–	60	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	35	–	45	–	55	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	25	–	30	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*	t_{OW}	0	–	0	–	0	–	ns

* Thansition is measured ±500mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$, (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of Write data of this write cycle.