National Semiconductor

Magnetic Memory Interface Circuits

DS75324 Memory Driver with Decode Inputs

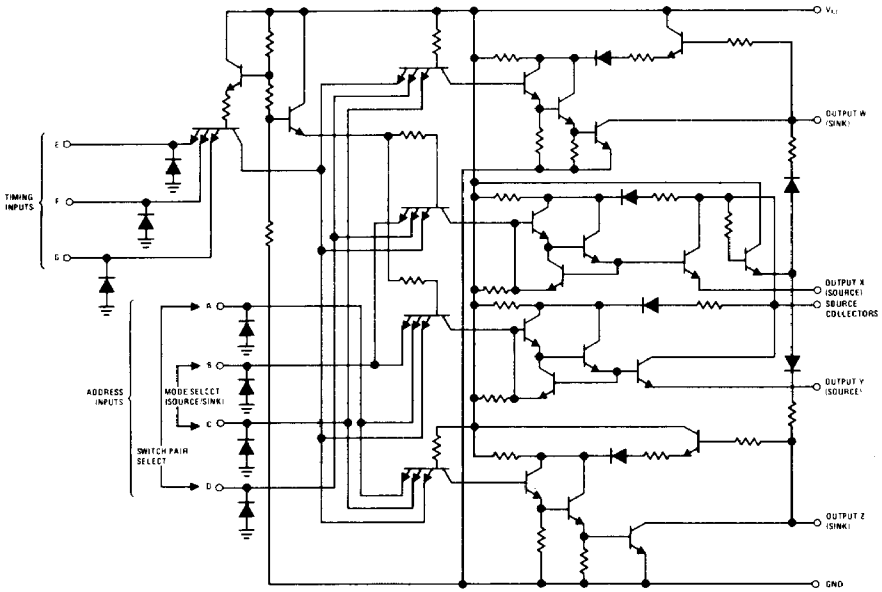
General Description

The DS75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X).

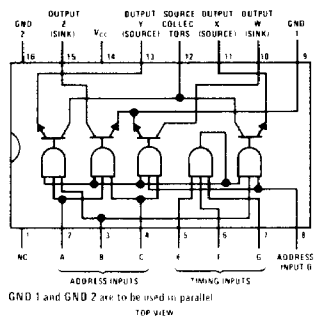
Features

- High voltage outputs
- Dual sink-source outputs
- Internal decoding and timing circuitry
- 400 mA output capability
- DTL/TTL compatible
- Input clamping diodes

Schematic and Connection Diagrams

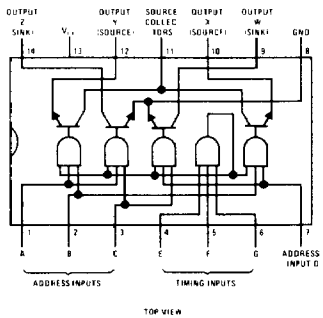


Dual-In-Line Package



Order Number DS75324J
See NS Package J16A

Dual-In-Line Package



Order Number DS75324N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC} (Note 4)	17V
Input Voltage (Note 5)	5.5V
Operating Case Temperature Range	0°C to +70°C
Power Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (V_{CC} = 14V, T_C = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Input Voltage Required to Insure Logical "1" At Any Input	*(Figure 1)*		3.5			V
$V_{IN(0)}$	Input Voltage Required to Insure Logical "0" At Any Input	*(Figure 1)*				0.8	V
$I_{IN(1)}$	Logical "1" Level Input Current	V_{IN} = 5V,	Address Input			200	μA
		(Figure 1)	Timing Input			100	μA
$I_{IN(0)}$	Logical "0" Level Input Current	V_{IN} = 0V,	Address Input			−6	mA
		(Figure 1)	Timing Input			−12	mA
V_{SAT}	Saturation Voltage	*(Figure 2)*	Sink, $I_{SINK} \simeq$ 420 mA, R_L = 53Ω		0.75	0.85	V
			Source, $I_{SOURCE} \simeq$ −420 mA, R_L = 47.5Ω		0.75	0.85	V
I_{OFF}	Output Reverse Current ("OFF" State)	V_{IN} = 0V, *(Figure 1)*			125	200	μA
I_{CC}	Supply Current	All Sources and Sinks OFF, V_{IN} = 0V, *(Figure 3)*			12.5	15	mA
		(Figure 4)	Either Sink Selected		30	40	mA
			Either Source Selected		25	35	mA
V_I	Input Clamp Voltage	I_{IN} = −12 mA, T_A = 25°C				−1.5	V

Switching Characteristics (V_{CC} = 14V, T_C = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay Time to Logical "1" Level	C_L = 20 pF	Sink Output, R_L = 53Ω, *(Figure 6)*			110	ns
			Source Output, R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*			90	ns
t_{pd0}	Propagation Delay Time to Logical "0" Level	C_L = 20 pF	Sink Output, R_L = 53Ω, *(Figure 6)*			40	ns
			Source Output, R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*			50	ns
t_s	Sink Storage Time					70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75324.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

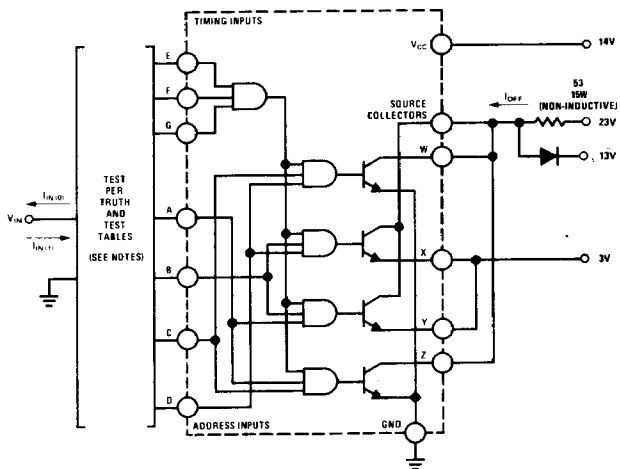
Note 4: Voltage values are with respect to network ground terminal.

Note 5: Input signals must be zero or positive with respect to network ground terminal.

Truth Table

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

Test Circuits and Switching Time Waveforms



Note 1: Check $V_{IN(1)}$ AND $V_{IN(0)}$ PER TRUTH TABLE.

Note 2: Measure $I_{IN(0)}$ per test table.

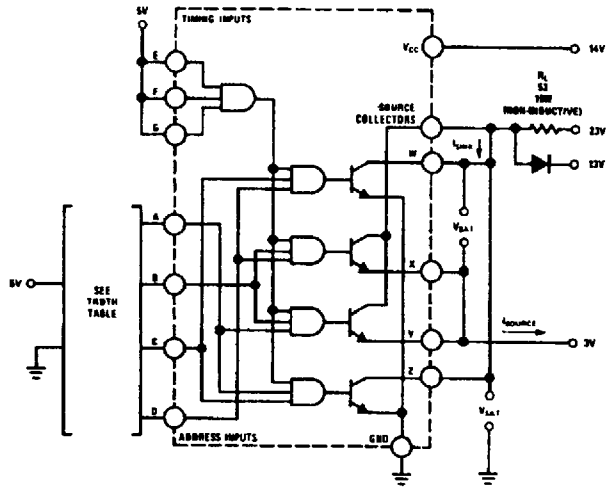
Note 3: When measuring $I_{IN(1)}$, all other inputs are at GND. Each input is tested separately.

TEST TABLE FOR $I_{IN(0)}$

APPLY 3.5V	GROUND	TEST $I_{IN(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

FIGURE 1. $V_{IN(0)}$, $V_{IN(1)}$, $I_{IN(0)}$, $I_{IN(1)}$, and I_{OFF}

Test Circuits and Switching Time Waveforms (Continued)



Note: This parameter must be measured using pulse techniques t_p = 500 ns, duty cycle ≤ 1%.

FIGURE 2. $V_{(SAT)}$

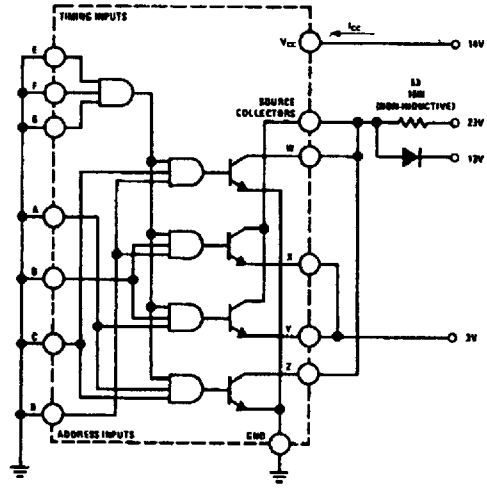


FIGURE 3. I_{CC} (All Outputs "OFF")

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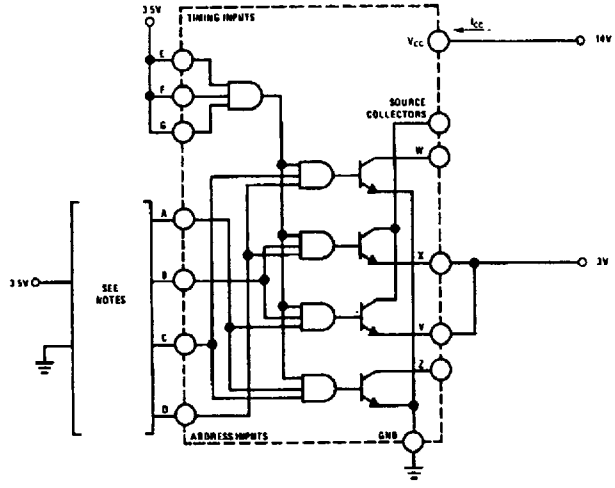
Test Circuits and Switching Time Waveforms (Continued)



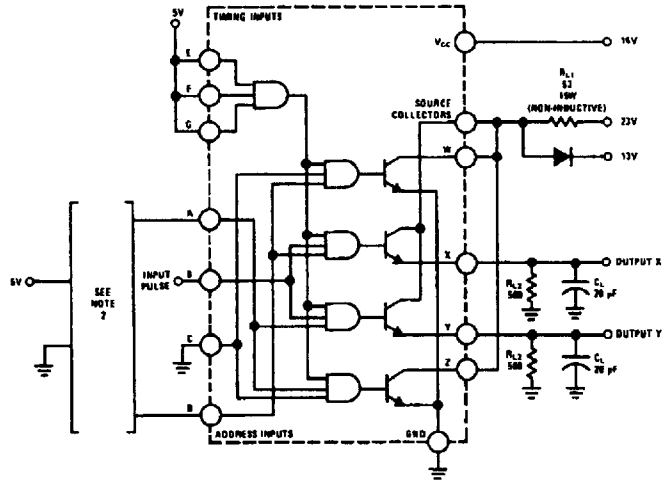
Note 1 GND A and B, apply +3.5V to C and D, and measure I_{CC} (output W is on)

Note 2. GND B and D, apply +3.5V to A and C and measure I_{CC} (output Z is on)

Note 3 GND A and C, apply +3.5V to B and D, and measure I_{CC} (output X is on)

Note 4 GND C and D, apply +3.5V to A and B, and measure I_{CC} (output Y is on)

FIGURE 4. I_{CC} (One Output "ON")



Note 1 The input waveform is supplied by a generator with the following characteristics $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{OUT} = 50\Omega$

Note 2. When measuring delay times at output X, apply +5V to input D, and GND A. When measuring delay times at output Y, apply +5V to input A, and GND D

Note 3 C_L includes probe and jig capacitance

Note 4 Unless otherwise noted all resistors are 0.5W.

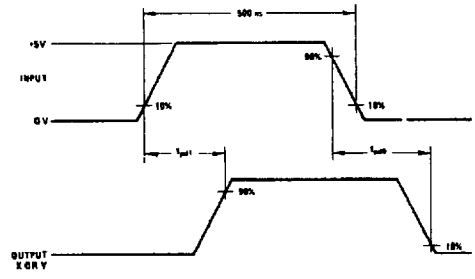
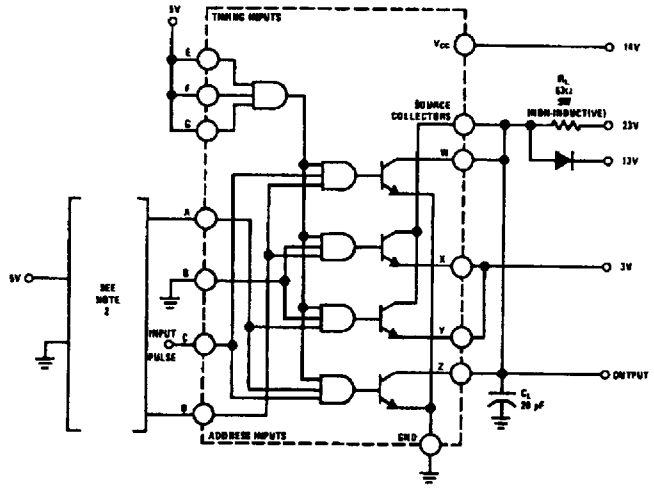


FIGURE 5. Source-Output Switching Times

Test Circuits and Switching Time Waveforms (Continued)



Note 1: The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.

Note 2: When measuring delay times at output W, apply +5V to input D, and GND A. When measuring delay times at output Z, apply +5V to input A, and GND D.

Note 3: C_L includes probe and jig capacitance.

FIGURE 6. Sink-Output Switching Times