

## CAT59C11/CAT59C11I

1K-Bit SERIAL E<sup>2</sup>PROM

### FEATURES

- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 64 x 16 or 128 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- RDY/BUSY Pin for End-of-Write Detection
- Hardware and Software Write Protection
- Power-Up Inadvertent Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

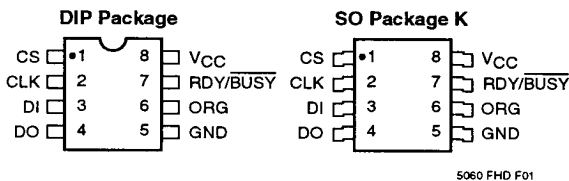
### DESCRIPTION

The CAT59C11 and CAT59C11I are 1K bit Serial E<sup>2</sup>PROM memory devices which can be configured as either 64 registers by 16 bits (ORG pin at V<sub>CC</sub>) or 128 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

The CAT59C11/CAT59C11I is manufactured using Catalyst's advanced CMOS E<sup>2</sup>PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

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### PIN CONFIGURATION

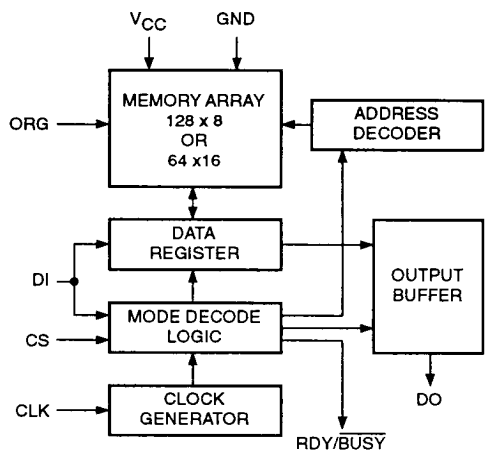


### PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
VCC	+5V Power Supply
GND	Ground
RDY/BUSY	Ready/Busy Status
ORG	Memory Organization

Note: When the ORG pin is connected to V<sub>CC</sub>, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	–55°C to +125°C
Storage Temperature .....	–65°C to +150°C
Voltage on Any Pin with Respect to Ground <sup>(1)</sup> .....	–2.0V to +V <sub>CC</sub> +2.0V
V <sub>CC</sub> with Respect to Ground .....	–2.0V to +7.0V
Package Power Dissipation Capability (T <sub>a</sub> = 25°C) .....	1.0W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(2)</sup> .....	100 mA

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N <sub>END</sub> <sup>(3)</sup>	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(3)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

**D.C. OPERATING CHARACTERISTICS**

CAT59C11 T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5V ±10%, unless otherwise specified.

CAT59C111 T<sub>A</sub> = –40°C to +85°C, V<sub>CC</sub> = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I <sub>CC1</sub>	Power Supply Current (Operating)			5	mA	DI = 0V, CLK = 5.0V V <sub>CC</sub> = 5.0V, CS = 5.0V Output Open
I <sub>CC2</sub>	Power Supply Current (Standby)			100	μA	DI = 0V, CLK = 0V V <sub>CC</sub> = 5.0V, CS = 0V
I <sub>LI</sub>	Input Leakage Current			2	μA	V <sub>IN</sub> = 5.5V
I <sub>LO</sub>	Output Leakage Current (Including ORG Pin)			10	μA	V <sub>OUT</sub> = 0V to 5.5V, CS = 0
V <sub>IH</sub>	High Level Input Voltage	2.0		V <sub>CC</sub> +1	V	
V <sub>IL</sub>	Low Level Input Voltage	–0.1		0.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.4			V	I <sub>OH</sub> = –400μA
V <sub>OL</sub>	Low Level Output Voltage			0.4	V	I <sub>OL</sub> = 2.1 mA

**Note:**

- (1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5V, which may overshoot to V<sub>CC</sub> +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V<sub>CC</sub> +1V.

## INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A6–A0	A5–A0			Read Address A <sub>N</sub> –A <sub>0</sub>
WRITE	1	X100	A6–A0	A5–A0	D7–D0	D15–D0	Write Address A <sub>N</sub> –A <sub>0</sub>
EWEN	1	0011	XXXXXXX	XXXXXX			Write Enable
EWDS	1	0000	XXXXXXX	XXXXXX			Write Disable
ERAL	1	0010	XXXXXXX	XXXXXX			Clear All Addresses
WRAL	1	0001	XXXXXXX	XXXXXX	D7–D0	D15–D0	Write All Addresses

## A.C. CHARACTERISTICS

CAT59C11 T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5V ±10%, unless otherwise specified.

CAT59C11I T<sub>A</sub> = –40°C to +85°C, V<sub>CC</sub> = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t <sub>CSS</sub>	CS Setup Time	50			ns	
t <sub>CSH</sub>	CS Hold Time	0			ns	
t <sub>DIS</sub>	DI Setup Time	100			ns	C <sub>L</sub> = 100pF V <sub>OL</sub> = 0.8V, V <sub>OH</sub> = 2.0V V <sub>IL</sub> = 0.45V, V <sub>IH</sub> = 2.4V
t <sub>DIH</sub>	DI Hold Time	100			ns	
t <sub>PD1</sub>	Output Delay to 1			500	ns	
t <sub>PD0</sub>	Output Delay to 0			500	ns	
t <sub>HZ</sub> <sup>(3)</sup>	Output Delay to High-Z			100	ns	C <sub>L</sub> = 100pF
t <sub>EW</sub>	Program/Erase Pulse Width			10	ms	
t <sub>CKH</sub>	Minimum Clock High Time	100			ns	
t <sub>CKL</sub>	Minimum Clock Low Time	660			ns	
t <sub>SV</sub>	RDY/BUSY Delay to Status Valid			500	ns	C <sub>L</sub> = 100pF
f <sub>CLK</sub>	Maximum Clock Frequency	DC		1	MHz	

Note:

(3) This parameter is tested initially and after a design or process change that affects the parameter.

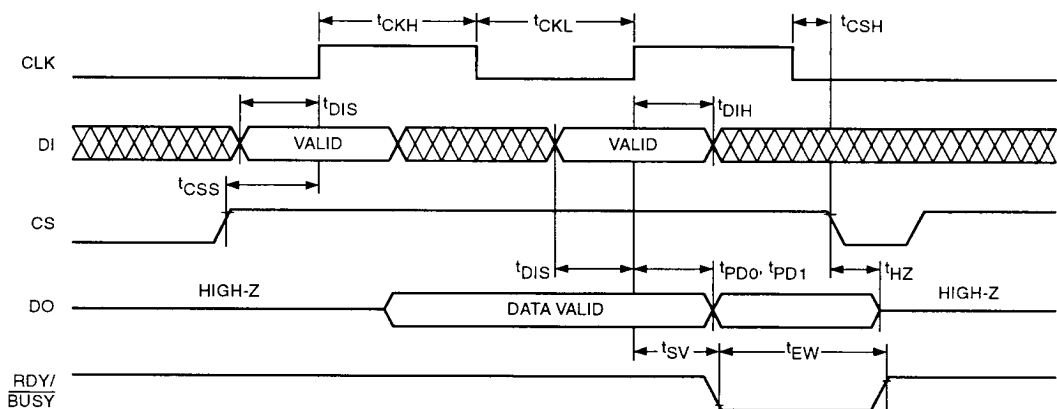
## DEVICE OPERATION

The CAT59C11/CAT59C11I is a 1024 bit nonvolatile memory intended for use with industry standard micro-processors. The CAT59C11/CAT59C11I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six 11 bit instructions (12 bit instruction in 128x8 organization) control the reading, writing and erase operations of the device. The CAT59C11/CAT59C11I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally in a high impedance state except when reading data from the device. The ready/busy status can

be determined after a write operation by polling the RDY/BUSY pin; a low level on this pin indicates that the write operation is not completed, while a high level indicates that the WRITE, ERASE or WRAL operation has been completed and the device is ready for the next instruction.

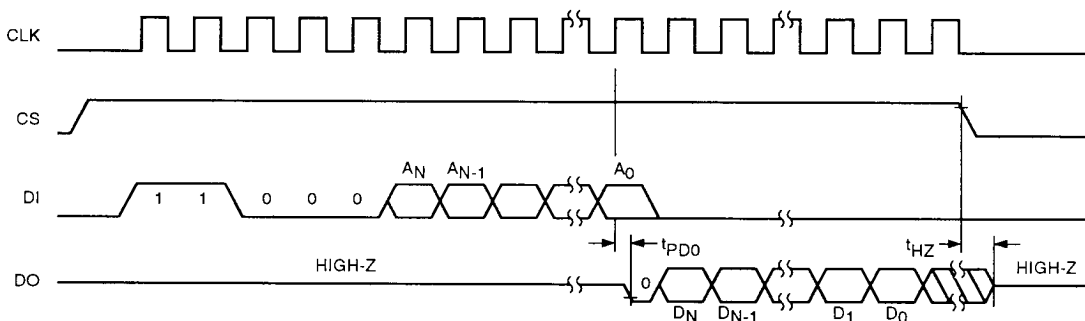
The format for all instructions sent to the CAT59C11/CAT59C11I is a logical "1" start bit, a 4 bit opcode, a 6 bit address (7 bit address when organized as 128x8), and for write operations a 16 bit data field (8 bit data field when organized as 128x8). At power-down, when  $V_{CC}$  falls below a threshold of approximately 3.5V, the data protection circuitry inhibits all erase and write instructions and a write disable (EWDS) is executed internally.

**Figure 1. Synchronous Data Timing<sup>(5)</sup>**



5060 FHD F03

**Figure 2. Read Instruction Timing<sup>(5)</sup>**



5060 FHD F04

Note:

(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected,  $A_N = A6$  and  $D_N = D7$ . When x16 organization is selected,  $A_N = A5$  and  $D_N = D15$ .

**NOTE:** This device will accept a start bit that is generated when both CLK and DI are high with respect to a low to high transition of CS.

### Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT59C11/CAT59C11I will come out of the high impedance state and, after sending an initial dummy zero bit (after a delay of  $t_{PD0}$  from the positive edge of the  $A_0$  clock), will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ). DO returns to High-Z after a delay of  $t_{HZ}$  from the negative going edge of CS.

### Erase/Write Enable and Disable

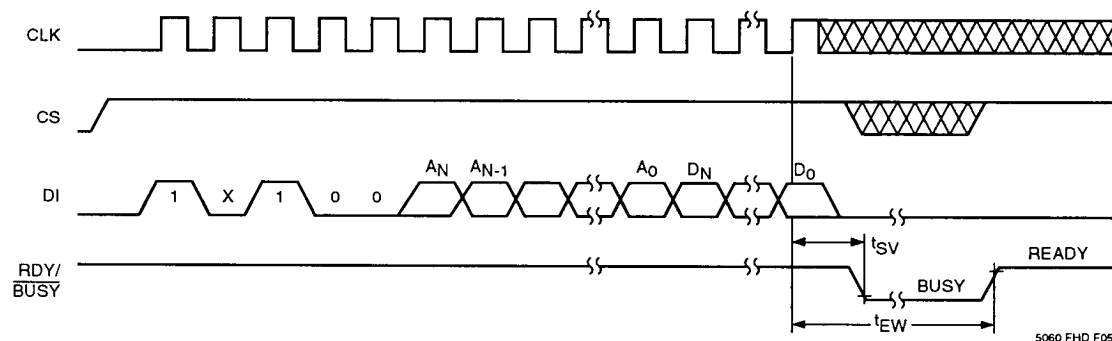
The CAT59C11/CAT59C11I powers up in the write disabled state. Any write after power-up or after a EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruc-

tion is enabled, it will remain enabled until power to the device is removed, or the EWEN instruction is sent. The EWEN instruction can be used to disable all CAT59C11/CAT59C11I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

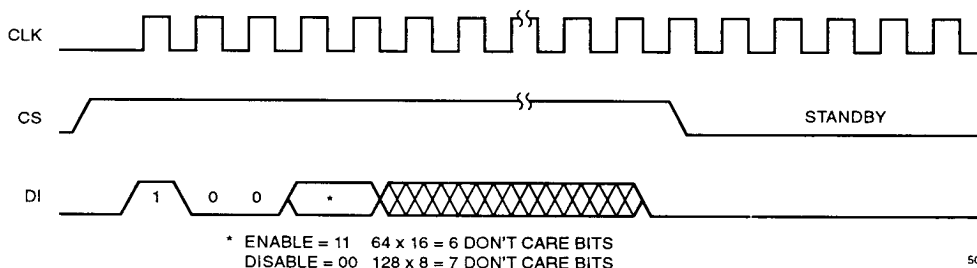
### Write

After receiving a WRITE command, address and data, the RDY/BUSY pin goes low (after a delay of  $t_{SV}$  from the positive edge of the  $D_0$  clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width ( $t_{EW}$ ) is timed from the positive clock edge of the last data bit ( $D_0$ ) and its completion is indicated by the RDY/BUSY pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

**Figure 3. Write Instruction Timing<sup>(5)</sup>**



**Figure 4. EWEN/EWDS Instruction Timing<sup>(5)</sup>**



Note:

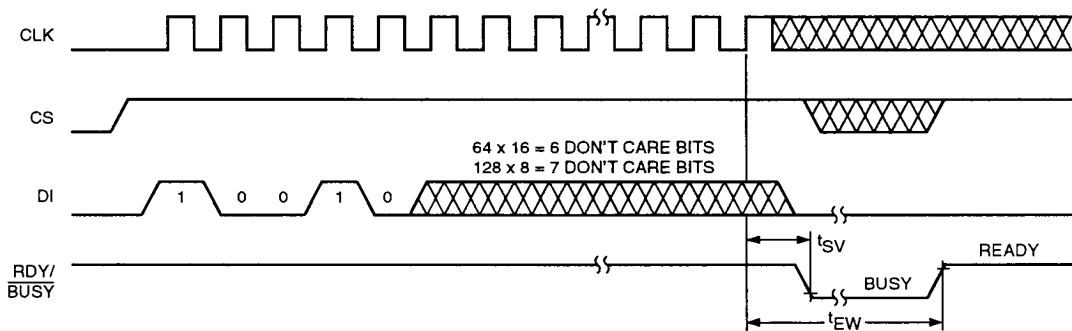
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected,  $AN = A6$  and  $DN = D7$ . When x16 organization is selected,  $AN = A5$  and  $DN = D15$ .

**Erase All**

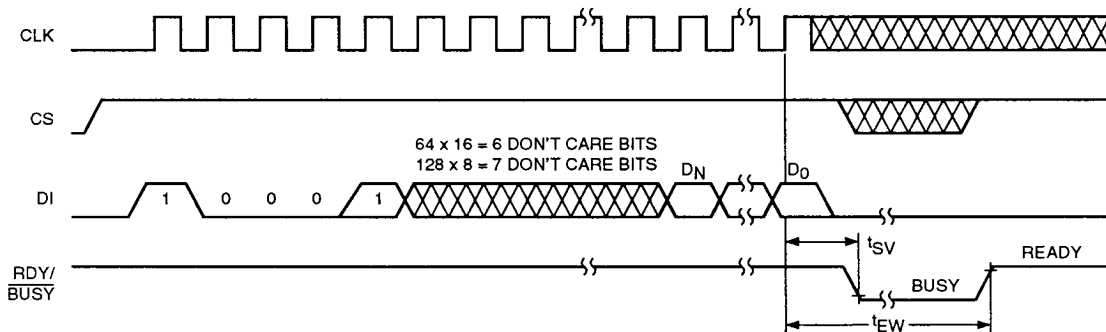
After receiving an ERAL command and address the RDY/BUSY pin goes low (after a delay of  $t_{SV}$  from the positive edge of the  $D_0$  clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width ( $t_{EW}$ ) is timed from the positive clock edge of the last don't care bit and its completion is indicated by the RDY/BUSY pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self-clocking mode. Once cleared, the contents of all memory bits return to a logical "1" state.

**Write All**

Upon receiving a WRAL command, address and data, the RDY/BUSY pin goes low (after a delay of  $t_{SV}$  from the positive edge of the  $D_0$  clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width ( $t_{EW}$ ) is timed from the positive edge of the last data bit ( $D_0$ ) and its completion is indicated by the RDY/BUSY pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. It is necessary for all memory locations to be cleared before the WRAL command is executed.

**Figure 5. ERAL Instruction Timing<sup>(5)</sup>**

5060 FHD F07

**Figure 6. WRAL Instruction Timing<sup>(5)</sup>**

5060 FHD F08

Note:

- (5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected,  $AN = A6$  and  $DN = D7$ . When x16 organization is selected,  $AN = A5$  and  $DN = D15$ .