FUJITSU

# MOS 4096-BIT DYNAMIC RANDOM ACCESS MEMORY

# MB 8227N/E/H

S-32 ORIG

002484 JUL 1 4 1980 OBSOLETE

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T-2484 FUJ

## 4,096-BIT DYNAMIC RANDOM ACCESS MEMORY

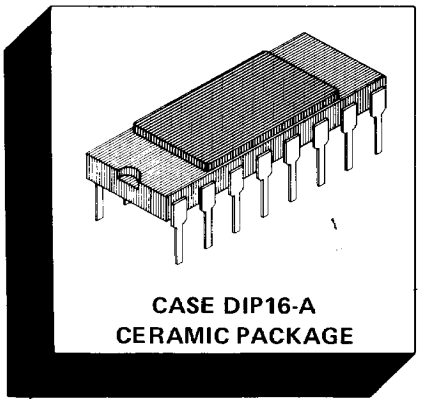
The Fujitsu MB 8227 is a fully decoded, dynamic NMOS random access memory organized as 4,096 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8227 to be housed in a standard 16 pin DIP. Pin-outs conform to the accepted industry standard.

The MB 8227 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerances are 10%. All inputs are TTL compatible; the output is three-state TTL.

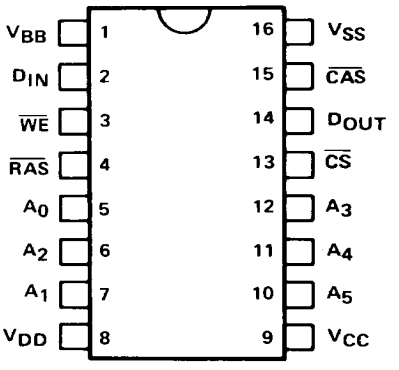
- 4,096 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  150 ns max. (MB 8227H)
  200 ns max. (MB 8227E)
  250 ns max. (MB 8227N)
- Cycle time:
  320 ns min. (MB 8227H)
  375 ns min. (MB 8227E)
  375 ns min. (MB 8227N)
- Low power: 462 mW active, 27 mW standby (max.)
- 10% tolerance on +12V, ±5V, supplies
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 64 refresh cycles



CASE DIP16-A
CERAMIC PACKAGE

- Output latched and valid into next cycle
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses, Data-out, Data-in, and Chip-Select
- Compatible with MK 4027

### PIN ASSIGNMENT



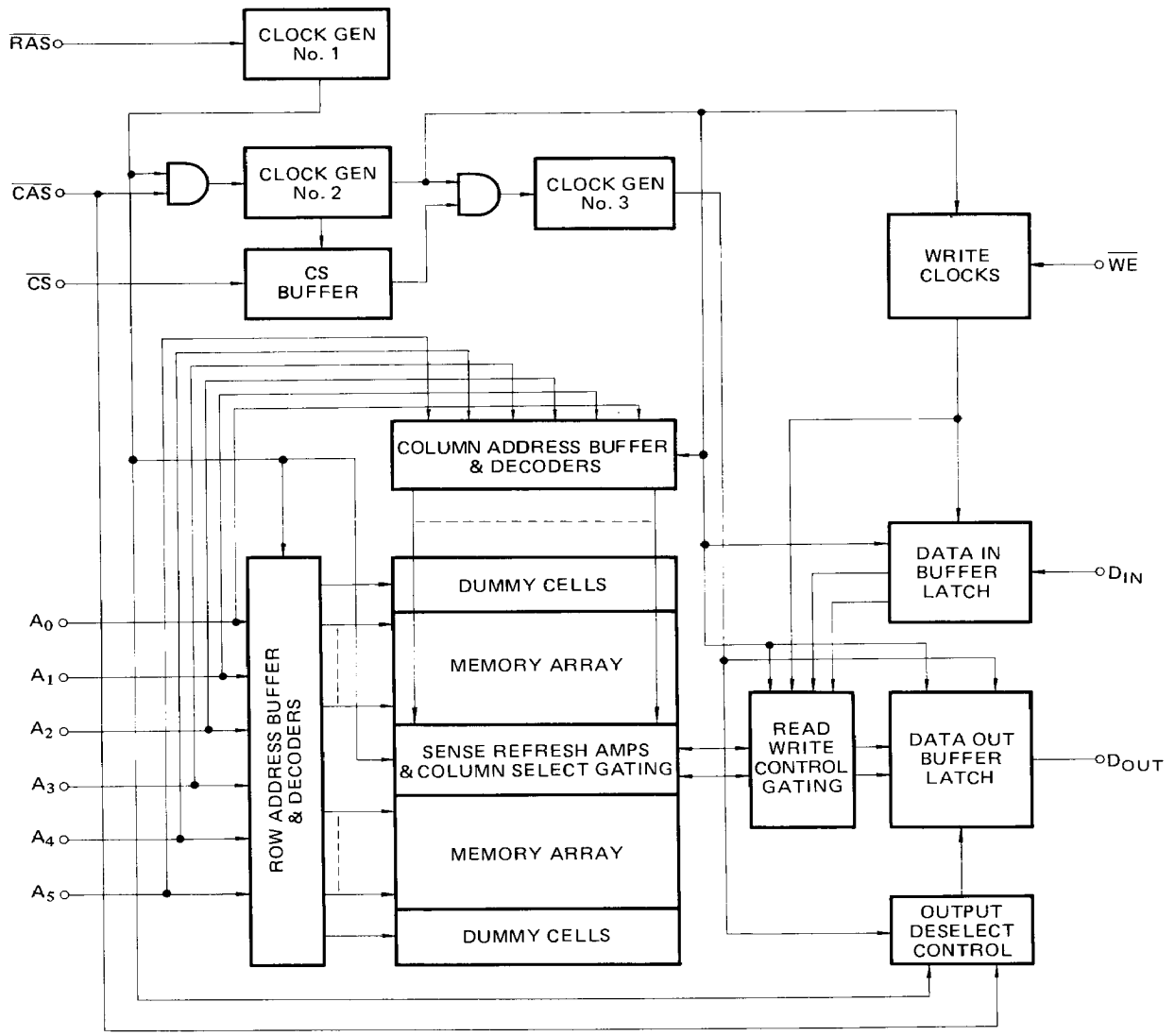

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

### ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{BB}$ | $V_{IN}$, $V_{OUT}$ | -0.5 to +20 | V |
| Voltage on $V_{DD}$, $V_{CC}$ supplies relative to $V_{SS}$ | $V_{DD}$, $V_{CC}$ | -0.5 to +15 | V |
| $V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0V$) | — | 0 | V |
| Storage Temperature | $T_{stg}$ | -55 to +150 | °C |
| Power Dissipation | $P_D$ | 1.0 | W |
| Short circuit output current | — | 50 | mA |

**Note:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Fig. 1 – MB 8227 BLOCK DIAGRAM




## CAPACITANCE

($T_A$ = 25°C)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input Capacitance $A_0 \sim A_5$, $D_{IN}$, $\overline{CS}$ | $C_{IN1}$ | — | 5 | pF |
| Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $C_{IN2}$ | — | 10 | pF |
| Output Capacitance $D_{OUT}$ | $C_{OUT}$ | — | 7 | pF |

## RECOMMENDED OPERATING CONDITIONS

**(Referenced to $V_{SS}$)**

| Parameter | NOTES | Symbol | Min | Typ | Max | Unit | Operating Temperature |
|---|---|---|---|---|---|---|---|
| Supply Voltage | 1 | $V_{DD}$ | 10.8 | 12.0 | 13.2 | V | 0°C to +70°C |
| | 1 2 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| | 1 | $V_{SS}$ | 0 | 0 | 0 | V | |
| | 1 | $V_{BB}$ | -4.5 | -5.0 | -5.5 | V | |
| Input High Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | 1 | $V_{IHC}$ | 2.4 | | 7.0 | V | |
| Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | 1 | $V_{IH}$ | 2.2 | | 7.0 | V | |
| Input Low Voltage, all inputs | 1 | $V_{IL}$ | -1.0 | | 0.8 | V | |

## STATIC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)**

| Parameter | NOTES | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| OPERATING CURRENT<br>Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC}$ min) | | $I_{DD1}$<br>$I_{BB1}$ | | 35<br>300 | mA<br>μA |
| STANDBY CURRENT<br>Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IHC}$, output disabled) | | $I_{DD2}$ | | 2.0 | mA |
| REFRESH CURRENT<br>Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = $V_{IHC}$; $t_{RC}$ min) | | $I_{DD3}$ | | 25 | mA |
| $V_{CC}$ POWER SUPPLY CURRENT ($\overline{CS}$ = $V_{IH}$) | 3 | $I_{CC}$ | -10 | 10 | μA |
| INPUT LEAKAGE CURRENT<br>Input leakage current, any input ($V_{BB}$ = -5V, 0V ≤ $V_{IN}$ ≤ 7V, all other pins not under test = 0V) | | $I_{IL}$ | -10 | 10 | μA |
| OUTPUT LEAKAGE CURRENT<br>(Data out is high impedance state, $\overline{CS}$ = $V_{IH}$, 0V ≤ $V_{OUT}$ ≤ 10V) | | $I_{OL}$ | -10 | 10 | μA |
| OUTPUT LEVELS<br>Output high voltage ($I_{OH}$ = -5mA)<br>Output low voltage ($I_{OL}$ = 3.2mA) | | $V_{OH}$<br>$V_{OL}$ | 2.4 | <br>0.4 | V<br>V |

**Notes:**

1) All voltages are referenced to $V_{SS}$.
2) Output voltage will swing from $V_{SS}$ to $V_{CC}$ when activated with no current loading. For purposes of maintaining data in the standby mode, $V_{CC}$ may be reduced to $V_{SS}$ without affecting refresh operations or data retention. However, the $V_{OH}$ (min) specification is not guaranteed in this mode.
3) When Data out is enabled, $V_{CC}$ power supply current depends upon output loading; $V_{CC}$ is connected to the output buffer only.

# DYNAMIC CHARACTERISTICS

NOTES 4, 5, 6

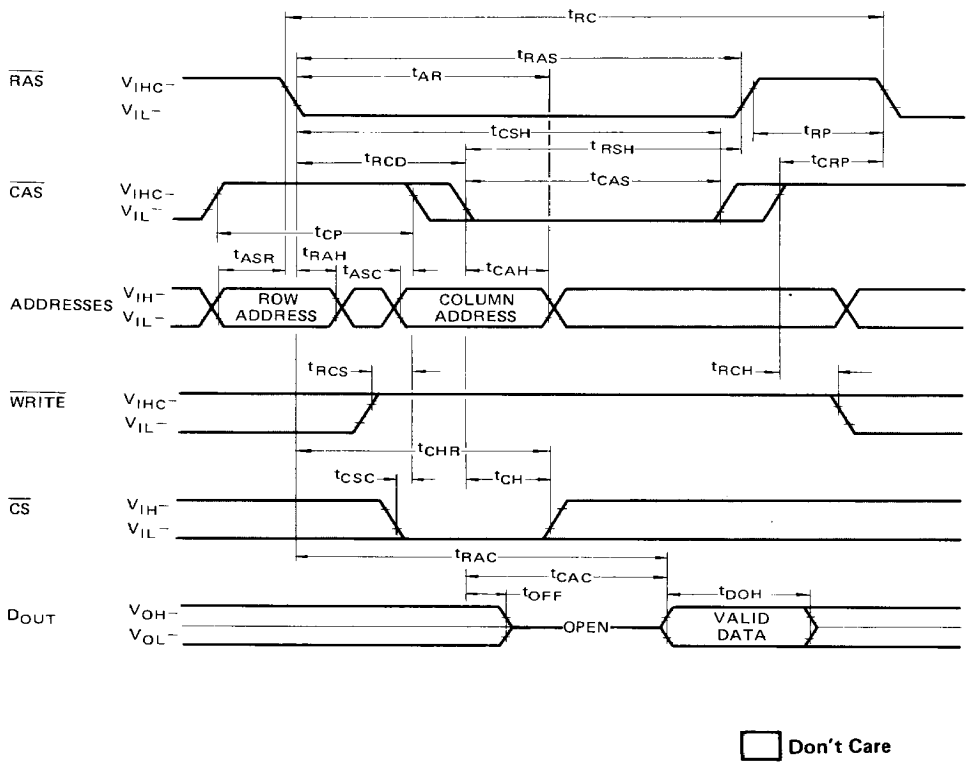
**(Recommended operating conditions unless otherwise noted.)**

| Parameter | NOTES | Symbol | MB 8227N | | MB 8227E | | MB 8227H | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Time between Refresh | | $t_{REF}$ | | 2 | | 2 | | 2 | ms |
| Random Read/Write Cycle Time | | $t_{RC}$ | 375 | | 375 | | 320 | | ns |
| Read-Write Cycle Time | | $t_{RWC}$ | 480 | | 420 | | 330 | | ns |
| Access Time from $\overline{RAS}$ | 7 9 | $t_{RAC}$ | | 250 | | 200 | | 150 | ns |
| Access Time from $\overline{CAS}$ | 8 9 | $t_{CAC}$ | | 165 | | 135 | | 100 | ns |
| Output Buffer Turn Off Delay | | $t_{OFF}$ | | 60 | | 50 | | 40 | ns |
| Transition Time | | $t_T$ | 3 | 50 | 3 | 50 | 3 | 35 | ns |
| $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 120 | | 120 | | 100 | | ns |
| $\overline{RAS}$ Pulse Width | | $t_{RAS}$ | 250 | 32000 | 200 | 32000 | 150 | 32000 | ns |
| $\overline{RAS}$ Hold Time | | $t_{RSH}$ | 165 | | 135 | | 100 | | ns |
| $\overline{CAS}$ Precharge Time | | $t_{CP}$ | 110 | | 80 | | 60 | | ns |
| $\overline{CAS}$ Pulse Width | | $t_{CAS}$ | 165 | | 135 | | 100 | | ns |
| $\overline{CAS}$ Hold Time | | $t_{CSH}$ | 250 | | 200 | | 150 | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | 10 | $t_{RCD}$ | 40 | 85 | 30 | 65 | 25 | 50 | ns |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | | $t_{CRP}$ | 0 | | 0 | | 0 | | ns |
| Row Address Set Up Time | | $t_{ASR}$ | 0 | | 0 | | 0 | | ns |
| Row Address Hold Time | | $t_{RAH}$ | 35 | | 25 | | 20 | | ns |
| Column Address Set Up Time | | $t_{ASC}$ | -5 | | -5 | | -5 | | ns |
| Column Address Hold Time | | $t_{CAH}$ | 75 | | 55 | | 45 | | ns |
| Column Address Hold Time Referenced to $\overline{RAS}$ | | $t_{AR}$ | 160 | | 120 | | 95 | | ns |
| Chip Select Set Up Time | | $t_{CSC}$ | -5 | | -5 | | -5 | | ns |
| Chip Select Hold Time | | $t_{CH}$ | 75 | | 55 | | 45 | | ns |
| Chip Select Hold Time Referenced to $\overline{RAS}$ | | $t_{CHR}$ | 160 | | 120 | | 95 | | ns |
| Read Command Set Up Time | | $t_{RCS}$ | 0 | | 0 | | 0 | | ns |
| Read Command Hold Time | | $t_{RCH}$ | 0 | | 0 | | 0 | | ns |
| Write Command Set Up Time | 11 | $t_{WCS}$ | 0 | | 0 | | 0 | | ns |
| Write Command Hold Time | | $t_{WCH}$ | 75 | | 55 | | 45 | | ns |
| Write Command Hold Time Referenced to $\overline{RAS}$ | | $t_{WCR}$ | 160 | | 120 | | 95 | | ns |
| Write Command Pulse Width | | $t_{WP}$ | 75 | | 55 | | 45 | | ns |
| Write Command to $\overline{RAS}$ Lead Time | | $t_{RWL}$ | 85 | | 70 | | 60 | | ns |
| Write Command to $\overline{CAS}$ Lead Time | | $t_{CWL}$ | 85 | | 70 | | 60 | | ns |
| Data In Set Up Time | | $t_{DS}$ | 0 | | 0 | | 0 | | ns |
| Data In Hold Time | | $t_{DH}$ | 75 | | 55 | | 45 | | ns |
| Data In Hold Time Referenced to $\overline{RAS}$ | | $t_{DHR}$ | 160 | | 120 | | 95 | | ns |
| $\overline{CAS}$ to $\overline{WE}$ Delay | 11 | $t_{CWD}$ | 90 | | 80 | | 60 | | ns |
| $\overline{RAS}$ to $\overline{WE}$ Delay | 11 | $t_{RWD}$ | 175 | | 145 | | 110 | | ns |
| Data Out Hold Time | | $t_{DOH}$ | 32 | | 32 | | 32 | | μs |

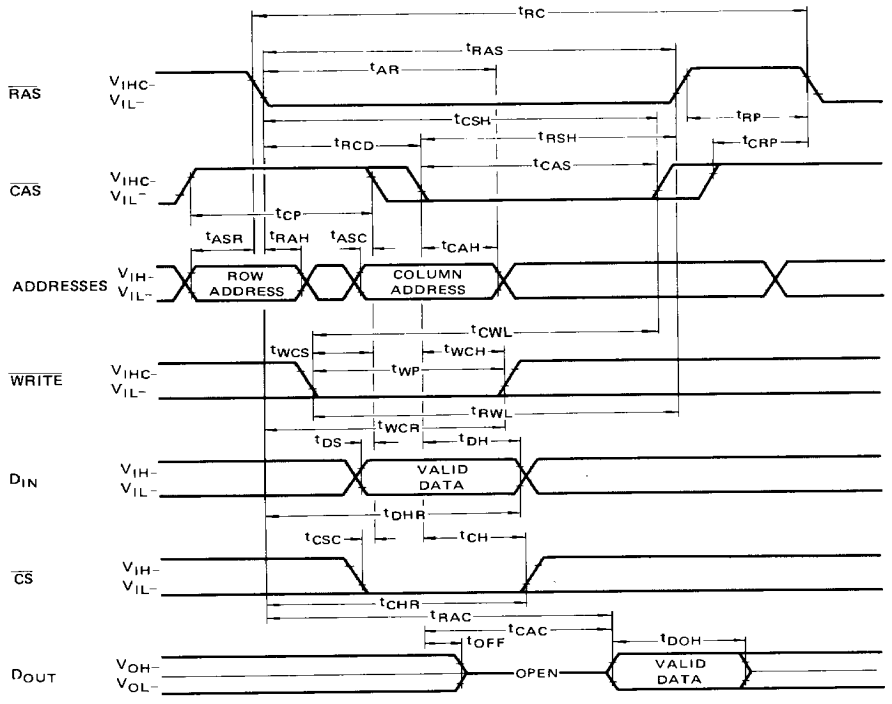
**Notes:**

4) Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5) Dynamic measurements assume $t_T$=5ns.
6) $V_{IHC}$ (min) or $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IHC}$ or $V_{IH}$ and $V_{IL}$.
7) Assumes that $t_{RCD} \leqslant t_{RCD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the value shown.
8) Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).
9) Measured with a load equivalent to 2 TTL loads and 100pF.
10) Operation within the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
11) $t_{WCS}$, $t_{CWD}$ and $t_{RWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and $D_{OUT}$ will contain the data written into the selected cell.
If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

## Read Cycle Timing Diagram

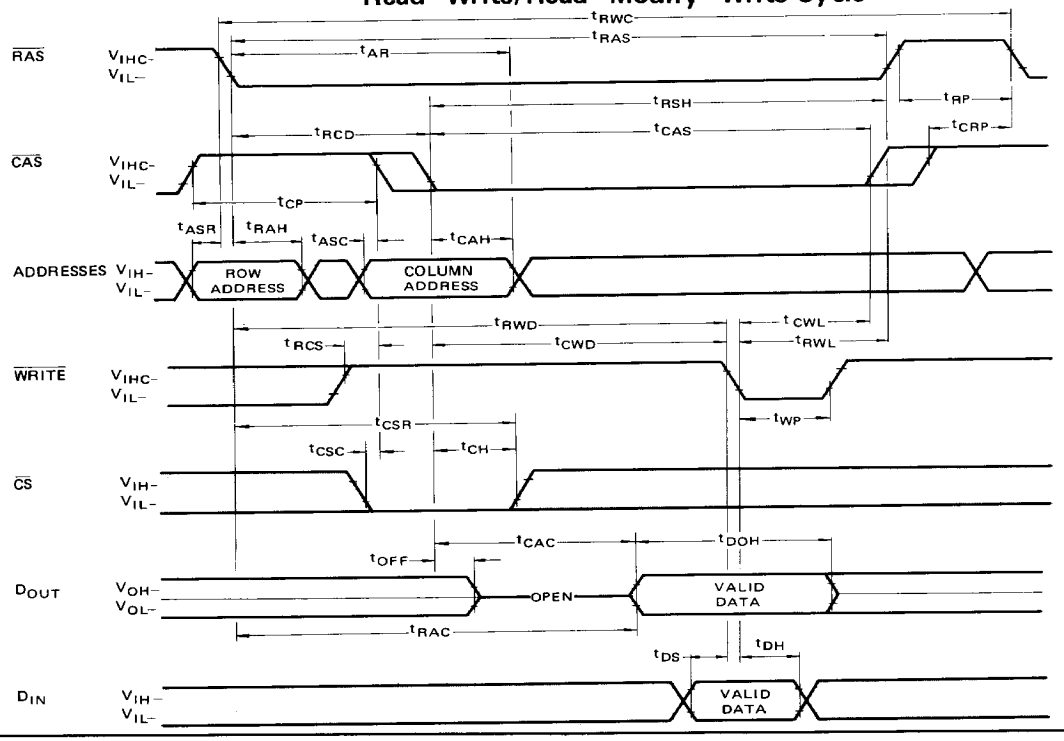


## Write Cycle (Early Write)




Don't Care

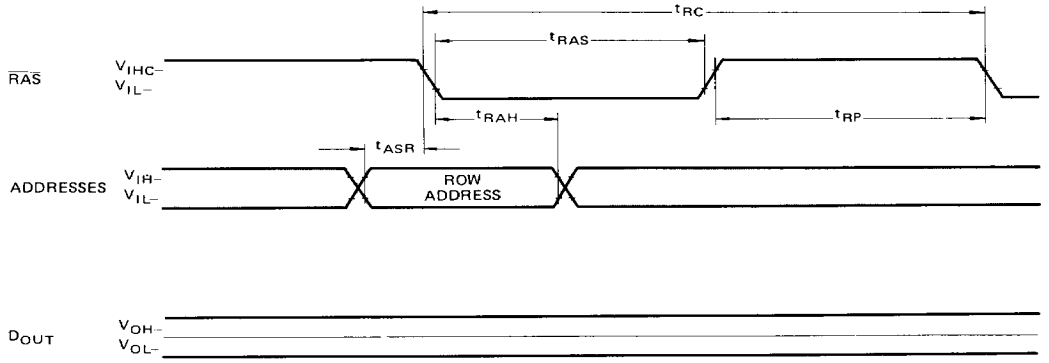
## Read–Write/Read–Modify–Write Cycle




Don't Care

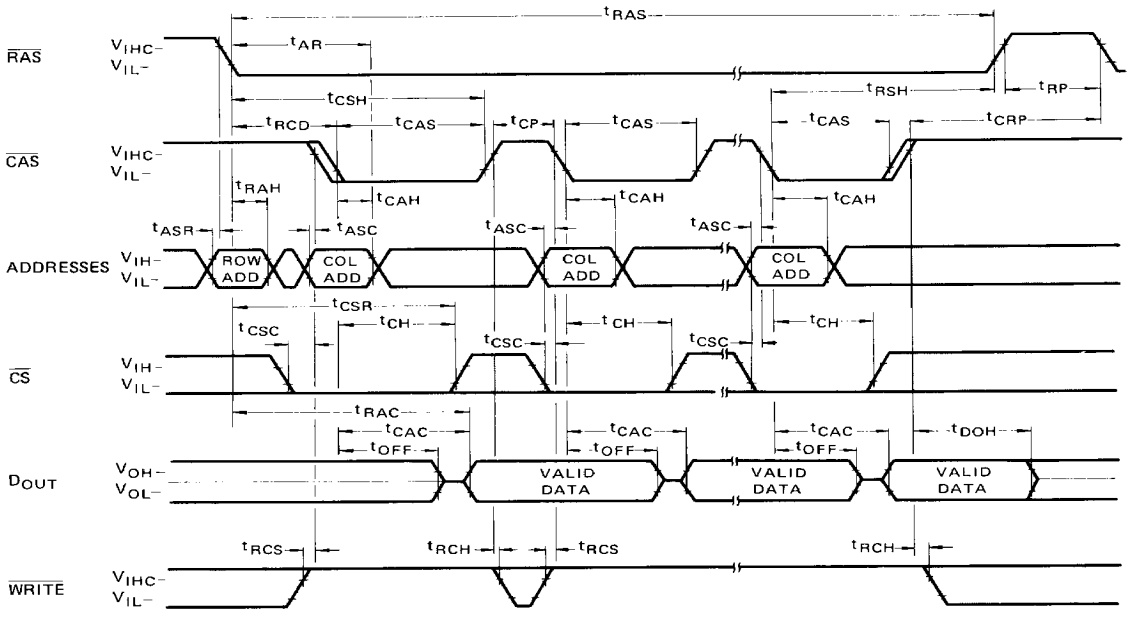
## "RAS–ONLY" Refresh Cycle

**NOTE:** $D_{OUT}$ remains unchanged from previous cycle.



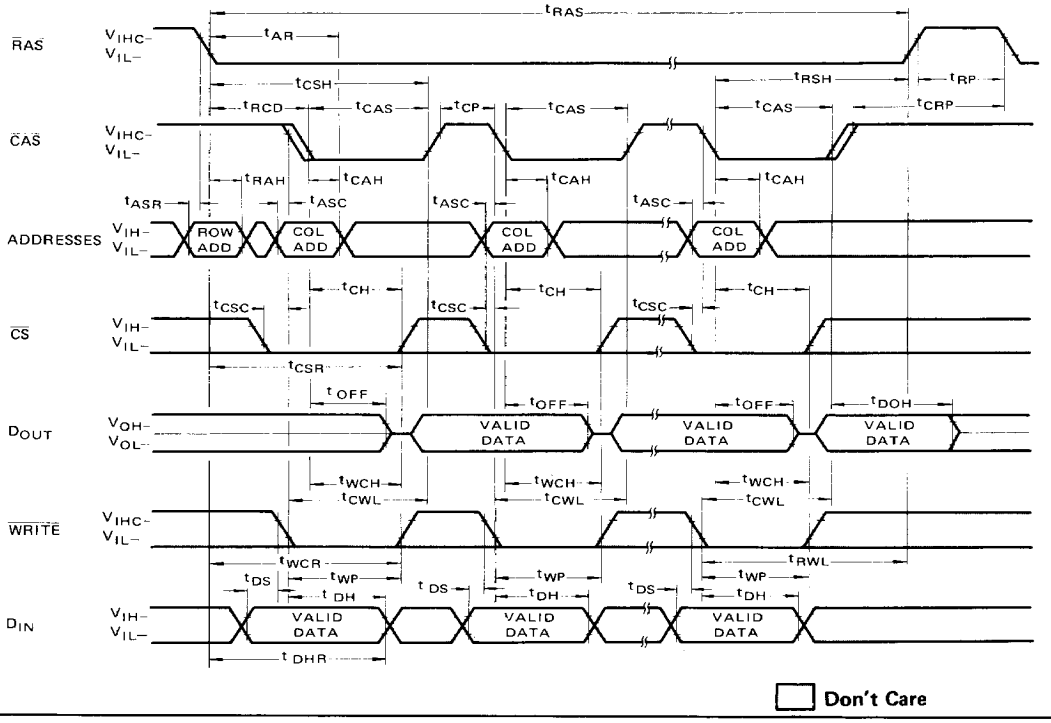

Don't Care

## Page Mode Read Cycle




Don't Care

## Page Mode Write Cycle




# DESCRIPTION

**Address Inputs:**
Twelve binary input address bits are required to decode any one of the 4096 storage locations of the MB 8227. The twelve input address bits are multiplexed, six at a time, into the chip via the address input pins ($A_0$ through $A_5$). The Row Address Strobe, $\overline{RAS}$, latches the 6 row address bits when a negative going TTL level clock is applied to $\overline{RAS}$; and the Column Address Strobe, $\overline{CAS}$, latches the 6 column address bits plus Chip Select, $\overline{CS}$, when a subsequent negative going TTL level clock is applied to $\overline{CAS}$. $\overline{CAS}$ is internally "gated" by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time ($t_{RAH}$) specification has been satisfied and before column address information is actually required. This gated $\overline{CAS}$ feature simplifies timing requirements for multiplexed inputs and minimizes the system access and cycle time.

**Write Enable:**
The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. The data input pin is disabled when the read mode is selected. $\overline{WE}$ can be driven by a standard TTL circuit without a pull-up resistor.

**Data Input:**
Data to be written into a selected memory cell is latched into an on-chip register during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, strobes the Data in ($D_{IN}$) register. Set-up and hold times are referenced to $\overline{WE}$ or $\overline{CAS}$, whichever negative transition occurs later. If the chip is unselected, $\overline{CS}$ high at $\overline{CAS}$ time, $\overline{WE}$ commands are not executed and data in the memory is not affected.

**Data Output:**
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output data is latched until $\overline{CAS}$ is brought low. Then the output, $D_{OUT}$, will go to an open circuit regardless of the state of any other input pin. In a read, read-modify-write, or delayed write cycle, if the chip is selected, the output latch and buffer will contain the data read from the selected memory cell after access time. In a write cycle ($\overline{WE}$ low before $\overline{CAS}$ low), if the chip is selected, the output latch and buffer will contain the input

(cont'd)

data after access time. The output remains valid until the next negative transition of $\overline{CAS}$. $\overline{RAS}$-only refresh cycles will not affect valid data.

**Page-Mode:**

Page-mode operation permits strobing the row-address into the MB 8227 while holding $\overline{RAS}$ at a logic low(0) throughout all successive memory operations in which the row address does not change. This permits successive memory operations at multiple column addresses with the same row address with higher speed and lower power. The power dissipated by the negative going edge of $\overline{RAS}$ is saved; and the access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

**Refresh:**

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 64 row addresses at least every two milliseconds. Any operation in which $\overline{RAS}$ transits accomplishes refresh. Regardless of the state of $\overline{CS}$, a read cycle will refresh the selected row. Refresh will also occur during a write or read-modify-write cycle, but the chip should be unselected to prevent data being written into the selected memory location. If, during a refresh cycle, the MB 8227 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if $\overline{RAS}$-only refresh is continued for long periods, the output buffer may lose data. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

**Power Considerations:**

The output buffer of the MB 8227 can be powered via $V_{CC}$ from the supply voltage (normally 5 volts) to which the memory is interfaced. In standby operation, $V_{CC}$ may be removed without affecting refresh. Thus standby power is conserved because all memory functions may be turned off except for $\overline{RAS}$ timing and refresh addresses.

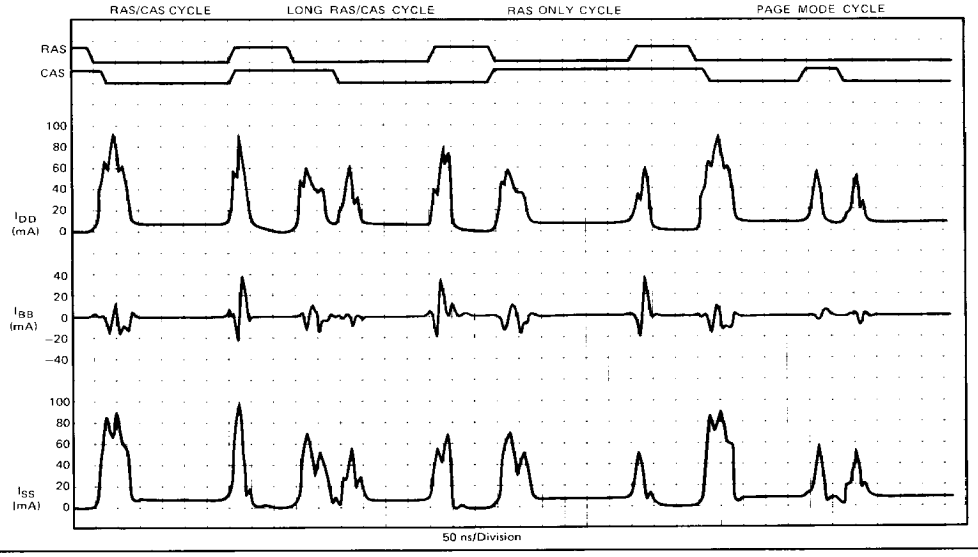
Most of the MB 8227 circuitry, including sense amplifiers, is dynamic, and most of the power drain comes from an address strobe ($\overline{RAS}$ or $\overline{CAS}$) edge. Thus, dynamic power dissipation depends mostly on operating frequency. To minimize power dissipation, the Row Address Strobe, $\overline{RAS}$, should only be applied to selected IC's. $\overline{CAS}$ must be supplied to all the IC's in a system in order to turn off unselected outputs. But IC's that didn't receive a $\overline{RAS}$ input will not dissipate power on $\overline{CAS}$ edges except for that needed to turn off outputs. If $\overline{RAS}$ is supplied only to selected chips, $\overline{CS}$ can be at logic zero. Chips that receive $\overline{CAS}$, but not $\overline{RAS}$, will be unselected regardless of $\overline{CS}$. However, for refresh, either the $\overline{CS}$ input or $\overline{CAS}$ must be high to prevent wired-OR outputs from turning on simultaneously.

**Power Up:**

No particular power supply sequencing is required for the MB 8227. However, absolute maximum ratings must be adhered to. Thus, $V_{BB}$ should be turned on first and turned off last, and $V_{BB}$ should be less than $V_{SS}$ when $V_{DD}$ is turned on. After power is applied, several cycles are required before proper operation is assured. About eight refresh cycles should be sufficient to accomplish this.

## Current Waveforms

**NOTE:** $V_{DD}$ = 13.2V, $V_{BB}$ = −4.5V, $T_A$ = 25°C



# TYPICAL CHARACTERISTICS CURVES

Fig. 2 – NORMALIZED ACCESS TIME vs $V_{DD}$ SUPPLY VOLTAGE

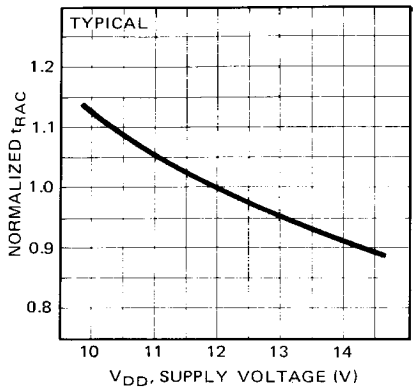



Fig. 3 – NORMALIZED ACCESS TIME vs $V_{BB}$ SUPPLY VOLTAGE

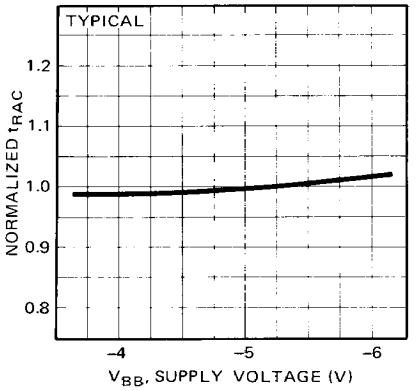



Fig. 4 – NORMALIZED ACCESS TIME vs $V_{CC}$ SUPPLY VOLTAGE

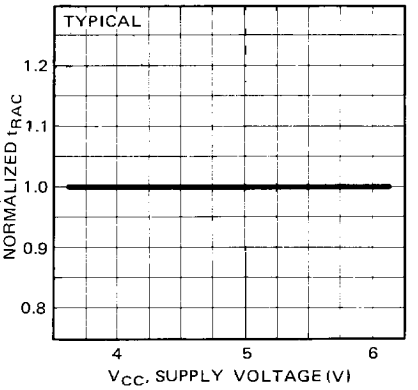



Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

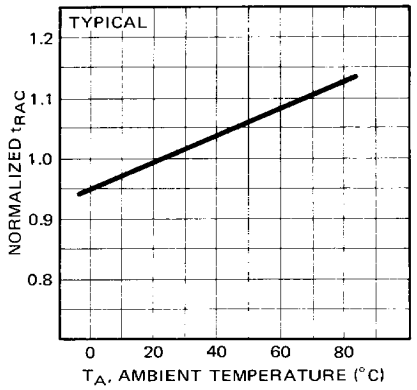



Fig. 6 – $I_{DD1}$ (AVERAGE) vs CYCLE RATE

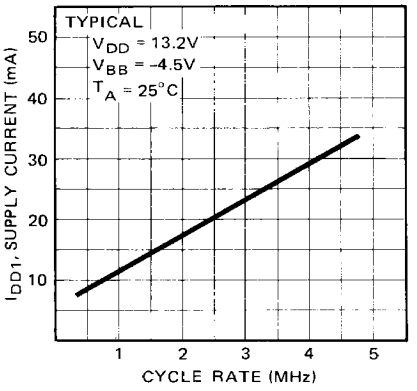



Fig. 7 – $I_{DD1}$ (AVERAGE) vs $V_{DD}$ SUPPLY VOLTAGE

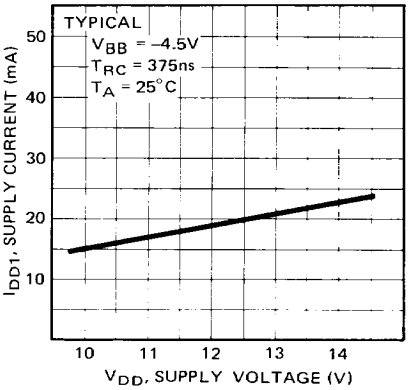



Fig. 8 – $I_{DD1}$ (AVERAGE) vs AMBIENT TEMPERATURE

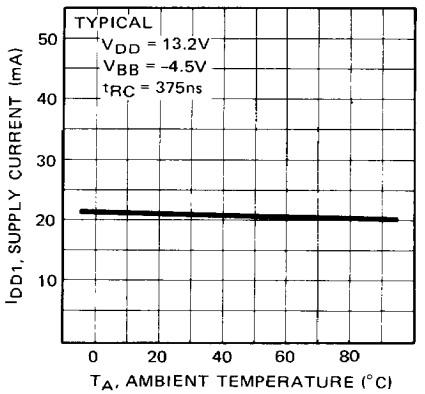



Fig. 9 – $I_{DD2}$ (STANDBY) vs $V_{DD}$ SUPPLY VOLTAGE

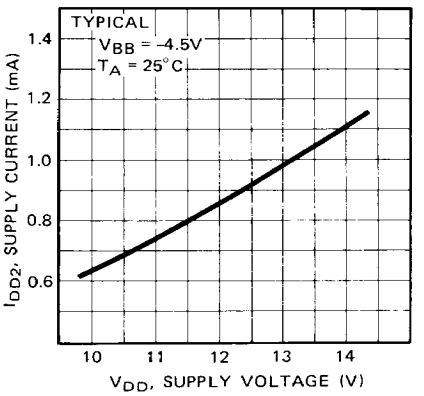



Fig. 10 – $I_{DD2}$ (STANDBY) vs AMBIENT TEMPERATURE

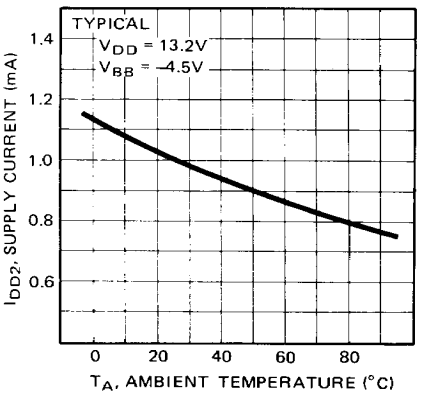


Fig. 11 – $I_{DD3}$ (RAS-ONLY) vs CYCLE RATE

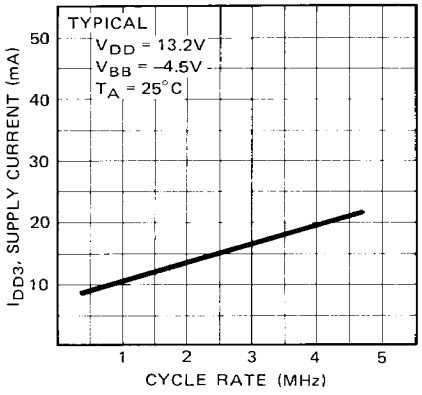



Fig. 12 – $I_{DD3}$ (RAS-ONLY) vs $V_{DD}$ SUPPLY VOLTAGE

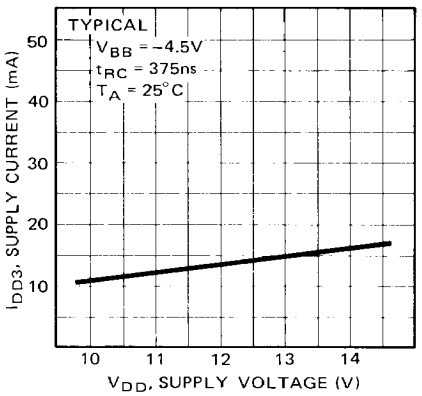



Fig. 13 – $I_{DD3}$ (RAS-ONLY) vs AMBIENT TEMPERATURE

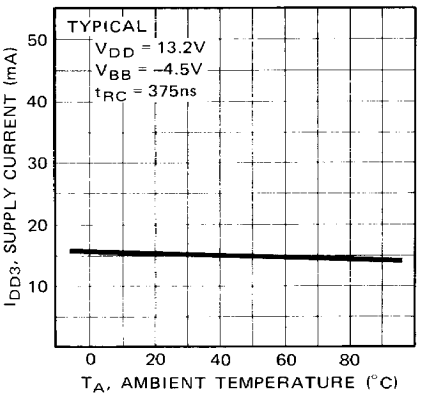



Fig. 14 – $V_{IHC}$, $V_{ILC}$ INPUT LEVELS vs $V_{DD}$ SUPPLY VOLTAGE

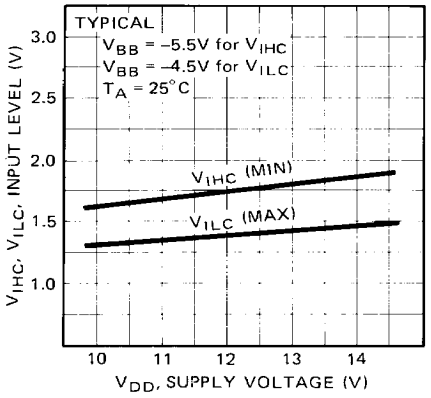



Fig. 15 – $V_{IHC}$, $V_{ILC}$ INPUT LEVELS vs $V_{BB}$ SUPPLY VOLTAGE

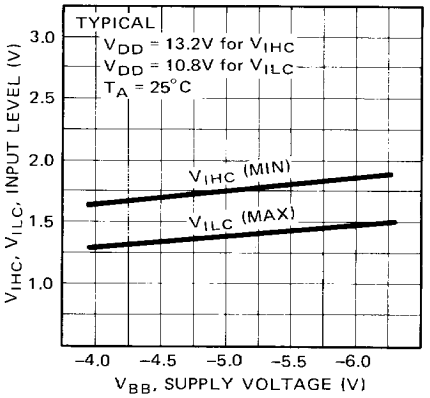



Fig. 16 – $V_{IHC}$, $V_{ILC}$ INPUT LEVELS vs AMBIENT TEMPERATURE

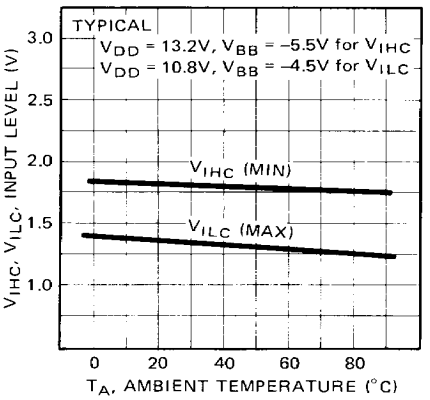



Fig. 17 – $V_{IH}$, $V_{IL}$ INPUT LEVELS vs $V_{DD}$ SUPPLY VOLTAGE

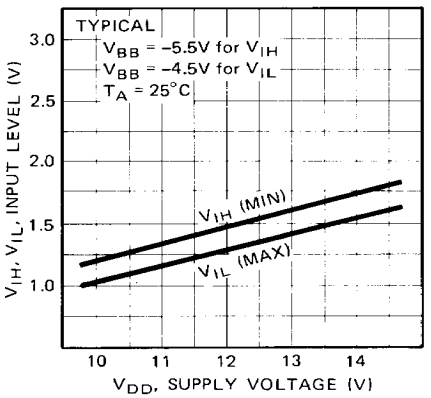



Fig. 18 – $V_{IH}$, $V_{IL}$ INPUT LEVELS vs $V_{BB}$ SUPPLY VOLTAGE

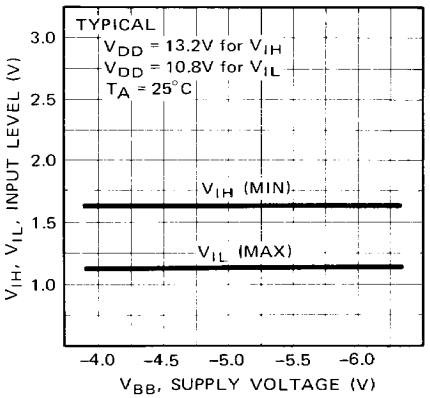
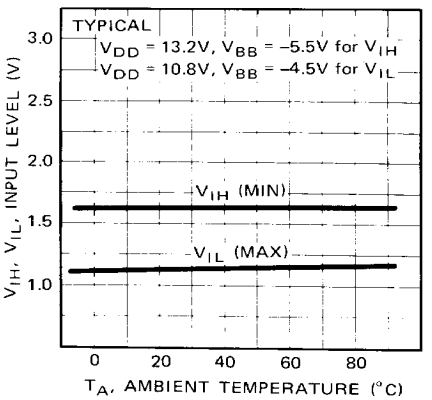
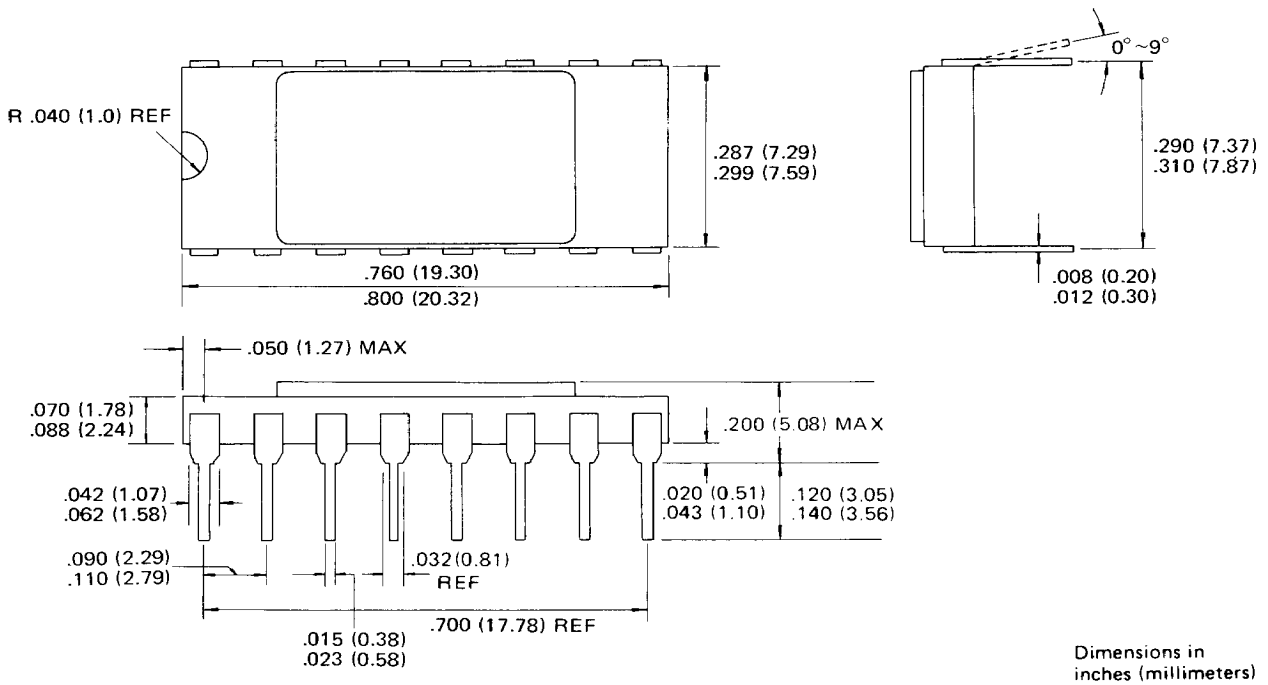



Fig. 19 – $V_{IH}$, $V_{IL}$ INPUT LEVELS vs AMBIENT TEMPERATURE



# PACKAGE DIMENSIONS

16-LEAD CERAMIC DUAL-iN-LINE PACKAGE
(CASE DIP 16-A)




Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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