Features

- 50 ns worst-case multiply time
- Low-power CMOS technology
- Replaces TRW MPY112K
- Two's complement or unsigned operands
- Three-state outputs
- Available screened to MIL-STD-883, Class B
- Package styles available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP

Description

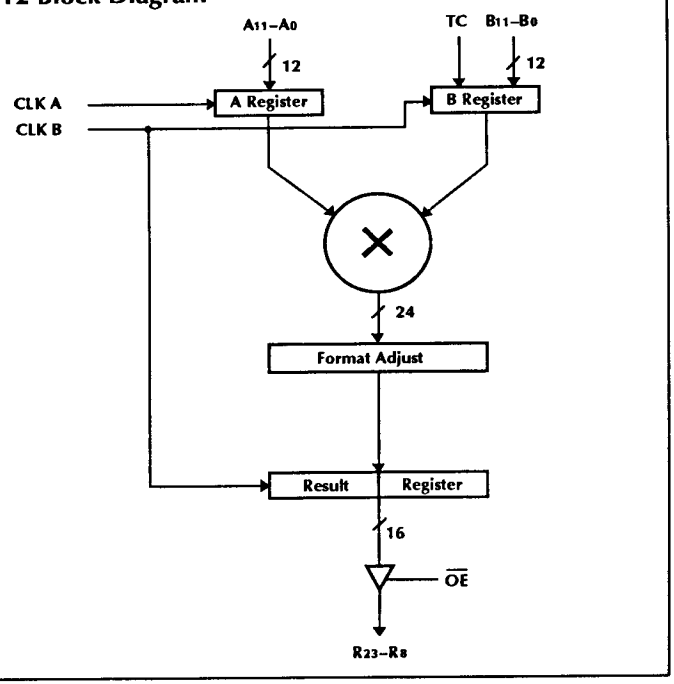
The **LMU112** is a high-speed, low power, 12-bit parallel multiplier built using advanced CMOS technology. The LMU112 is pin and functionally compatible with TRW's MPY112K.

The A and B input operands are loaded into their respective registers on the rising edge of the separate clock inputs (CLK A and CLK B). Two's complement or unsigned magnitude operands are accommodated via the operand control bit, TC, which is loaded along with the B operands. The operands are specified to be in two's complement format when TC is asserted and unsigned magnitude when TC is de-asserted. Mixed mode operation is not allowed.

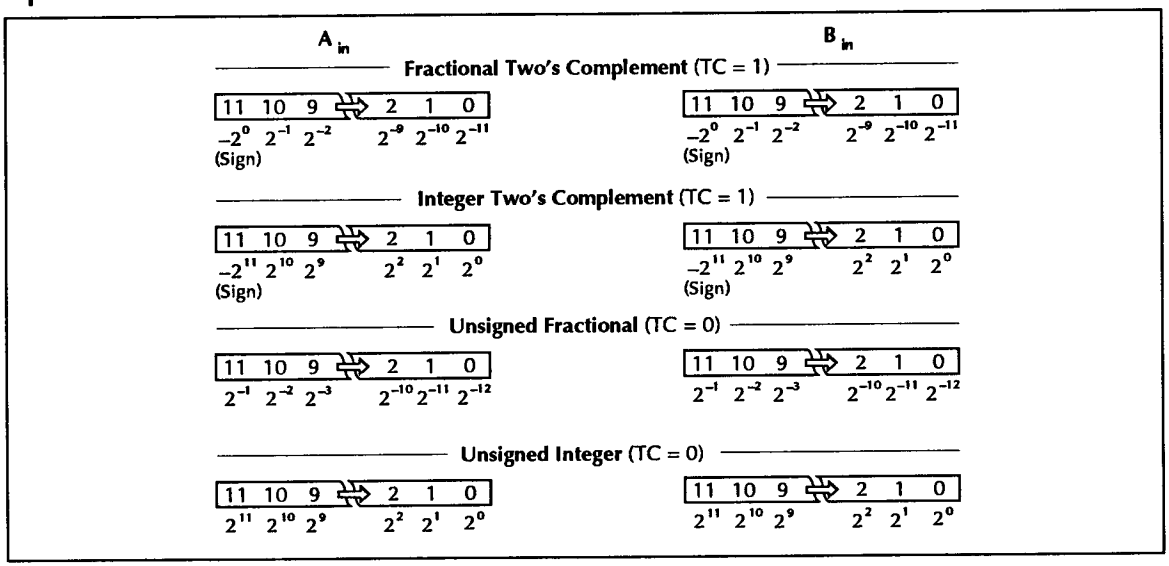
For two's complement operands, the 17 most significant bits at the output of the asynchronous multiplier array are shifted one bit position to the left. This is done to discard the redundant copy of the sign-bit, which is in the most significant bit position, and extend the bit precision by one bit. The result is then truncated to the 16 MSB's and loaded into the output register on the rising edge of CLK B.

The contents of the output register are made available via three-state buffers by asserting $\overline{OE}$. When $\overline{OE}$ is de-asserted, the outputs (R23–R8) are in the high impedance state.

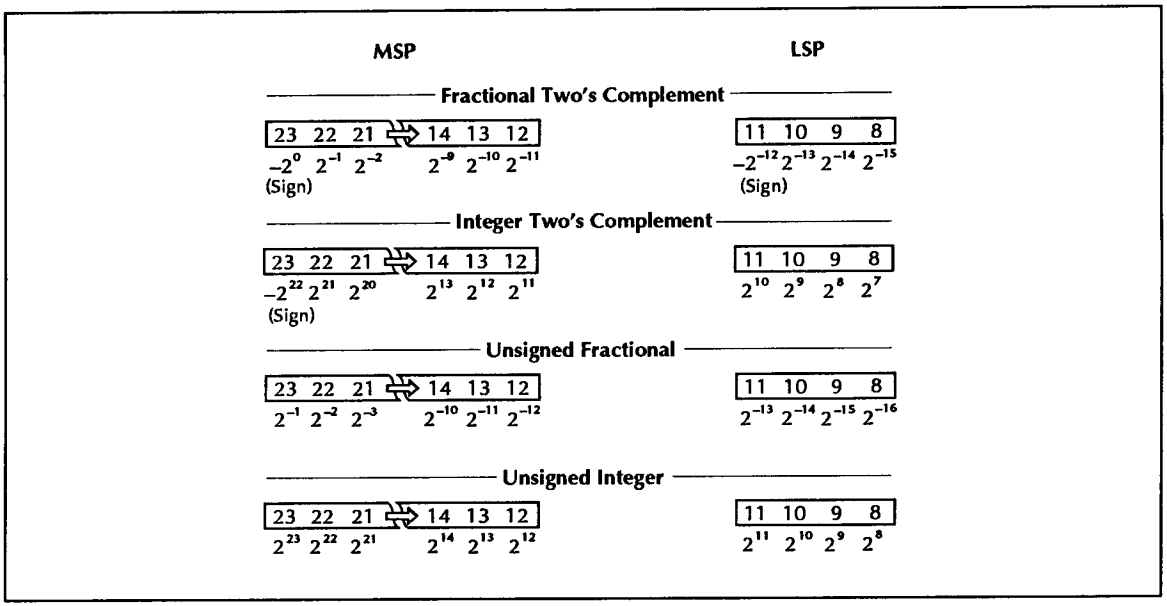
LMU112 Block Diagram



Input Formats



Output Formats



Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	Note 3	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_I ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_O ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_O = Ground, Vcc = Max, Note 4, 8			–250	mA
I_{CC1}	Vcc Current, Dynamic	Notes 5, 6		10	20	mA
I_{CC2}	Vcc Current, Quiescent	Note 7			1.0	mA

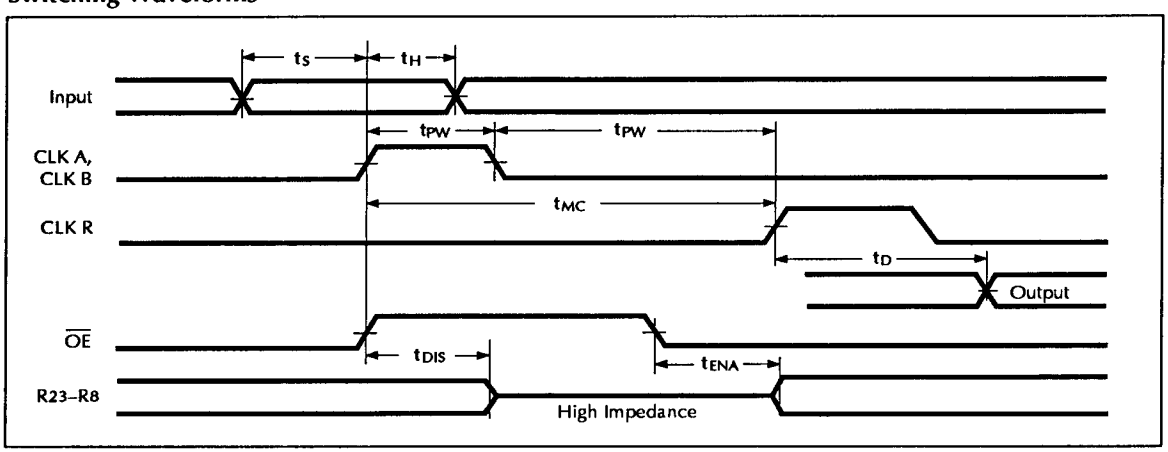
Switching Characteristics *Over Commercial Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU112-60		LMU112-50	
		Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		60		50
t_D	Output Delay		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25
t_{PW}	Clock Pulse Width	15		15	
t_H	Input Register Hold Time	0		0	
t_S	Input Register Setup Time	15		15	

Switching Characteristics *Over Military Operating Range (Notes 9, 10) (ns)*

Symbol	Parameter	LMU112-65		LMU112-55	
		Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55
t_D	Output Delay		30		30
t_{ENA}	Output Enable Time (Note 11)		30		30
t_{DIS}	Output Disable Time (Note 11)		30		30
t_{PW}	Clock Pulse Width	20		20	
t_H	Input Register Hold Time	0		0	
t_S	Input Register Setup Time	15		15	

Switching Waveforms



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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Ordering Information

Commercial Operating Range (0°C to +70°C)

Package Style	Performance	
	60 ns	50 ns
48-pin Plastic DIP (0.6") — P5	LMU112PC60	LMU112PC50
48-pin Sidebraze (0.6") Hermetic DIP — D5	LMU112DC60	LMU112DC50

Military Operating Range (–55°C to +125°C)

Package Style	Performance	
	65 ns	55 ns
48-pin Sidebraze (0.6") Hermetic DIP — D5	LMU112DM65 LMU112DME65 LMU112DMB65	LMU112DM55 LMU112DME55 LMU112DMB55

Pin Assignments

Pin	Function	Pin	Function
1	A10	25	R18
2	A11	26	R17
3	B0	27	R16
4	B1	28	R15
5	B2	29	R14
6	B3	30	R13
7	B4	31	R12
8	B5	32	R11
9	B6	33	R10
10	B7	34	R9
11	B8	35	R8
12	VCC	36	GND
13	VCC	37	GND
14	B9	38	CLK A
15	B10	39	A0
16	B11	40	A1
17	TC	41	A2
18	CLK B	42	A3
19	$\overline{OE}$	43	A4
20	R23	44	A5
21	R22	45	A6
22	R21	46	A7
23	R20	47	A8
24	R19	48	A9

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