National Semiconductor

# DS3896/DS3897 BTL Trapezoidal™ Transceivers

## General Description

These advanced transceivers are specifically designed to overcome problems associated with driving a densely populated backplane, and thus provide significant improvement in both speed and data integrity. Their low output capacitance, low output signal swing and noise immunity features make them ideal for driving low impedance buses with minimum power consumption.

The DS3896 is an octal high speed schottky bus transceiver with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. On the other hand, the DS3896 provides high package density for data/address lines.

The open collector drivers generate precise trapezoidal waveforms, which are relatively independent of capacitive loading conditions on the outputs. This significantly reduces noise coupling to adjacent lines. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity and provide equal rejection to both negative and positive going noise pulses on the bus.

To minimize bus loading, these devices also feature a schottky diode in series with the open collector output that isolates the driver output capacitance in the disabled state. The output low voltage is typically "1V" and the output high level is intended to be 2V. This is achieved by terminating the bus with a pull up resistor to 2V at both ends. The device can drive an equivalent DC load of 18.5Ω (or greater) in the above configuration.

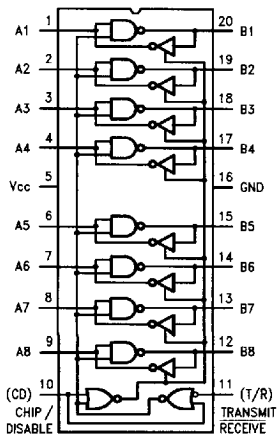
These signalling requirements, including a 1 volt signal swing, low output capacitance and precise receiver thresholds are referred to as Bus Transceiver Logic (BTL™).

## Features

- 8 bit DS3896 transceiver provides high package density
- 4 bit DS3897 transceiver provides separate driver input and receiver output pins
- BTL compatible
- Less than 5 pF output capacitance for minimal bus loading
- 1 Volt bus signal swing reduces power consumption
- Trapezoidal driver waveforms ($t_r$, $t_f \cong 6$ ns typical) reduce noise coupling to adjacent lines
- Temperature insensitive receiver thresholds track the bus logic high level to maximize noise immunity in both high and low states
- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs and receiver outputs

## Logic Diagrams

**DS3896N, M**

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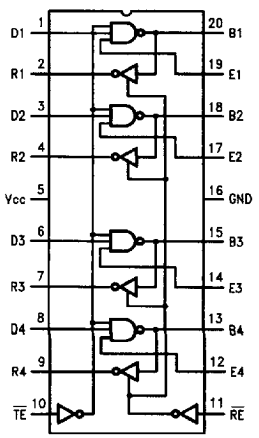
**DS3897N, J, M**

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 6V |
| Control Input Voltage | 5.5V |
| Driver Input and Receiver Output | 5.5V |
| Receiver Input and Driver Output | 2.5V |
| Power Dissipation at 70°C N Package | 1480 mW |
| J Package | 1250 mW |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage, $V_{CC}$ | 4.75 | 5.25 | V |
| Bus Termination Voltage | 1.90 | 2.10 | V |
| Operating Free Air Temperature | 0 | 70 | °C |

## Electrical Characteristics: (Note 2 and 3) ($0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Driver and Control Inputs: (An, Dn, En, CD, T/$\overline{R}$, $\overline{RE}$, $\overline{TE}$)** | | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | | 2.0 | | | V |
| $V_{IL}$ | Logical "0" Input Voltage | | | | 0.8 | V |
| $I_I$ | Logical "1" Input Current | An = Dn = En = $V_{CC}$ | | | 1 | mA |
| $I_{IH}$ | Logical "1" Input Current | An = Dn = En = 2.4V | | | 40 | μA |
| $I_{IL}$ | Logical "0" Input Current | An = Dn = En = 0.4V | | −1 | −1.6 | mA |
| $I_{ILC}$ | Logical "0" Input Current | CD = T/$\overline{R}$ = $\overline{RE}$ = $\overline{TE}$ = 0.4V | | −180 | −400 | μA |
| $V_{CL}$ | Input Diode Clamp Voltage | Iclamp = −12 mA | | −0.9 | −1.5 | V |
| **Driver Output/Receiver Input: (Bn)** | | | | | | |
| $V_{OLB}$ | Low Level Bus Voltage | An = Dn = En = T/$\overline{R}$ = 2V, VL = 2V<br>RL = 18.5Ω, CD = $\overline{TE}$ = 0.8V (*Figure 1*) | 0.75 | 1.0 | 1.2 | V |
| $I_{IHB}$ | Maximum Bus Current (Power On) | An = Dn = En = 0.8V, $V_{CC}$ = 5.25V<br>Bn = 2V | | 10 | 100 | μA |
| $I_{ILB}$ | Maximum Bus Current (Power Off) | An = Dn = En = 0.8V, $V_{CC}$ = 0V<br>Bn = 2V | | | 100 | μA |
| $V_{TH}$ | Receiver Input Threshold | $V_{CC}$ = 5V | 1.47 | 1.55 | 1.62 | V |
| **Receiver Output: (An, Rn)** | | | | | | |
| $V_{OH}$ | Logical "1" Output Voltage | Bn = 1.2V, $I_{OH}$ = −400 μA<br>CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V | 2.4 | 3.2 | | V |
| $V_{OL}$ | Logical "0" Output Voltage | Bn = 2V, $I_{OL}$ = 16 mA<br>CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V | | 0.35 | 0.5 | V |
| $I_{OS}$ | Output Short Circuit Current | Bn = 1.2V<br>CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V | −20 | −70 | −100 | mA |
| $I_{CC}$ | Supply Current (DS3896) | $V_{CC}$ = 5.25V | | 90 | 135 | mA |
| $I_{CC}$ | Supply Current (DS3897) | $V_{CC}$ = 5.25V | | 50 | 80 | mA |

**Note 1.** "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristic" provide conditions for actual device operation.

**Note 2.** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

**Note 3.** All typicals are given for $V_{CC}$ = 5V and $T_a$ = 25°C.

## DS3896 Switching Characteristics

**(0°C ≤ $T_A$ ≤ 70°C, 4.75V ≤ $V_{CC}$ ≤ 5.25V** unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Driver:** | | | | | | |
| $t_{DLH}$ | An to Bn | CD = 0.8V, T/$\overline{R}$ = 2.0V, VL = 2V | 5 | 9 | 15 | ns |
| $t_{DHL}$ | | *(Figure 2)* | 5 | 9 | 15 | ns |
| $t_{DLHC}$ | CD to Bn | An = T/$\overline{R}$ = 2.0V, VL = 2V | 5 | 10 | 18 | ns |
| $t_{DHLC}$ | | *(Figure 2)* | 5 | 12 | 20 | ns |
| $t_{DLHT}$ | T/$\overline{R}$ to Bn | VCI = An, VC = 5V, *(Figure 5)* | 5 | 15 | 25 | ns |
| $t_{DHLT}$ | | CD = 0.8V, RC = 390Ω, CL = 30 pF<br>RL1 = 18Ω, RL2 = NC, VL = 2V | 5 | 22 | 35 | ns |
| $t_R$ | Driver Output Rise Time | CD = 0.8V, T/$\overline{R}$ = 2V, VL = 2V | 3 | 6 | 10 | ns |
| $t_F$ | Driver Output Fall Time | *(Figure 2)* | 3 | 6 | 10 | ns |
| **Receiver:** | | | | | | |
| $t_{RLH}$ | Bn to An | CD = 0.8V, T/$\overline{R}$ = 0.8V | 5 | 12 | 18 | ns |
| $t_{RHL}$ | | *(Figure 3)* | 5 | 10 | 18 | ns |
| $t_{RLZC}$ | CD to An | Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 5 pF<br>RL1 = 390Ω, RL2 = NC, VL = 5V *(Figure 4)* | 5 | 10 | 18 | ns |
| $t_{RZLC}$ | | Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 30 pF<br>RL1 = 390Ω, RL2 = 1.6k, VL = 5V *(Figure 4)* | 5 | 8 | 15 | ns |
| $t_{RHZC}$ | | Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V,<br>RL1 = 390Ω, RL2 = NC, CL = 5 pF *(Figure 4)* | 2 | 4 | 8 | ns |
| $t_{RZHC}$ | | Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V,<br>RL1 = NC, RL2 = 1.6k, CL = 30 pF *(Figure 4)* | 3 | 7 | 12 | ns |
| $t_{RLZT}$ | T/$\overline{R}$ to An | VCI = Bn, VC = 2V, RC = 18Ω,<br>CD = 0.8V, VL = 5V, RL1 = 390Ω,<br>RL2 = NC, CL = 5 pF *(Figure 5)* | 5 | 10 | 18 | ns |
| $t_{RZLT}$ | | VCI = Bn, VC = 2V, RC = 18Ω,<br>CD = 0.8V, VL = 5V, RL1 = 390Ω,<br>RL2 = 1.6k, CL = 30 pF *(Figure 5)* | 14 | 24 | 40 | ns |
| $t_{RHZT}$ | | VCI = Bn, VC = 0V, RC = 18Ω,<br>CD = 0.8V, VL = 0V, RL1 = 390Ω,<br>RL2 = NC, CL = 5 pF *(Figure 5)* | 2 | 4 | 8 | ns |
| $t_{RZHT}$ | | VCI = Bn, VC = 0V, RC = 18Ω,<br>CD = 0.8V, VL = 0V, RL1 = NC<br>RL2 = 1.6k, CL = 30 pF *(Figure 5)* | 2 | 8 | 15 | ns |
| $t_{NR}$ | Receiver Noise Rejection Pulse Width | *(Figure 6)* | 3 | 6 | | ns |

**Note:** NC means open

## DS3897 Switching Characteristics

**(0°C ≤ $T_A$ ≤ 70°C, 4.75V ≤ $V_{CC}$ ≤ 5.25V** unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Driver:** | | | | | | |
| $t_{DLH}$ | Dn, En to Bn | $\overline{TE}$ = 0.8V, $\overline{RE}$ = 2.0V, VL = 2V | 5 | 9 | 15 | ns |
| $t_{DHL}$ | | *(Figure 2)* | 5 | 9 | 15 | ns |
| $t_{DLHT}$ | $\overline{TE}$ to Bn | An = $\overline{RE}$ = 2.0V, VL = 2V, *(Figure 2)* | 5 | 10 | 18 | ns |
| $t_{DHLT}$ | | RL1 = 18Ω, RL2 = NC, VL = 2V *(Figure 5)* | 5 | 12 | 20 | ns |
| $t_R$ | Driver Output Rise Time | CD = 0.8V, T/$\overline{R}$ = 2V, VL = 2V | 3 | 6 | 10 | ns |
| tF | Driver Output Fall Time | *(Figure 2)* | 3 | 6 | 10 | ns |

## DS3897 Switching Characteristics (Continued)

**(0°C ≤ $T_A$ ≤ 70°C, 4.75V ≤ $V_{CC}$ ≤ 5.25V unless otherwise specified)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Receiver:** | | | | | | |
| $t_{RLH}$ | Bn to Rn | $\overline{TE}$ = 2.0V, $\overline{RE}$ = 0.8V (*Figure 3*) | 5 | 10 | 18 | ns |
| $t_{RHL}$ | | | 5 | 12 | 18 | ns |
| $t_{RLZR}$ | $\overline{RE}$ to Rn | Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 5 pF RL1 = 390Ω, RL2 = NC (*Figure 4*) | 5 | 10 | 18 | ns |
| $t_{RZLR}$ | | Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6k (*Figure 4*) | 5 | 8 | 15 | ns |
| $t_{RHZR}$ | | Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 4*) | 2 | 4 | 8 | ns |
| $t_{RZHR}$ | | Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = NC, RL2 = 1.6k, CL = 30 pF (*Figure 4*) | 3 | 7 | 12 | ns |
| $t_{NR}$ | Receiver Noise Rejection Pulse Width | (*Figure 6*) | 3 | 6 | | ns |
| **Driver plus Receiver:** | | | | | | |
| $t_{DRLH}$ | Dn to Rn | $\overline{TE}$ = $\overline{RE}$ = 0.8V (*Figure 7*) | 10 | 20 | 30 | ns |
| $t_{DRHL}$ | | | 10 | 20 | 30 | ns |

**Note:** NC means open

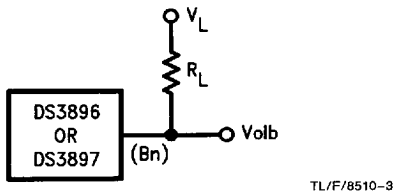


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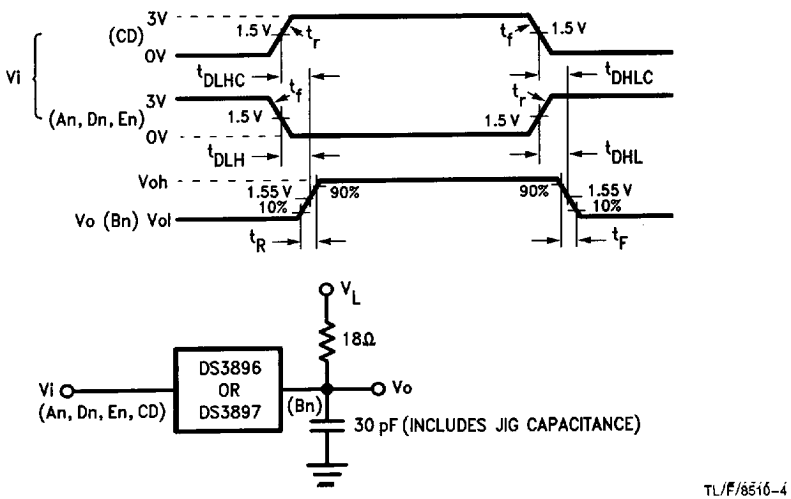
**FIGURE 1. Driver Output Low Voltage Test**

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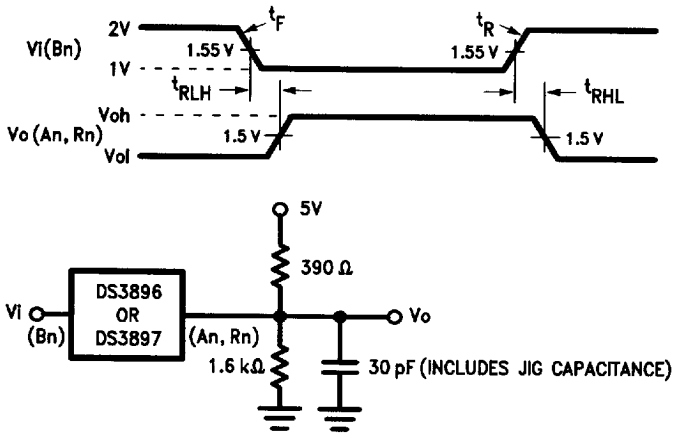
**Note:** $t_r = t_f \leq 5$ ns from 10% to 90%

**FIGURE 2. Driver Propagation Delays**

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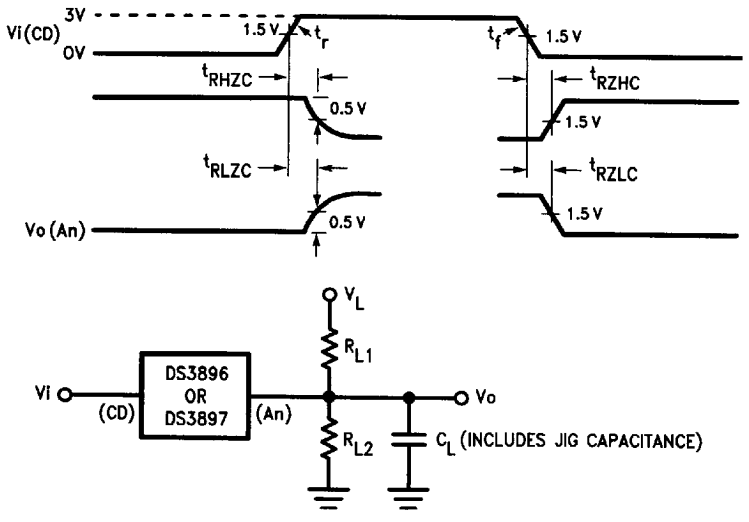
**Note:** $t_R = t_F \leq 10$ ns from 10% to 90%

**FIGURE 3. Receiver Propagation Delays**

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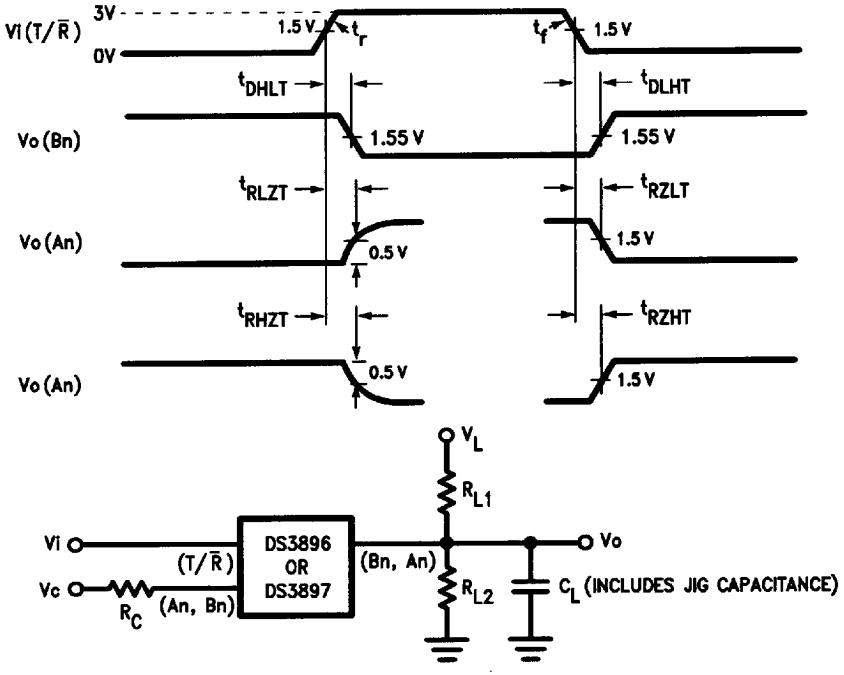
**Note:** $t_r = t_f \leq 5$ ns from 10% to 90%

**FIGURE 4. Propagation Delay from CD pin to An**

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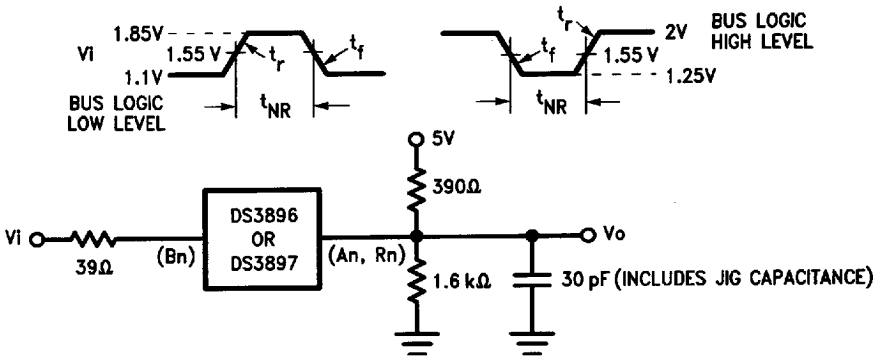
**Note:** $t_r = t_f \leq 5$ ns from 10% to 90%

**FIGURE 5. Propagation Delay from T/$\overline{R}$ pin to An or Bn**

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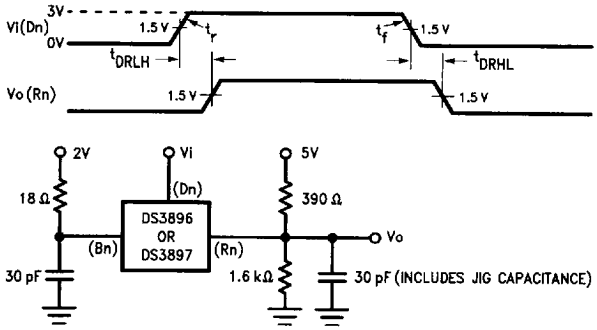
**Note:** $t_r = t_f = 2$ ns from 10% to 90%

***FIGURE 6. Receiver Noise Immunity: "No Response at Output" Input Waveforms***

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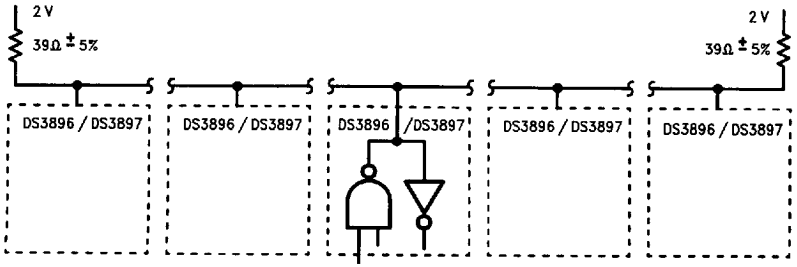
**Note:** $t_r = t_f \leq 5$ ns from 10% to 90%

**FIGURE 7. Driver Plus Receiver Delays**

## Typical Application

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