

# CD40106B Types

## CMOS Hex Schmitt Triggers

High-Voltage Types (20-Volt Rating)

■ CD40106B consists of six Schmitt-trigger circuits. Each circuit functions as an inverter with Schmitt-trigger action on the input. The trigger switches at different points for positive- and negative-going signals. The difference between the positive-going voltage ( $V_P$ ) and the negative-going voltage ( $V_N$ ) is defined as hysteresis voltage ( $V_H$ ) (see Fig.6). The CD40106B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- Schmitt-trigger action with no external components
- Hysteresis voltage (typ.) 0.9 V at  $V_{DD} = 5$  V, 2.3 V at  $V_{DD} = 10$  V, and 3.5 V at  $V_{DD} = 15$  V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Low  $V_{DD}$  to  $V_{SS}$  current during slow input ramp
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators

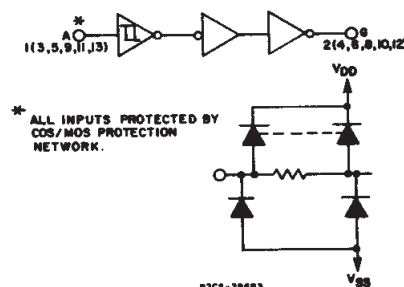
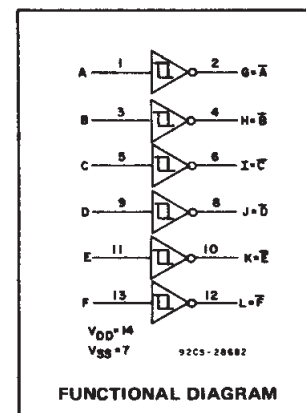


Fig.1 – Logic diagram  
(1 of 6 Schmitt triggers).

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD} + 0.5$  V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$  mA

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at 12mW/ $^\circ\text{C}$  to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+265^\circ\text{C}$

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ Full Package-Temperature Range)	3	18	V

### DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20$  ns,  $C_L = 50$  pF,  $R_L = 200$  k $\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V <sub>DD</sub> (V)	TYP.	MAX.	
Propagation Delay Time: t <sub>PHL</sub> t <sub>PLH</sub>		5 10 15	140 70 60	280 140 120	ns
Transition Time: t <sub>THL</sub> t <sub>TLH</sub>		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C <sub>IN</sub>	Any Input		5	7.5	pF

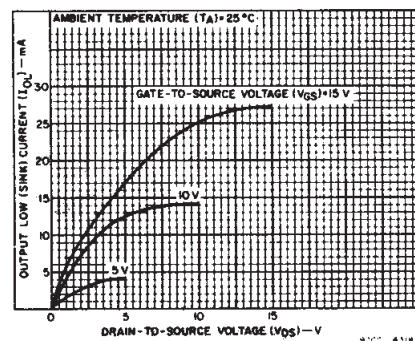


Fig.2 – Typical output low (sink)  
current characteristics.

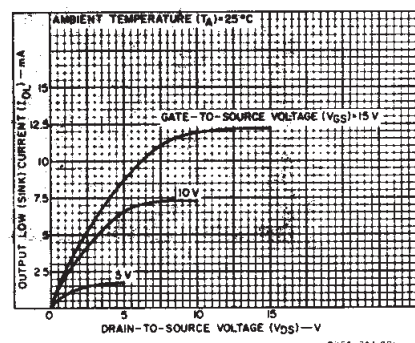


Fig.3 – Minimum output low (sink)  
current characteristics.

# CD40106B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA	
	—	0,10	10	2	2	60	60	—	0.02	2		
	—	0,15	15	4	4	120	120	—	0.02	4		
	—	0,20	20	20	20	600	600	—	0.04	20		
Positive Trigger Threshold Voltage V <sub>P</sub> Min.	—	—	5	2.2	2.2	2.2	2.2	2.2	2.9	—	V	
	—	—	10	4.6	4.6	4.6	4.6	4.6	5.9	—		
	—	—	15	6.8	6.8	6.8	6.8	6.8	8.8	—		
V <sub>P</sub> Max.	—	—	5	3.6	3.6	3.6	3.6	—	2.9	3.6	V	
	—	—	10	7.1	7.1	7.1	7.1	—	5.9	7.1		
	—	—	15	10.8	10.8	10.8	10.8	—	8.8	10.8		
Negative Trigger Threshold Voltage V <sub>N</sub> Min.	—	—	5	0.9	0.9	0.9	0.9	0.9	1.9	—	V	
	—	—	10	2.5	2.5	2.5	2.5	2.5	3.9	—		
	—	—	15	4	4	4	4	4	5.8	—		
V <sub>N</sub> Max.	—	—	5	2.8	2.8	2.8	2.8	—	1.9	2.8	V	
	—	—	10	5.2	5.2	5.2	5.2	—	3.9	5.2		
	—	—	15	7.4	7.4	7.4	7.4	—	5.8	7.4		
Hysteresis Voltage V <sub>H</sub> Min.	—	—	5	0.3	0.3	0.3	0.3	0.3	0.9	—	V	
	—	—	10	1.2	1.2	1.2	1.2	1.2	2.3	—		
	—	—	15	1.6	1.6	1.6	1.6	1.6	3.5	—		
V <sub>H</sub> Max.	—	—	5	1.6	1.6	1.6	1.6	—	0.9	1.6	V	
	—	—	10	3.4	3.4	3.4	3.4	—	2.3	3.4		
	—	—	15	5	5	5	5	—	3.5	5		
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—		
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage Low-Level, V <sub>OL</sub> Max.	—	5	5	0.05				—	0	0.05	V	
	—	10	10	0.05				—	0	0.05		
	—	15	15	0.05				—	0	0.05		
Output Voltage High Level, V <sub>OH</sub> Min.	—	0	5	4.95				4.95	5	—	V	
	—	0	10	9.95				9.95	10	—		
	—	0	15	14.95				14.95	15	—		
Input Current, I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA	

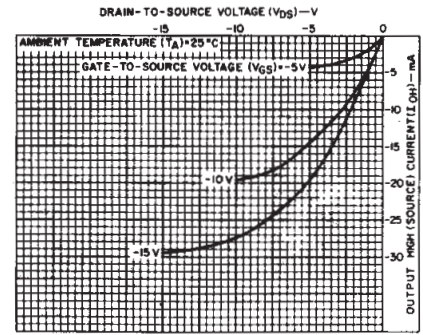


Fig. 4 - Typical output high (source) current characteristics.

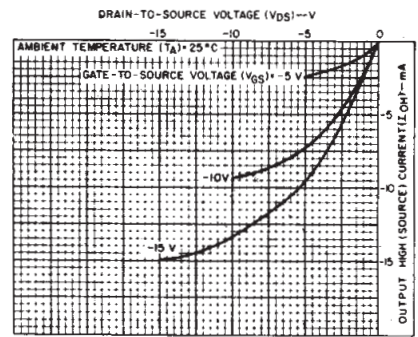


Fig. 5 - Minimum output high (source) current characteristics.

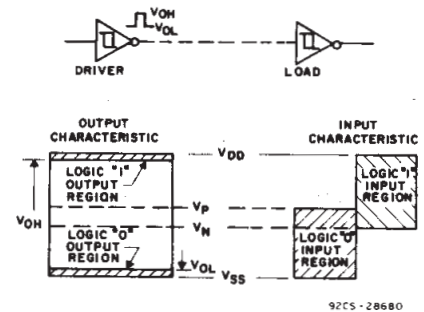


Fig. 7 - Input and output characteristics.

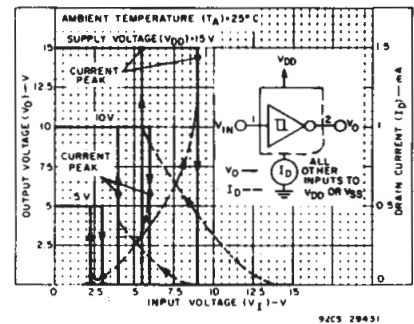
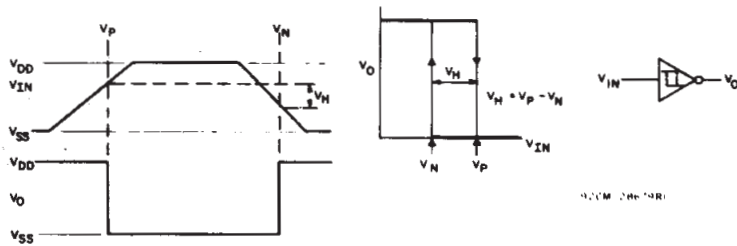


Fig. 8 - Typical current and voltage transfer characteristics.



a) Definition of  $V_P$ ,  $V_N$ ,  $V_H$

b) Transfer characteristics of 1 of 6 gates

Fig. 6 - Hysteresis definition, characteristics, and test set-up.

## CD40106B Types

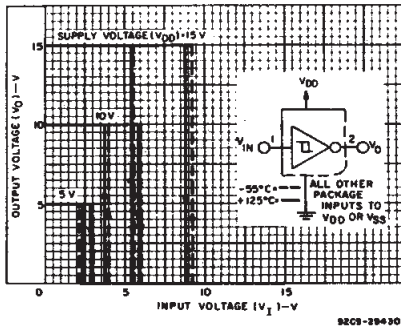


Fig. 9 - Typical voltage transfer characteristics as a function of temperature.

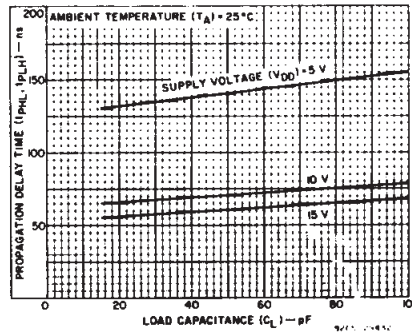


Fig. 10 - Typical propagation delay time as a function of load capacitance.

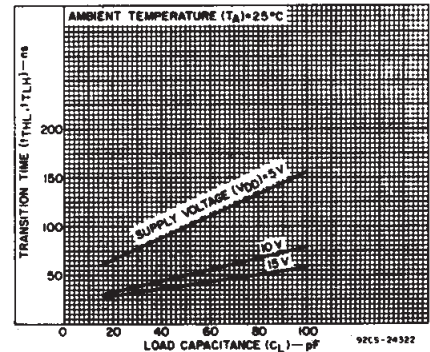


Fig. 11 - Typical transition time as a function of load capacitance.

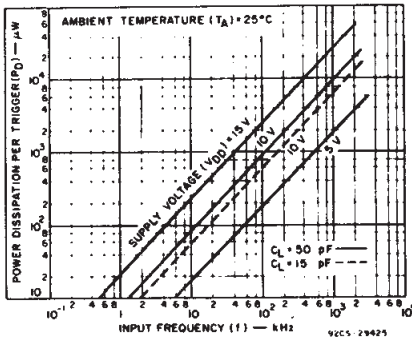


Fig. 12 - Typical power dissipation per trigger as a function of input frequency.

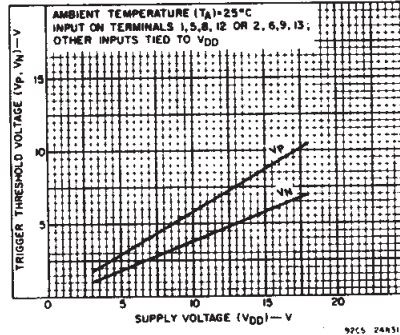


Fig. 13 - Typical trigger threshold voltage as a function of supply voltage.

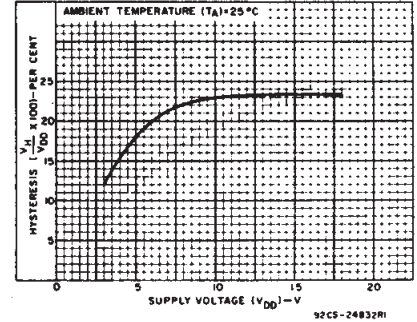


Fig. 14 - Typical per cent hysteresis as a function of supply voltage.

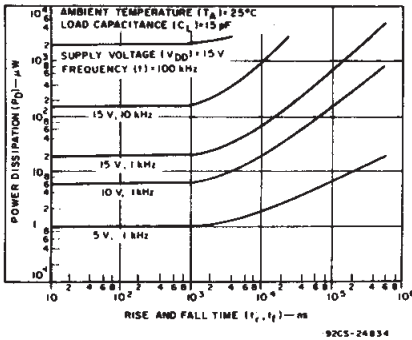


Fig. 15 - Typical power dissipation as a function of rise and fall times.

### APPLICATIONS



Fig. 16 - Wave shaper.

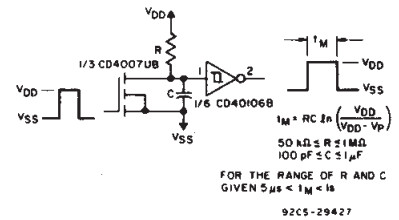


Fig. 17 - Monostable multivibrator.

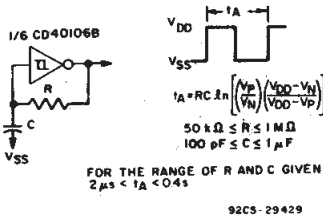


Fig. 18 - Astable multivibrator.

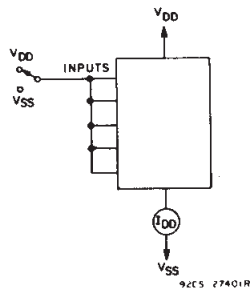


Fig. 19 - Quiescent device current test circuit.

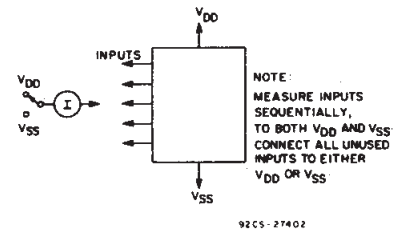


Fig. 20 - Input current test circuit.

## CD40106B Types

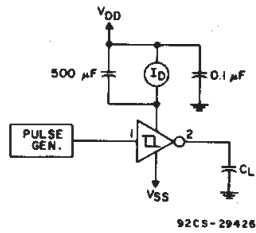
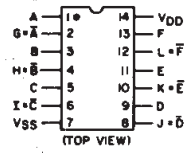
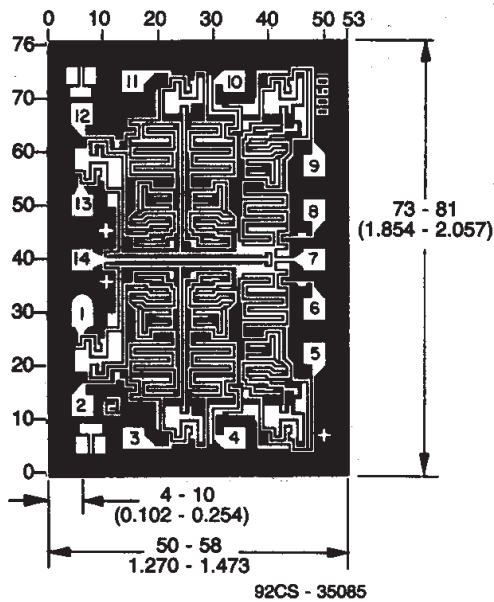


Fig.21 — Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD40106BH

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40106BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40106BE	<a href="#">Samples</a>
CD40106BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40106BE	<a href="#">Samples</a>
CD40106BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40106BF	<a href="#">Samples</a>
CD40106BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40106BF3A	<a href="#">Samples</a>
CD40106BK	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI			
CD40106BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	<a href="#">Samples</a>
CD40106BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	<a href="#">Samples</a>
CD40106BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	<a href="#">Samples</a>
CD40106BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	<a href="#">Samples</a>
CD40106BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	<a href="#">Samples</a>
CD40106BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	<a href="#">Samples</a>
CD40106BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	<a href="#">Samples</a>
CD40106BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106B	<a href="#">Samples</a>
CD40106BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106B	<a href="#">Samples</a>
CD40106BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0106B	<a href="#">Samples</a>
CD40106BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0106B	<a href="#">Samples</a>
CD40106BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0106B	<a href="#">Samples</a>
CD40106BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0106B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40106BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0106B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD40106B, CD40106B-MIL :**

- Catalog: [CD40106B](#)
- Military: [CD40106B-MIL](#)

NOTE: Qualified Version Definitions:

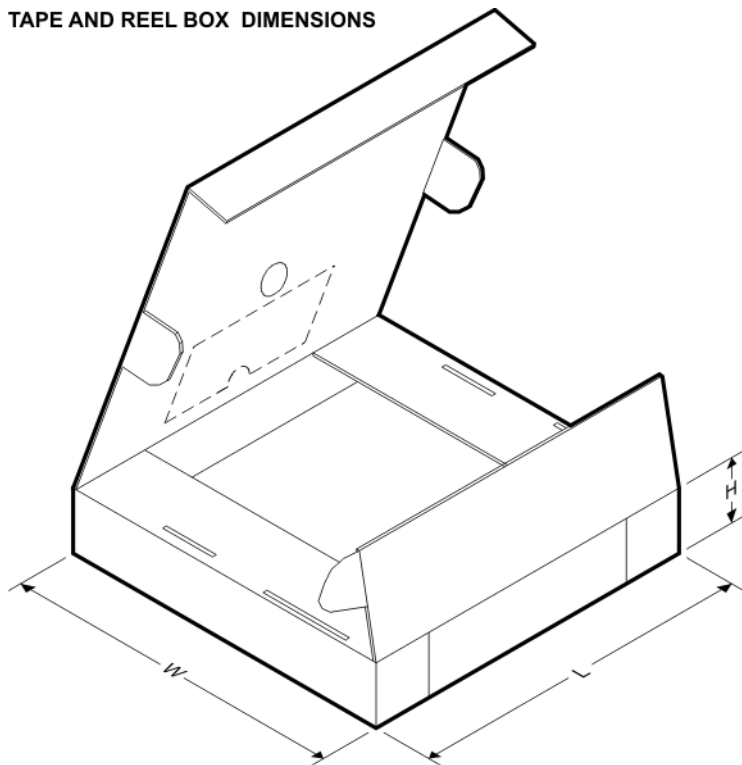
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40106BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40106BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



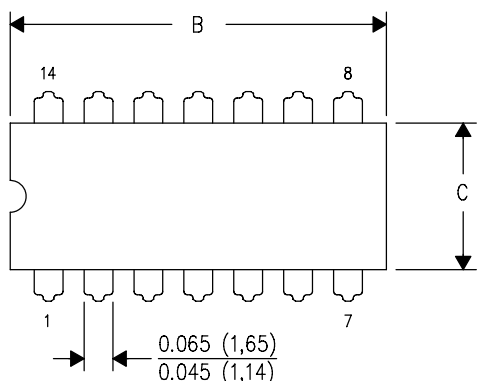
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40106BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD40106BM96G4	SOIC	D	14	2500	367.0	367.0	38.0
CD40106BMT	SOIC	D	14	250	367.0	367.0	38.0
CD40106BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD40106BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



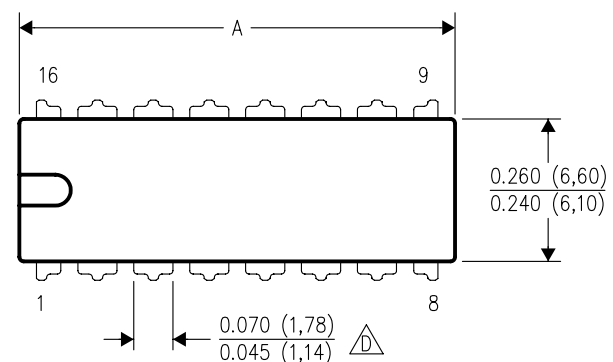
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

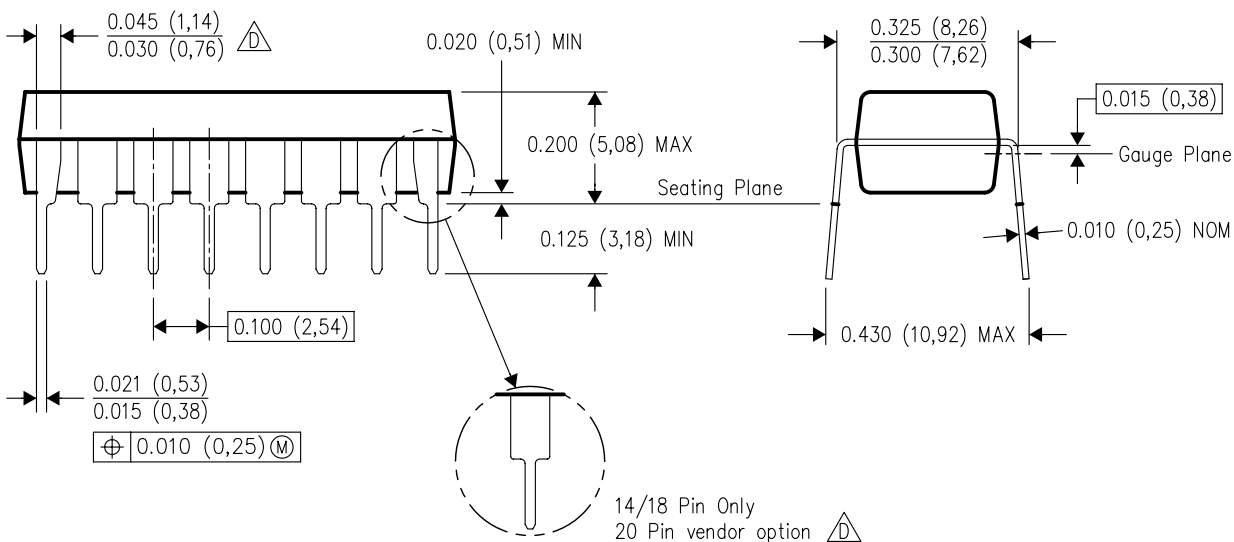
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



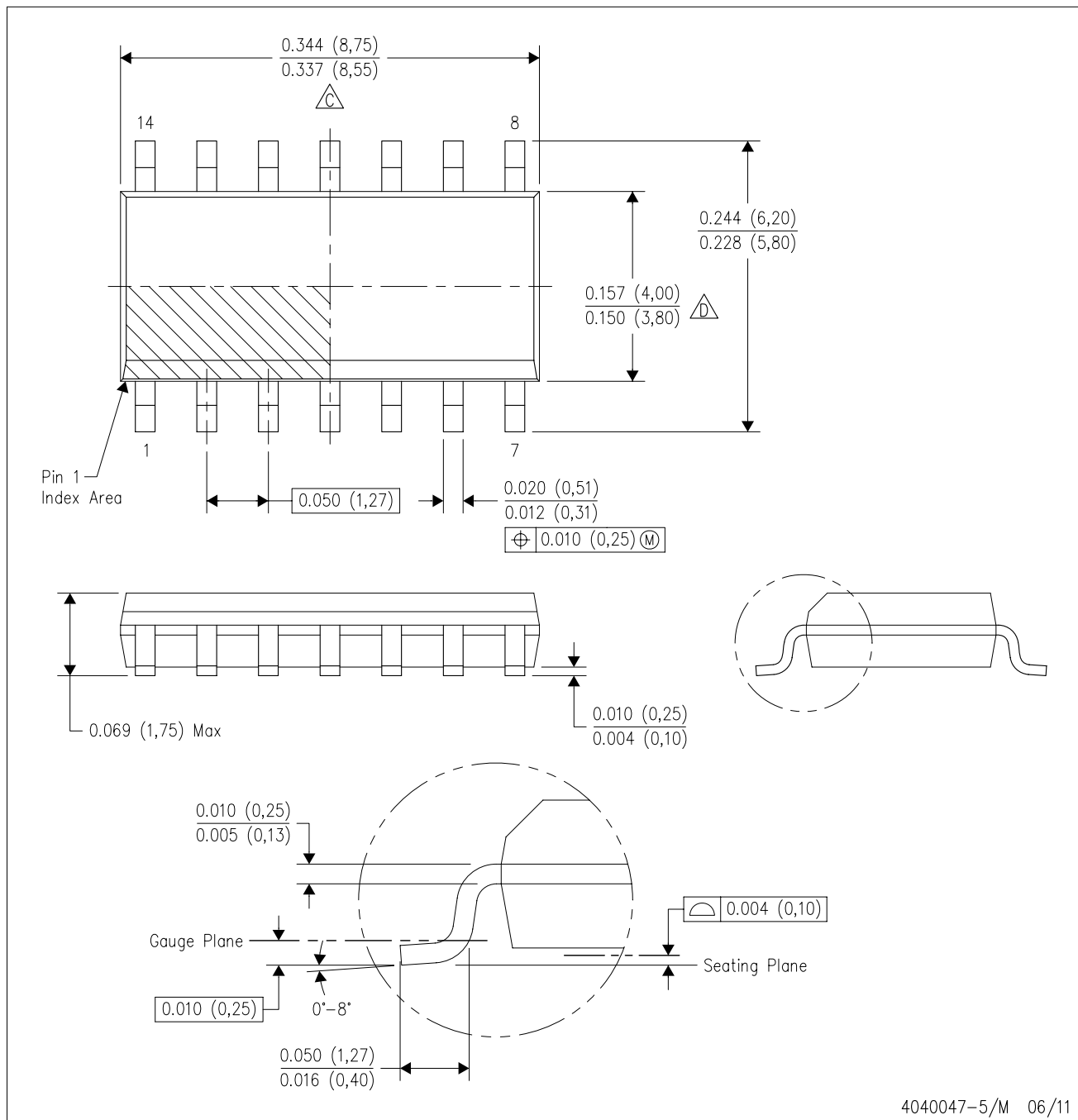
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

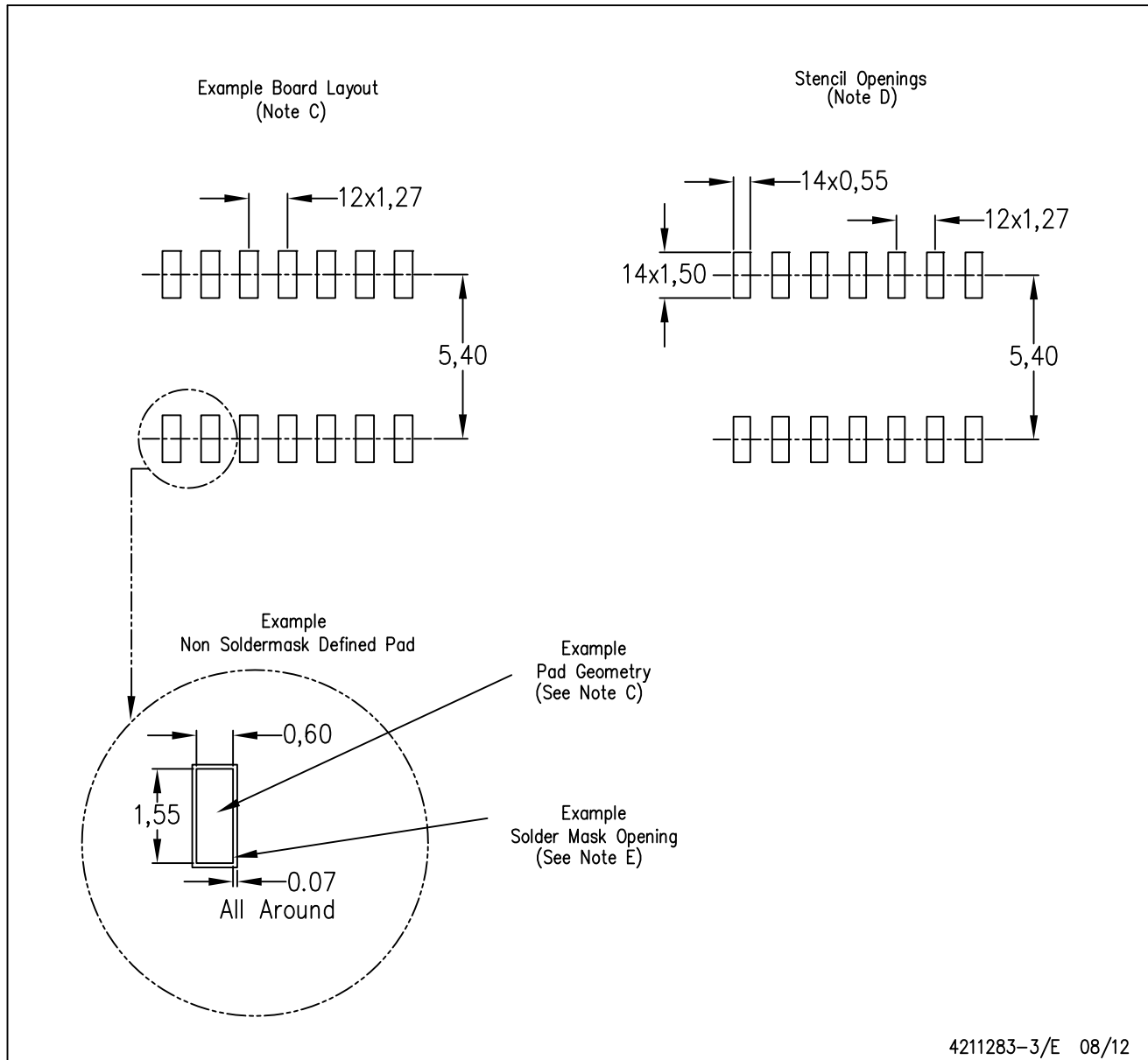
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

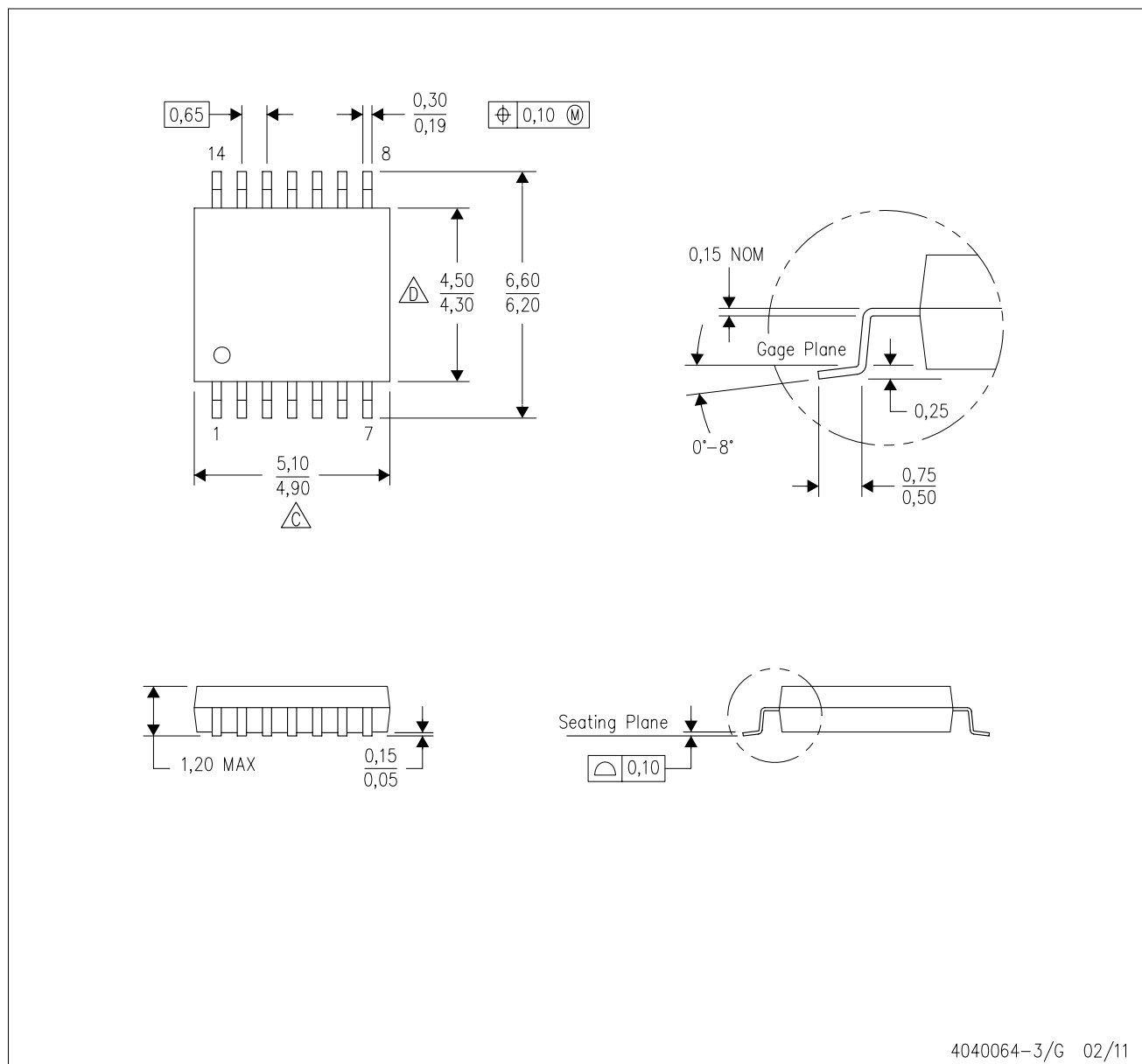
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

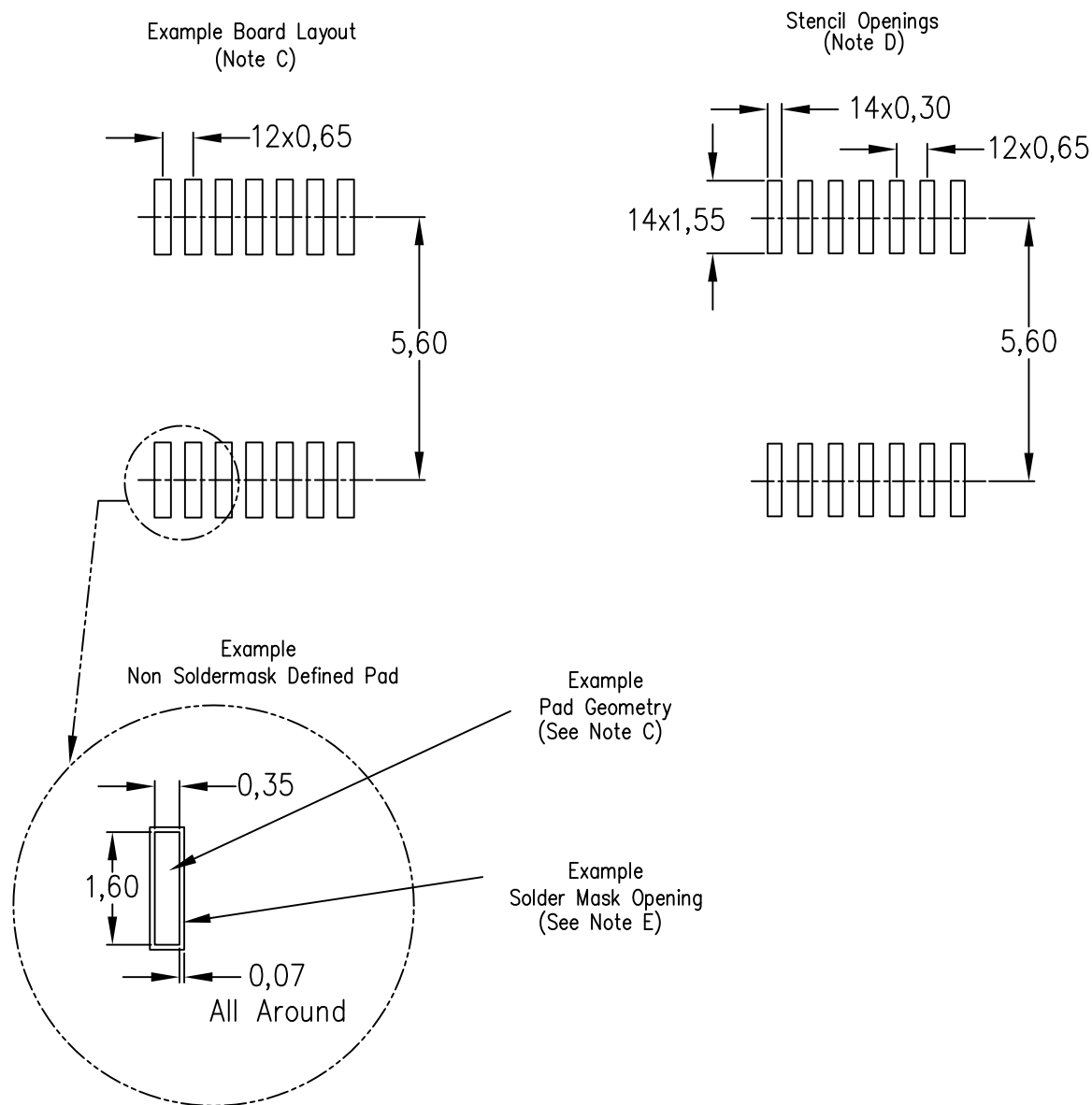
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

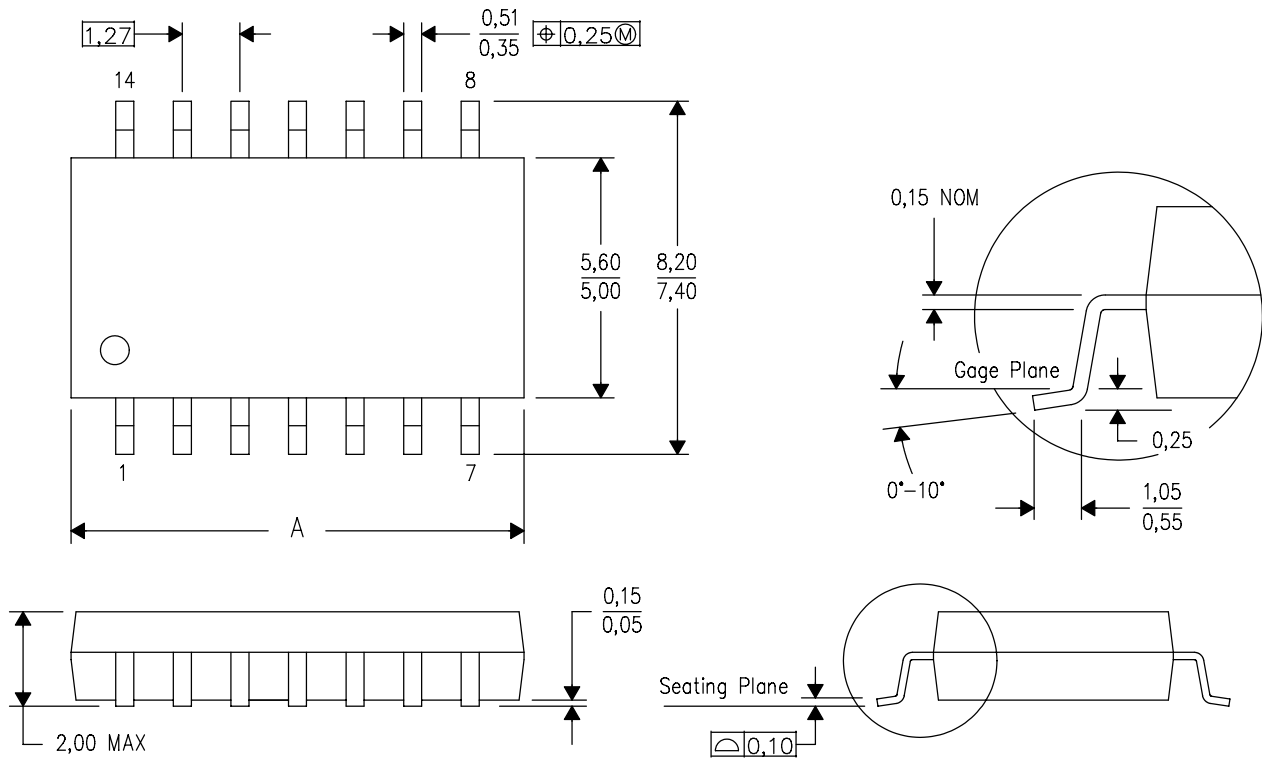
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.