

NEW PRODUCT

T-46-07-05

MITSUBISHI ALSTTLs

M74ALS374P

OCTAL D-TYPE EDGE-TRIGGERED FLIP FLOP
WITH 3-STATE OUTPUT (NONINVERTED)

6249827 MITSUBISHI (DGT L LOGIC)

91D 12525 D

DESCRIPTION

The M74ALS374P is a semiconductor integrated circuit consisting of eight D-type positive edge-triggered flip-flop circuits with 3-state noninverted output and is provided with an output control and a clock input, both common to all circuits.

FEATURES

- Positive edge triggering
- 3-state, high fan-out ($I_{OL} = 24\text{mA}$, $I_{OH} = -2.6\text{mA}$)
- High package density with eight circuits in one package
- Output control and clock inputs common to all eight circuits
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

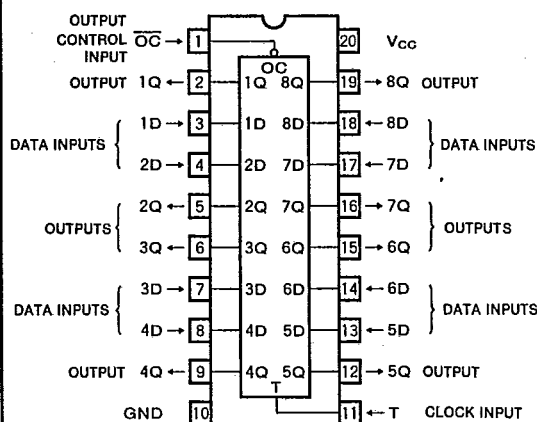
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

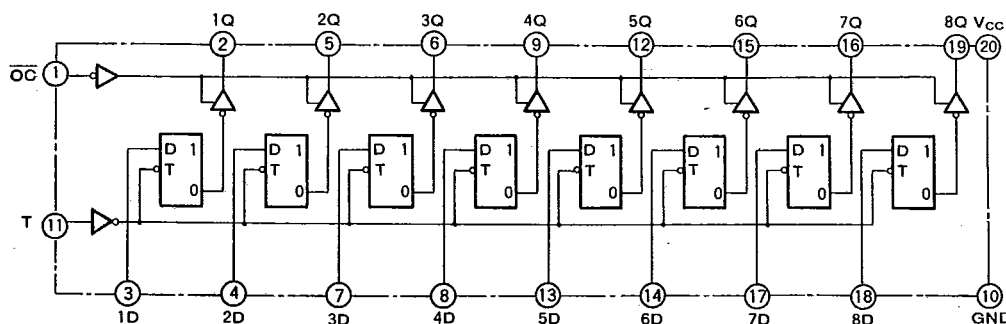
The eight D-type edge-triggered flip-flop circuits have the common output control $\overline{OC}$ and clock input T. When T changes from low to high, the status of D immediately before the change appears the output Q in accordance with the function table.

While $\overline{OC}$ is high, 1Q~8Q are in the high-impedance state "Z" irrespective of other inputs. $\overline{OC}$ does not affect the internal operation of the flip-flops. While Q is "Z", old data can be retained or new data can be entered. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bidirectional bus driver.

PIN CONFIGURATION (TOP VIEW)



LOGIC DIAGRAM



6249827 MITSUBISHI (DGTL LOGIC)

91D 12526 D

OCTAL D-TYPE EDGE-TRIGGERED FLIP FLOP
WITH 3-STATE OUTPUT(NONINVERTED)

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FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OC}^*$	T	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q^0
H	X	X	Z

Note 1. ↑ : Transition from low to high level (positive edge trigger)

 Q^0 : Level of Q before the indicated input conditions were established

Z : High impedance state

X : Irrelevant

* : Data can be stored irrespective of $\overline{OC}$

ABSOLUTE MAXIMUM RATINGS ($T_A = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5~+7	V
V_I	Input voltage		-0.5~+7	V
V_O	Output voltage	High-level state or high-impedance state	-0.5~+5.5	V
T_{opr}	Operating free-air ambient temperature range		-20~+75	$^\circ\text{C}$
T_{stg}	Storage temperature range		-65~+150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		-2.6	mA
I_{OL}	Low-level output current	0		24	mA
T_{opr}	Operating free-air ambient temperature range	-20		+75	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IC}	Input clamp voltage	$V_{CC}=4.5\text{V}, I_{IC}=-18\text{mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC}=4.5\sim 5.5\text{V}, I_{OH}=-0.4\text{mA}$	$V_{CC}-2$			V
		$V_{CC}=4.5\text{V}, I_{OH}=-2.6\text{mA}$	2.4	3.2		
V_{OL}	Low-level output voltage	$V_{CC}=4.5\text{V}, I_{OL}=12\text{mA}$		0.25	0.4	V
		$I_{OL}=24\text{mA}$		0.35	0.5	
I_{OZH}	Off-state high-level output current	$V_{CC}=5.5\text{V}, V_O=2.7\text{V}$			20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.5\text{V}, V_O=0.4\text{V}$			-20	μA
I_I	Input current at maximum voltage	$V_{CC}=5.5\text{V}, V_I=7\text{V}$			0.1	mA
I_{IH}	High-level input current	$V_{CC}=5.5\text{V}, V_I=2.7\text{V}$			20	μA
I_{IL}	Low-level input current	$V_{CC}=5.5\text{V}, V_I=0.4\text{V}$			-0.2	mA
I_O	Output current	$V_{CC}=5.5\text{V}, V_O=2.25\text{V}$	-30		-112	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.5\text{V}$		11	19	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.5\text{V}$		19	28	mA
I_{CCZ}	Supply current, all outputs disabled	$V_{CC}=5.5\text{V}$		20	31	mA

* : All typical values are at $V_{CC}=5\text{V}, T_A=25^\circ\text{C}$.

OCTAL D-TYPE EDGE-TRIGGERED FLIP FLOP WITH 3-STATE OUTPUT (NONINVERTED)

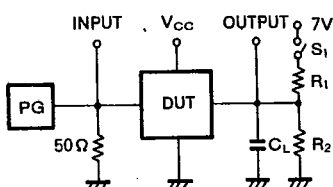
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SWITCHING CHARACTERISTICS

Symbol	Parameter	Test conditions/Limits (Note 2)									Unit
		Input	Outputs	V _{CC} =5V	V _{CC} =4.5~5.5V						
				C _L =15pF	C _L =50pF						
				R ₁ =R ₂ =500Ω	R ₁ =R ₂ =500Ω						
				T _a =25°C	T _a =0~70°C			T _a =-20~+75°C			
				Typ	Min	Typ *	Max	Min	Typ *	Max	
f _{max}	Maximum clock frequency	T	1Q~8Q		35	60		33	60		MHz
t _{PLH}	Propagation time	T	1Q~8Q	5.5	3	7.5	12	3	7.5	13	ns
t _{PHL}				8.5	5	10	16	5	10	17	
t _{PZH}	Output enable time	$\overline{OC}$	1Q~8Q	7	5	8	17	5	8	18	ns
t _{PZL}				8	7	10	18	7	10	19	
t _{PHZ}	Output disable time	$\overline{OC}$	1Q~8Q	3	2	5	10	2	5	11	ns
t _{PLZ}				4	3	4.5	18	3	4.5	19	

* : All typical values are at V_{CC}=5V, T_a=25°C.

Note 2. Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

PRR ≤ 1MHz

t_r=2ns, t_f=2ns

V_{IH}=3.5V, V_{IL}=0.3V

duty cycle=50%

Z_O=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S ₁
t _{PLH}	Open
t _{PHL}	Open
t _{PZH}	Open
t _{PZL}	Closed
t _{PHZ}	Open
t _{PLZ}	Closed

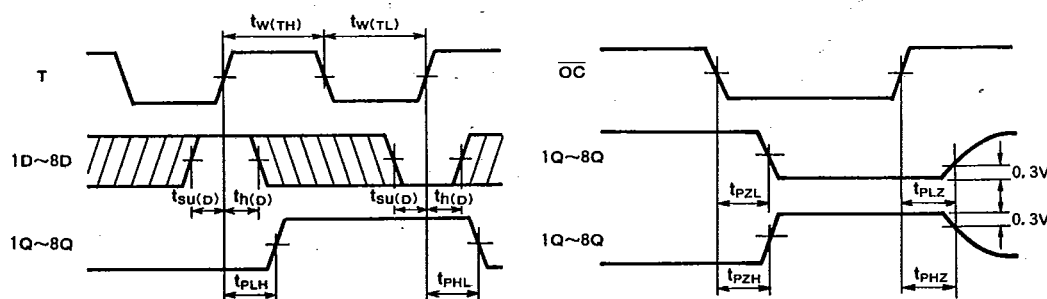
TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R₂=500Ω)

Symbol	Parameter		Limits						Unit
			T _a =0~70℃			T _a =-20~+75℃			
			Min	Typ *	Max	Min	Typ *	Max	
t _{W(TH)}	Pulse width	T "H"	14	4		15	4		ns
t _{W(TL)}		T "L"	14	8		15	8		
t _{SU(D)}	Setup time before T _t	1D~8D	10	4		11	4		ns
t _{H(D)}	Hold time after T _t	1D~8D	0	-2		1	-2		ns

* : All typical values are at V_{CC}=5V, T_a=25°C.

† : Transition from low to high (positive edge trigger)

TIMING DIAGRAM (Reference level = 1.3V)



Note 3. The shaded areas indicate the period when the Input is permitted to change for predictable output performance.

PACKAGE OUTLINES

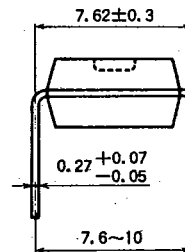
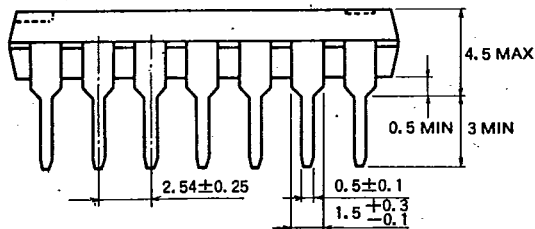
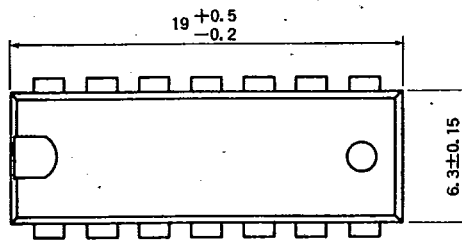
MITSUBISHI {DGTL LOGIC}

91D 12323

D T-9020

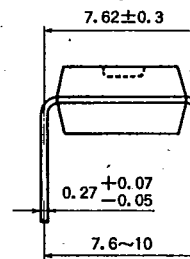
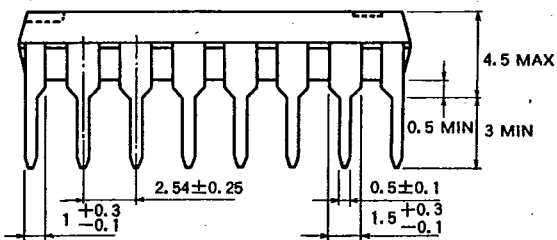
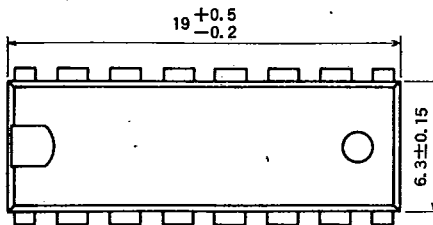
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



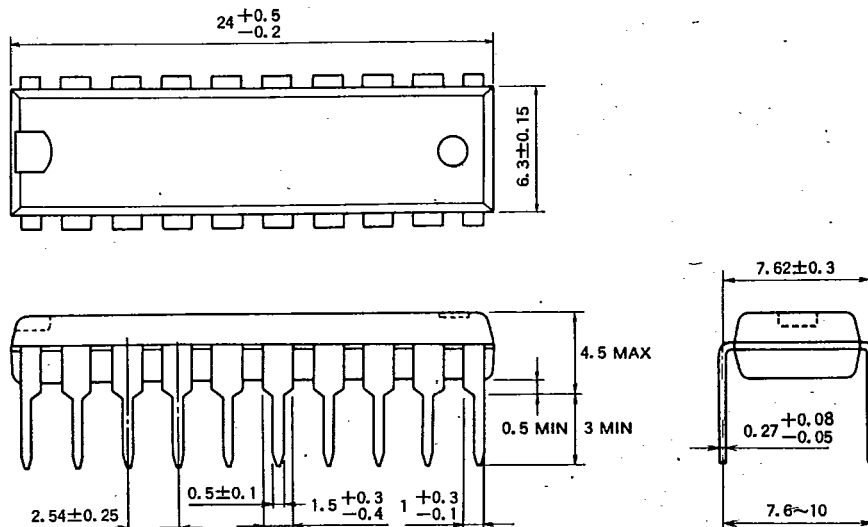
PACKAGE OUTLINES

91D 12324 D *T-90-20*

6249827 MITSUBISHI (DGTL LOGIC)

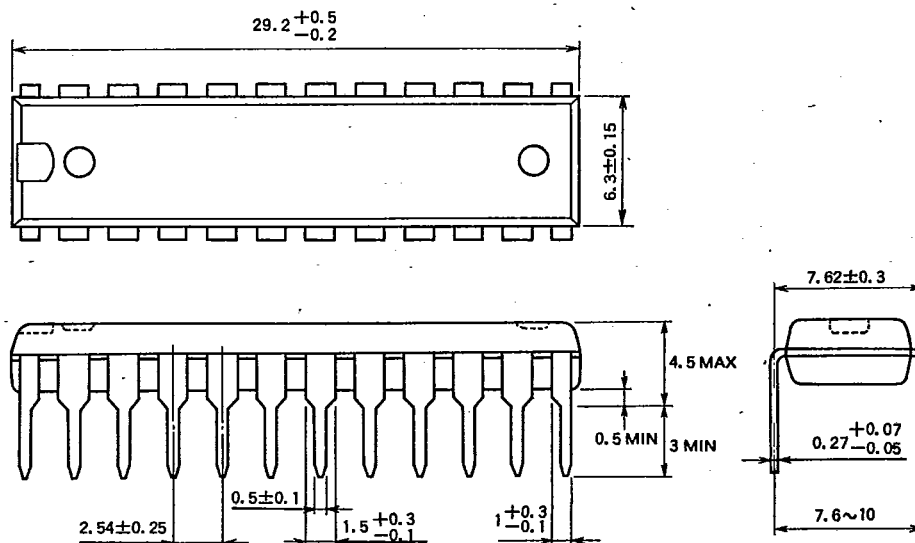
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE DESIGNATION TABLE

MITSUBISHI (DGTL LOGIC)

91D D

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T-90-20

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	*	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	*	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	*	Hex Inverter	14P2P
M74ALS05ADP	**	Hex Inverter with Open Collector Output	14P2P
M74ALS08DP	*	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	**	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	*	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	*	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	**	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	**	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	**	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	*	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	**	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	**	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	*	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	**	Dual J-K Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	*	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	**	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	*	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	**	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	**	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	**	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	**	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	*	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	**	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	**	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	*	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	*	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	**	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	**	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	**	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	**	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	**	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	**	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	**	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	**	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	**	Hex Noninverting Buffer	14P2P

*: New product **: Under development

6249827 MITSUBISHI (DGTL LOGIC)

91D 12785 D

MITSUBISHI ALSTTLs

DESCRIPTION

MITSUBISHI (DGTL LOGIC)

91D D

6249827 0012785 9 MIT3

T-90-20

DESCRIPTION

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

MITSUBISHI ALSTTLs
PACKAGE OUTLINES

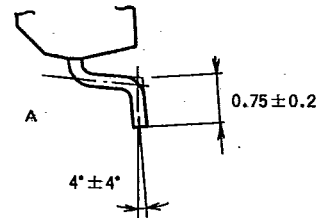
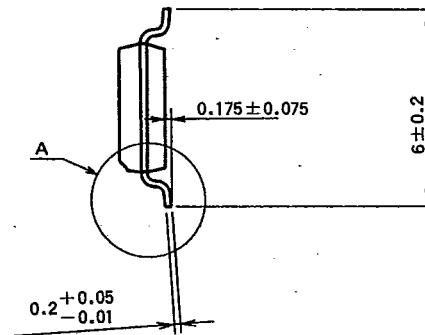
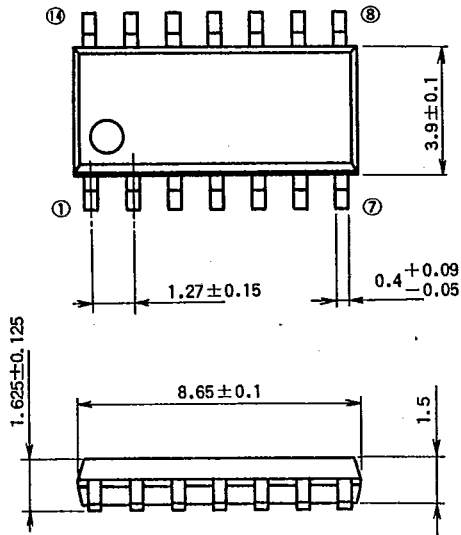
MITSUBISHI (DGTL LOGIC)

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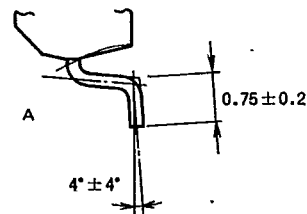
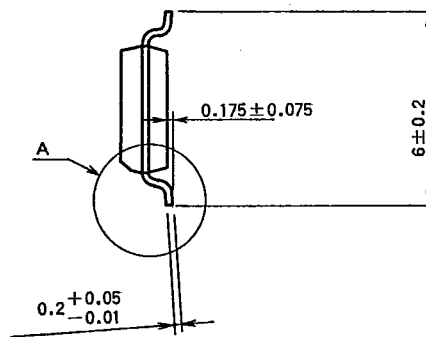
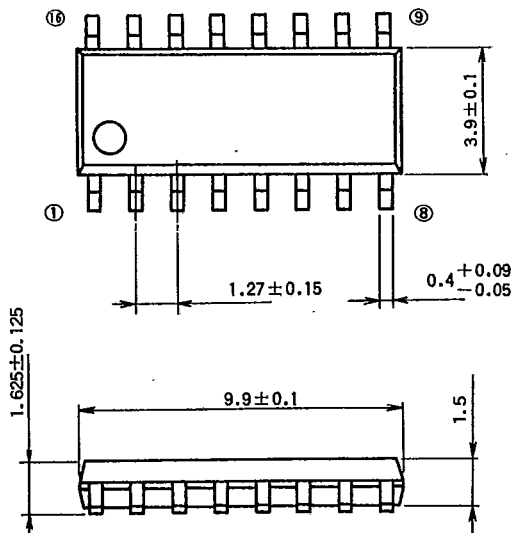
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



MITSUBISHI ALSTTLs
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC)

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