8- Bit Latches, 8-Bit Registers

SN54LS373 SN54S373
SN54LS374 SN54S374

Features/Benefits

- **Three-state outputs drive bus lines**
- **8-bit data path matches byte boundaries**
- **Hysteresis improves noise margin**
- **Low current PNP inputs reduce loading**
- **Ideal for microprocessor interface**

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS373	J,L,W	Mil	Non-invert	Latch	LS
SN54LS374				Register	
SN54S373				Latch	S
SN54S374				Register	

Description

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

Function Tables

'373 8-Bit Latch

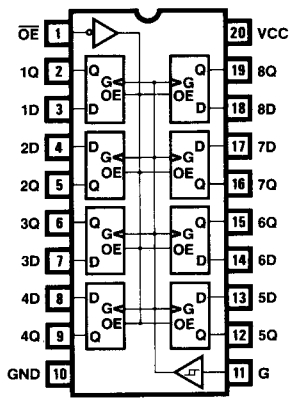
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'374 8-Bit Register

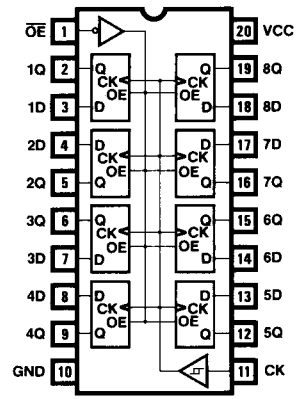
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'373 8-Bit Latch



'374 8-Bit Register



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		-55		125	°C
t_w	Width of Clock/Gate	High	15			ns
		Low	15			
t_{su}	Setup time	'LS373	5↓			ns
		'LS374	20↑			
t_h	Hold time	'LS373	20↓			ns
		'LS374	0↑			

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage					0.7	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			-0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7 V			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -1 mA	2.4	3.4		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-20	μA
I_{OZH}			V_O = 2.7 V			20	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		-30		-130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	'LS373		24	40	mA
			'LS374		27	40	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 667 Ω				35	50		MHz
t_{PLH}	Data to output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/Gate to output delay			20	30		15	28	ns
t_{PHL}				18	30		19	28	ns
t_{PZL}	Output enable delay			25	36		21	28	ns
t_{PZH}				15	28		20	28	ns
t_{PLZ}	Output disable delay	C_L = 5 pF R_L = 667 Ω		15	25		14	25	ns
t_{PHZ}				12	20		12	20	ns

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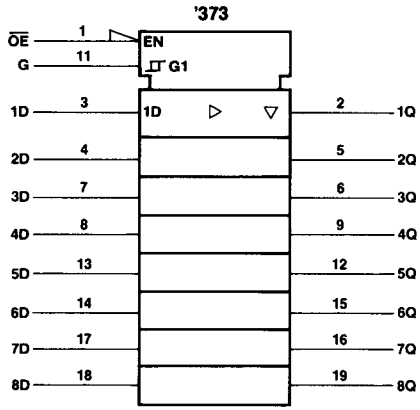
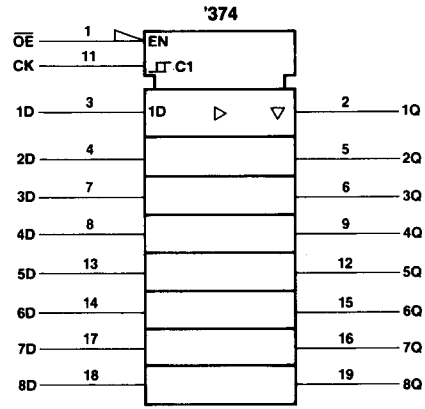
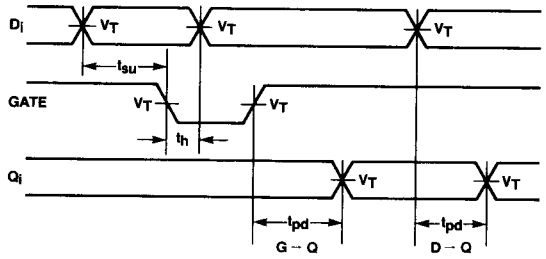
IEEE Symbols

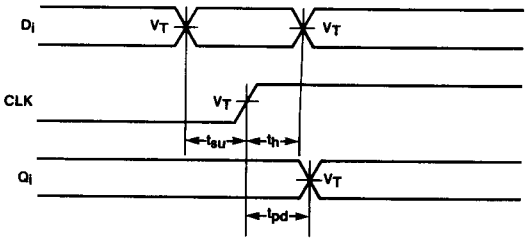




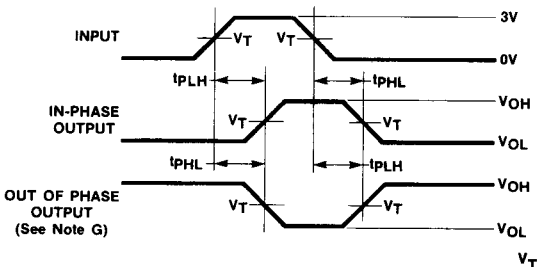
'373 Timing Diagrams



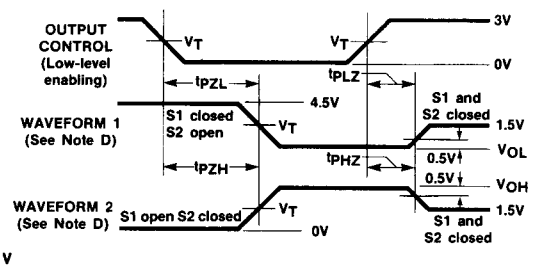
'374 Timing Diagrams



Test Waveforms



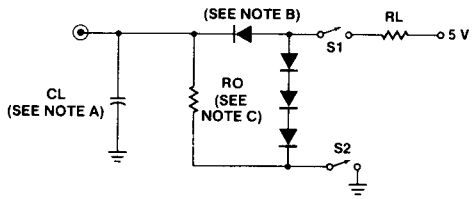
Propagation Delay



Enable and Disable

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series 54S, R_O = 1 K, V_T = 1.5 V.
For Series 54LS, R_O = 5 K, V_T = 1.3 V.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and:
For series 54S, t_R ≤ 2.5 ns, t_F ≤ 2.5 ns.
For Series 54LS and PAL devices, t_R ≤ 15 ns, t_F ≤ 6 ns.
G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

Standard Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		-55		125	°C
t_w	Width of Clock/Gate	High	6			ns
		Low	7.3			
t_{su}	Setup time	'S373	0↓			ns
		'S374	5↑			
t_h	Hold time	'S373	10↓			ns
		'S374	2↑			

↑↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 20 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = -2 mA	2.4	3.4		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.5 V			-50	μA
I_{OZH}			V_O = 2.4 V			50	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	'S373		105	160	mA
			'S374		90	140	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S373 MIN	'S373 TYP	'S373 MAX	'S374 MIN	'S374 TYP	'S374 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 15 pF R_L = 280 Ω				75	100		MHz
t_{PLH}	Data to output delay			7	12				ns
t_{PHL}				7	12				ns
t_{PLH}	Clock/Gate to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns