# M74ALS109AP



## DUAL J-$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

T-46-07-07

### DESCRIPTION

The M74ALS109AP is a semiconductor integrated circuit consisting of two J-$\overline{K}$ positive edge-triggered flip-flop circuits. Each of the circuits has independent inputs J, $\overline{K}$, clock T, direct set $\overline{S_D}$ and direct reset $\overline{R_D}$.

### FEATURES

- Positive edge-triggering
- Independent inputs and outputs for each flip-flop
- Direct set and reset inputs
- J and $\overline{K}$ inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

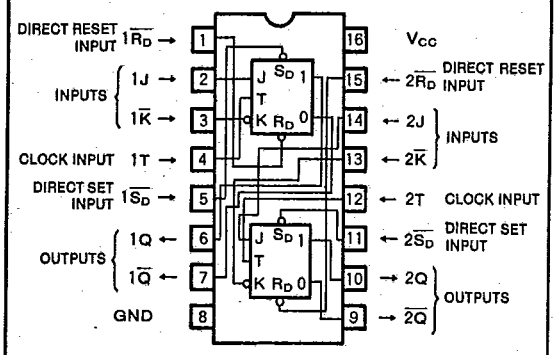
### APPLICATION

General purpose, for use in industrial and consumer digital equipment.

### FUNCTIONAL DESCRIPTION

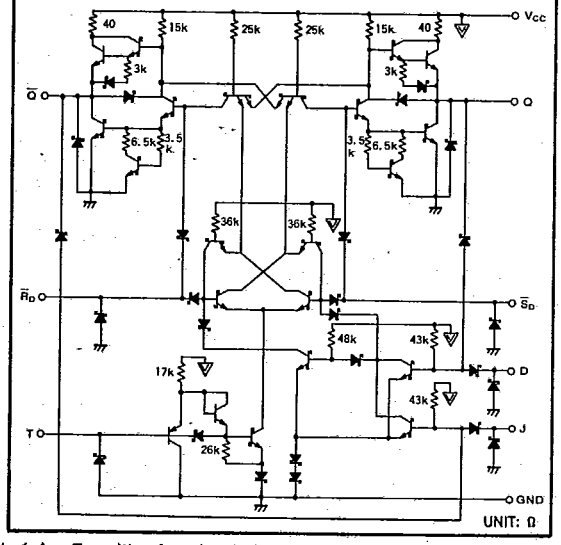
When T changes from low-level to high-level, the signals applied just before the change on J and $\overline{K}$ appear at Q and $\overline{Q}$ outputs in accordance with the function table. Use of $\overline{S_D}$ and $\overline{R_D}$ allows direct R-S flip-flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are high-level. But if $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously from this condition, the state of Q and $\overline{Q}$ cannot be predicted. When used as a J-$\overline{K}$ flip-flop, $\overline{S_D}$ and $\overline{R_D}$ should be held at high-level. D-type flip-flop operation is possible by connecting J and $\overline{K}$.

### PIN CONFIGURATION (TOP VIEW)




Outline 16P4

### CIRCUIT SCHEMATIC (EACH FLIP-FLOP)




### FUNCTION TABLE (Note 1)

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{S_D}$ | $\overline{R_D}$ | T | J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | L | X | X | $Q^0$ | $\overline{Q}^0$ |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | $Q^0$ | $\overline{Q}^0$ |
| H | H | ↑ | H | H | H | L |

Note 1 ↑ : Transition from low to high level (positive edge trigger)

$Q^0$ : Level of Q before the indicated steady-state input conditions were established.

$\overline{Q}^0$ : Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Toggle : Complement of previous state appears on each output with ↑ transition.

X : Irrelevant

* : When $\overline{S_D}$ or $\overline{R_D}$ is near $V_{IL\ MAX}$ in this condition, the level of $V_{OH}$ is not guaranteed. Moreover, if $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level from this condition then the state of Q and $\overline{Q}$ cannot be predicted.

### ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5~+7 | V |
| $V_I$ | Input voltage | | −0.5~+7 | V |
| $V_O$ | Output voltage | High-level state | −0.5~$V_{CC}$ | V |
| $T_{opr}$ | Operating free-air ambient temperature range | | −20~+75 | °C |
| $T_{stg}$ | Storage temperature range | | −65~+150 | °C |



MITSUBISHI ELECTRIC

# DUAL J-$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | 0 | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | 0 | | 8 | mA |
| $T_{opr}$ | Operating free-air ambient temperature range | −20 | | +75 | °C |

## ELECTRICAL CHARACTERISTICS ($T_a$ = −20 ~ +75°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ* | Max | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.5V, $I_{IC}$=−18mA | | | | −1.2 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$=4.5~5.5V, $I_{OH}$=−0.4mA | | $V_{CC}$−2 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$=4.5V | $I_{OL}$=4mA | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$=8mA | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum voltage | J, $\overline{K}$, T | $V_{CC}$=5.5V, $V_I$=7V | | | | 0.1 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 0.2 | |
| $I_{IH}$ | High-level input current | J, $\overline{K}$, T | $V_{CC}$=5.5V, $V_I$=2.7V | | | | 20 | μA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | 40 | |
| $I_{IL}$ | Low-level input current | J, $\overline{K}$, T | $V_{CC}$=5.5V, $V_I$=0.4V | | | | −0.2 | mA |
| | | $\overline{S_D}$, $\overline{R_D}$ | | | | | −0.4 | |
| $I_O$ | Output current | | $V_{CC}$=5.5V, $V_O$=2.25V | | −30 | | −112 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$=5.5V (Note 2) | | | 2.4 | 4 | mA |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

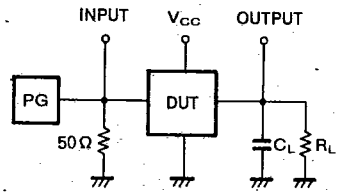
Note 2: The supply current is measured alternately at J = $\overline{K}$ = $\overline{S_D}$ = T = 0V, $\overline{R_D}$ = 4.5V (Q = high-level) and J = $\overline{K}$ = $\overline{R_D}$ = T = 0V, $\overline{S_D}$ = 4.5V ($\overline{Q}$ = high-level).

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | | | Test conditions/Limits (Note 3) | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$=5V, $C_L$=15pF, $R_L$=500Ω | $V_{CC}$=4.5~5.5V, $C_L$=50pF, $R_L$=500Ω | | | | | | |
| | | | | $T_a$=25°C | $T_a$=0~70°C | | | $T_a$=−20~+75°C | | | |
| | | Inputs | Outputs | Typ | Min | Typ* | Max | Min | Typ* | Max | |
| $f_{max}$ | Maximum clock frequency | T | Q, $\overline{Q}$ | | 34 | 75 | | 30 | 75 | | MHz |
| $t_{PLH}$ | Propagation time | $\overline{S_D}$, $\overline{R_D}$ | Q, $\overline{Q}$ | 4.5 | 3 | 6.5 | 13 | 3 | 6.5 | 14 | ns |
| $t_{PHL}$ | | | | 7 | 5 | 9.5 | 15 | 5 | 9.5 | 16 | |
| $t_{PLH}$ | | T | Q, $\overline{Q}$ | 6.5 | 5 | 8.5 | 16 | 5 | 8.5 | 17 | ns |
| $t_{PHL}$ | | | | 7 | 5 | 10 | 18 | 5 | 10 | 19 | |

*: All typical values are at $V_{CC}$ = 5V, $T_a$ = 25°C.

Note 3: Measurement circuit




(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
$t_r$=2ns, $t_f$=2ns
$V_{IH}$=3.5V, $V_{IL}$=0.3V
duty cycle=50%
$Z_O$=50Ω

(2) $C_L$ includes probe and jig capacitance.

## DUAL J-$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH SET AND RESET

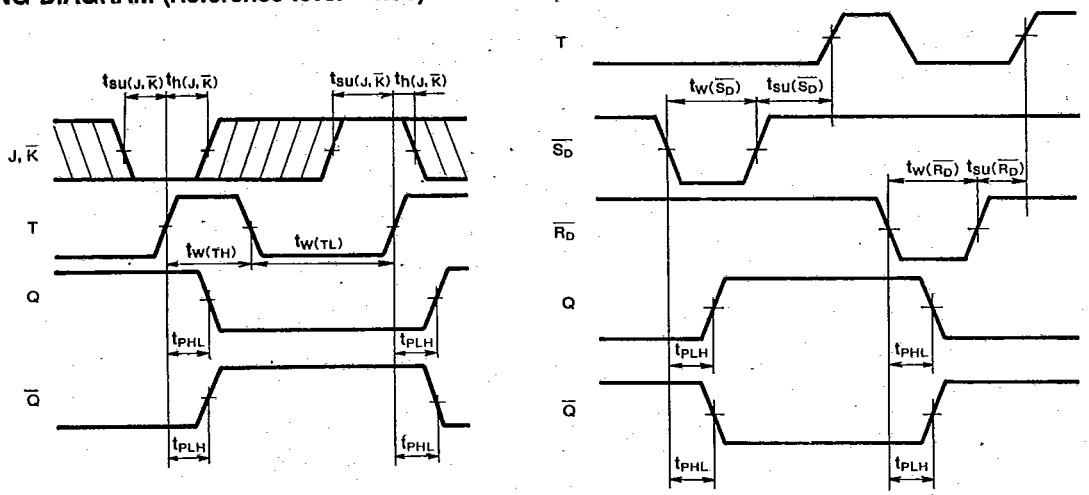
### TIMING REQUIREMENTS ($V_{CC}$=4.5V~5.5V, $C_L$=50pF, $R_L$=500Ω)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_a$=0~70℃ | | | $T_a$=−20~+75℃ | | | |
| | | | Min | Typ* | Max | Min | Typ* | Max | |
| $t_{w(\overline{S_D})}$ | Pulse width | $\overline{S_D}$ "L" | 15 | 5 | | 16 | 5 | | ns |
| $t_{w(\overline{R_D})}$ | | $\overline{R_D}$ "L" | 15 | 5 | | 16 | 5 | | |
| $t_{w(TH)}$ | | T "H" | 14.5 | 4 | | 15.5 | 4 | | |
| $t_{w(TL)}$ | | T "L" | 14.5 | 9.5 | | 15.5 | 9.5 | | |
| $t_{su(J,\overline{K})}$ | Setup time before T ↑ | J, $\overline{K}$ | 15 | 3.5 | | 16 | 3.5 | | ns |
| $t_{su(\overline{S_D})}$ | | $\overline{S_D}$ "H" (inactive) | 10 | 1 | | 11 | 1 | | |
| $t_{su(\overline{R_D})}$ | | $\overline{R_D}$ "H" (inactive) | 10 | 1 | | 11 | 1 | | |
| $t_{h(D)}$ | Hold time after T ↑ | J, $\overline{K}$ | 0 | −1 | | 1 | −1 | | ns |

*: All typical values are at $V_{CC}$=5V, $T_a$=25°C.

↑: Transition from low to high (positive edge trigger)

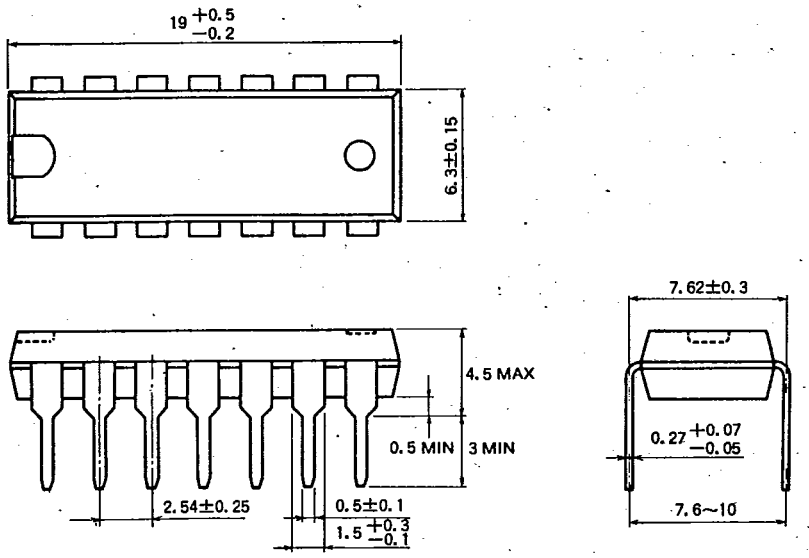
### TIMING DIAGRAM (Reference level = 1.3V)




Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

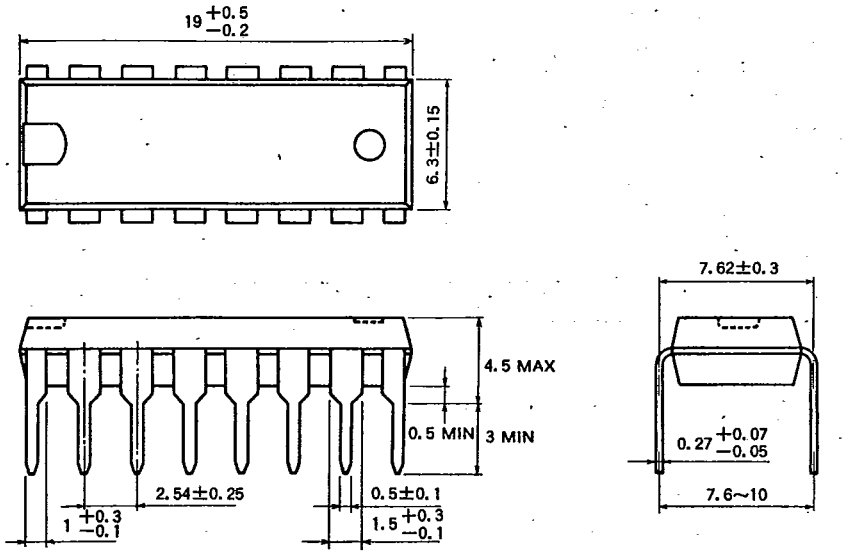
## TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm




## TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm

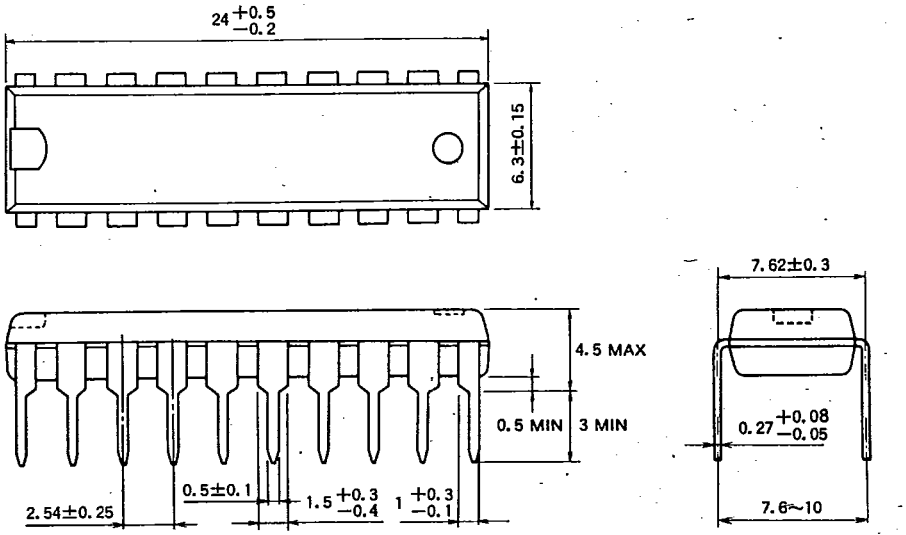


# PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)
91D 12324 D T-90-20

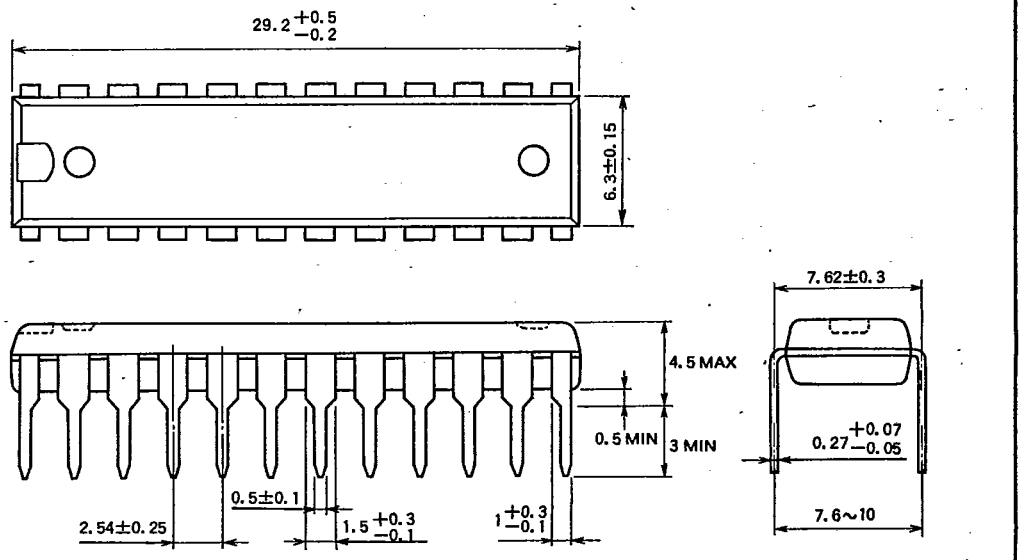
## TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm




## TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



# TYPE DESIGNATION TABLE



## ALSTTL SERIES SOP TYPE DESIGNATION TABLE

| Type | | Circuit function | Package Outlines |
|---|---|---|---|
| M74ALS00ADP | ★ | Quadruple 2-Input Positive NAND Gate | 14P2P |
| M74ALS02DP | ★ | Quadruple 2-Input Positive NOR Gate | 14P2P |
| M74ALS04ADP | ★ | Hex Inverter | 14P2P |
| M74ALS05ADP | ★★ | Hex Inverter with Open Colletor Output | 14P2P |
| M74ALS08DP | ★ | Quadruple 2-Input Positive AND Gate | 14P2P |
| M74ALS09DP | ★★ | Quadruple 2-Input Positive AND Gate with Open Collector Output | 14P2P |
| M74ALS10ADP | ★ | Triple 3-Input Positive NAND Gate | 14P2P |
| M74ALS11ADP | ★ | Triple 3-Input Positive AND Gate | 14P2P |
| M74ALS20ADP | ★★ | Dual 4-Input Positive NAND Gate | 14P2P |
| M74ALS27DP | ★★ | Triple 3-Input Positive NOR Gate | 14P2P |
| M74ALS30ADP | ★★ | Single 8-Input Positive NAND Gate | 14P2P |
| M74ALS32DP | ★ | Quadruple 2-Input Positive OR Gate | 14P2P |
| M74ALS37ADP | ★★ | Quadruple 2-Input Positive NAND Buffer | 14P2P |
| M74ALS38ADP | ★★ | Quadruple 2-Input Positive NAND Buffer with Open Collector Output | 14P2P |
| M74ALS74ADP | ★ | Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset | 14P2P |
| M74ALS109ADP | ★★ | Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop with Set and Reset | 16P2P |
| M74ALS112ADP | ★ | Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset | 16P2P |
| M74ALS131DP | ★★ | 3-Line to 8-Line Decoder/Demultiplexer with Address Register | 16P2P |
| M74ALS138DP | ★ | 3-Line to 8-Line Decoder/Demultiplexer | 16P2P |
| M74ALS153DP | ★★ | Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe | 16P2P |
| M74ALS157DP | ★ | Quadruple 2-Line to 1-Line Data Selector/Multiplexer | 16P2P |
| M74ALS161BDP | ★★ | Synchronous Presettable 4-Bit Binary Counter with Direct Reset | 16P2P |
| M74ALS163BDP | ★★ | Fully Synchronous Presettable 4-Bit Binary Counter | 16P2P |
| M74ALS169BDP | ★★ | Synchronous 4-Bit Binary Counter | 16P2P |
| M74ALS174DP | ★ | Hex D-Type Positive Edge-Triggered Flip-Flop with Reset | 16P2P |
| M74ALS175DP | ★★ | Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset | 16P2P |
| M74ALS193DP | ★★ | Synchronous Presettable Up/Down 4-Bit Binary Counter | 16P2P |
| M74ALS240ADWP | ★ | Octal Buffer/Line Driver with 3-State Output (Inverted) | 20P2V |
| M74ALS244ADWP | ★ | Octal Buffer/Line Driver with 3-State Output (Noninverted) | 20P2V |
| M74ALS245ADWP | ★★ | Octal Bus Transceiver with 3-State Output (Noninverted) | 20P2V |
| M74ALS245A-1DWP | ★★ | Octal Bus Transceiver with 3-State Output (Noninverted) | 20P2V |
| M74ALS257DP | ★ | Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output | 16P2P |
| M74ALS273DWP | ★★ | Octal D-Type Positive Edge-Triggered Flip-Flop with Reset | 20P2V |
| M74ALS299DWP | ★★ | 8-Bit Universal Shift/Storage Register with 3-State Output | 20P2V |
| M74ALS373DWP | ★★ | Octal D-Type Transparent Latch with 3-State Output | 20P2V |
| M74ALS374DWP | ★★ | Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output | 20P2V |
| M74ALS533DWP | ★★ | Octal D-Type Transparent Latch with 3-State Output (Inverted) | 20P2V |
| M74ALS534DWP | ★★ | Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted) | 20P2V |
| M74ALS561ADWP | ★★ | Synchronous Presettable 4-Bit Binary Counter with 3-State Output | 20P2V |
| M74ALS569ADWP | ★★ | Synchronous Up/Down 4-Bit Binary Counter with 3-State Output | 20P2V |
| M74ALS573ADWP | ★★ | Octal D-Type Transparent Latch with 3-State Output (Noninverted) | 20P2V |
| M74ALS574ADWP | ★★ | Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted) | 20P2V |
| M74ALS640ADWP | ★★ | Octal Bus Transceiver with 3-State Output (Inverted) | 20P2V |
| M74ALS642ADWP | ★★ | Octal Bus Transceiver with Open Collector Output (Inverted) | 20P2V |
| M74ALS645ADWP | ★★ | Octal Bus Transceiver with 3-State Output (Noninverted) | 20P2V |
| M74ALS1034DP | ★★ | Hex Noninverting Buffer | 14P2P |

★: New product ★★ : Under development

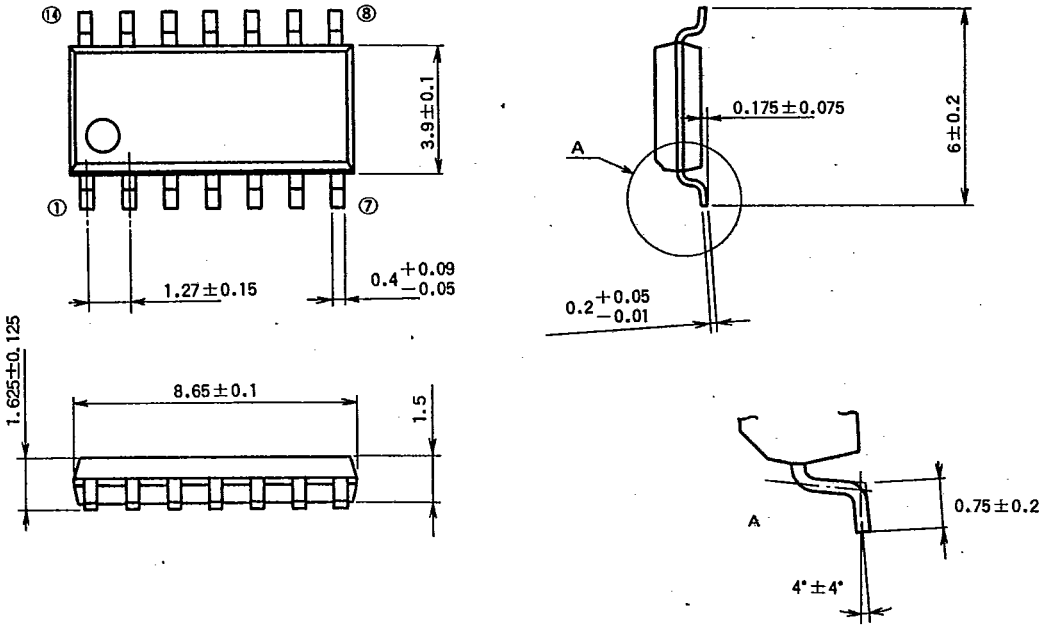
**DESCRIPTION**

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

MITSUBISHI (DGTL LOGIC) 91D D 6249827 0012786 0 MIT3
T-90-20

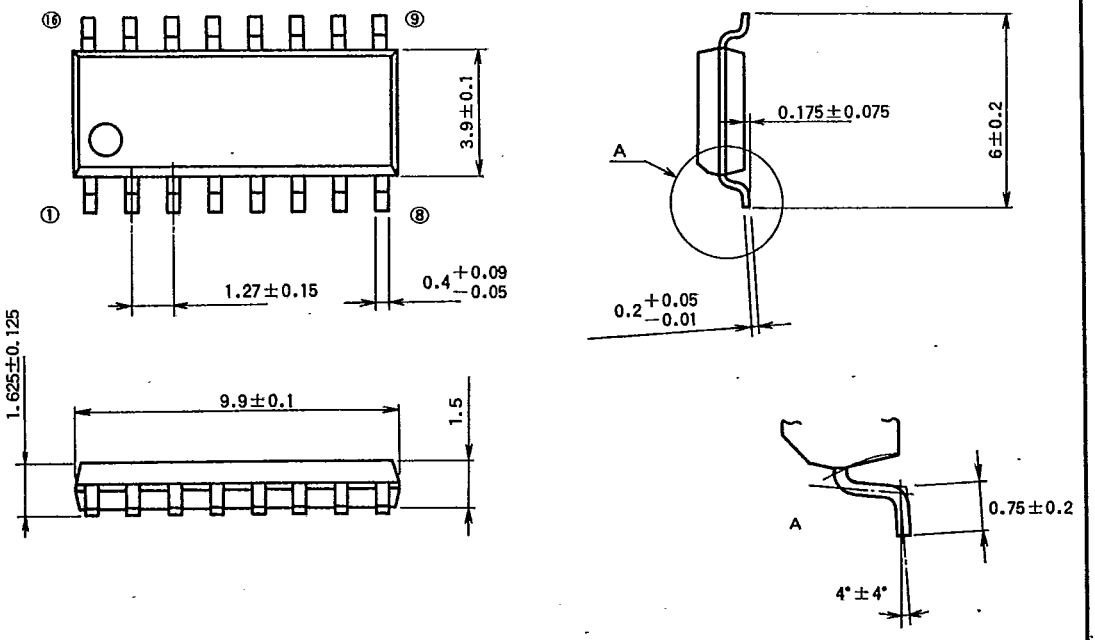
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm




TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



# PACKAGE OUTLINES



TYPE 20P2V 20-PIN MOLDED PLASTIC SOP (JEDEC 300mil body)

Dimension in mm