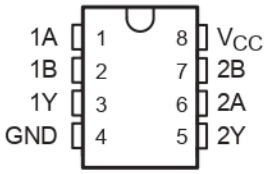
SLRS024 – DECEMBER 1976 – REVISED MAY 1990

## PERIPHERAL DRIVERS FOR HIGH-VOLTAGE HIGH-CURRENT DRIVER APPLICATIONS

- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **Medium-Speed Switching**
- **Circuit Flexibility for Varied Applications and Choice of Logic Function**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability**

**D OR P PACKAGE**
**(TOP VIEW)**




**SUMMARY OF SERIES SN75471**

| DEVICE | LOGIC OF COMPLETE CIRCUIT | PACKAGES |
|---|---|---|
| SN75471 | AND | D, P |
| SN75472 | NAND | D, P |
| SN75473 | OR | D, P |

## description

Series SN75471 dual peripheral drivers are functionally interchangeable with series SN75451B and series SN75461 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than series 75451B (limits are the same as series SN75461). Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN75471, SN75472, and SN75473 are dual peripheral AND, NAND, and OR drivers, respectively, (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

Series SN75471 drivers are characterized for operation from 0°C to 70°C.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage, $V_I$ . . . . . 5.5 V
Inter-emitter voltage (see Note 2) . . . . . 5.5 V
Off-state output voltage, $V_O$ . . . . . 70 V
Continuous collector or output current (see Note 3) . . . . . 400 mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 3) . . . . . 500 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to the network GND, unless otherwise specified.
2. This is the voltage between two emitters, A and B.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

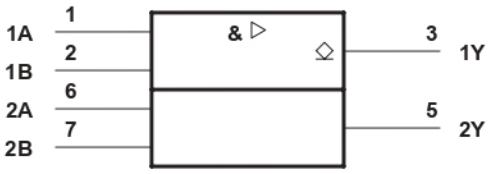
**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

## recommended operating conditions

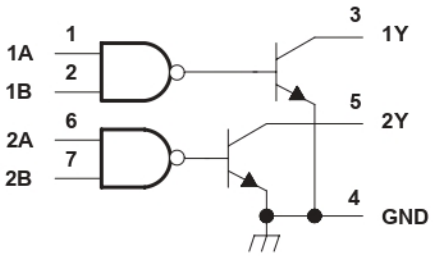
| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

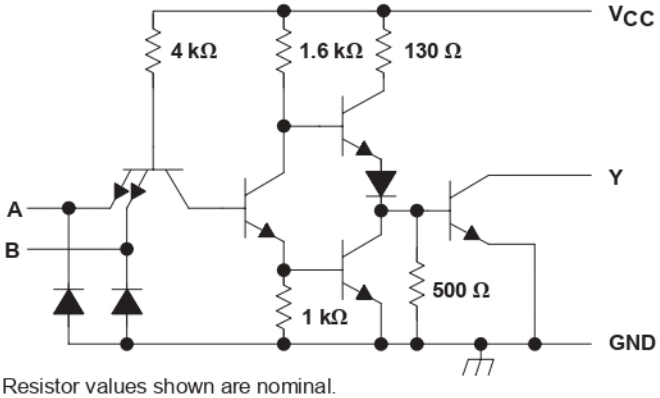



**SN75471 FUNCTION TABLE (each driver)**

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | H (off state) |

positive logic: $Y = AB$ or $\overline{A} + \overline{B}$

## SN75471 schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range

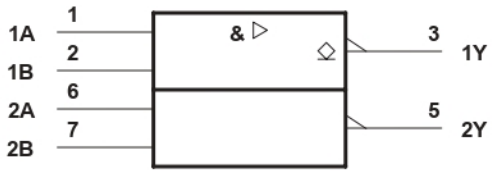
| PARAMETER | | TEST CONDITIONS | SN75471 MIN | SN75471 TYP‡ | SN75471 MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, $I_I$ = –12 mA | | –1.2 | –1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | | 100 | µA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | –1 | –1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 7 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 52 | 65 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

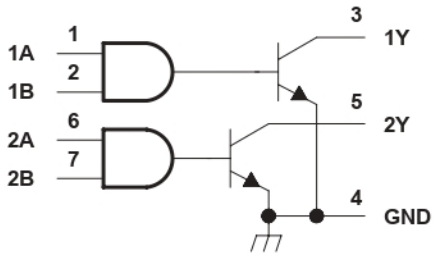
| PARAMETER | | TEST CONDITIONS | SN75471 MIN | SN75471 TYP | SN75471 MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 1 | | 30 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 25 | 40 | |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 8 | 20 | |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 2 | $V_S$–18 | | | mV |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

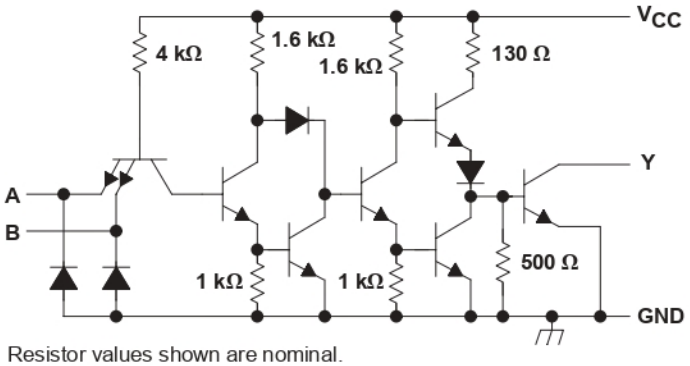



**SN75472 FUNCTION TABLE (each driver)**

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

## SN75472 schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | SN75472 MIN | SN75472 TYP‡ | SN75472 MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, $I_I$ = –12 mA | | –1.2 | –1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | | 100 | µA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | –1 | –1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 13 | 17 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 61 | 76 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

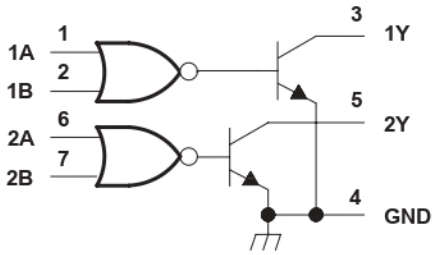
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | SN75472 MIN | SN75472 TYP | SN75472 MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 1 | | 45 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 30 | 50 | |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 13 | 25 | |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 2 | $V_S$–18 | | | mV |

## logic symbol†


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

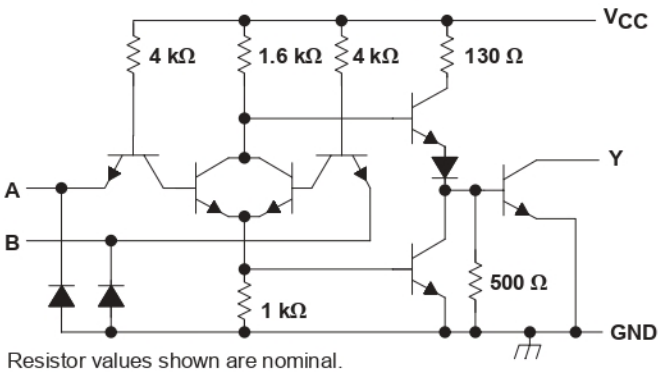



**FUNCTION TABLE (each driver)**

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | H (off state) |

positive logic:
$Y = A + B$ or $\overline{A}\,\overline{B}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range

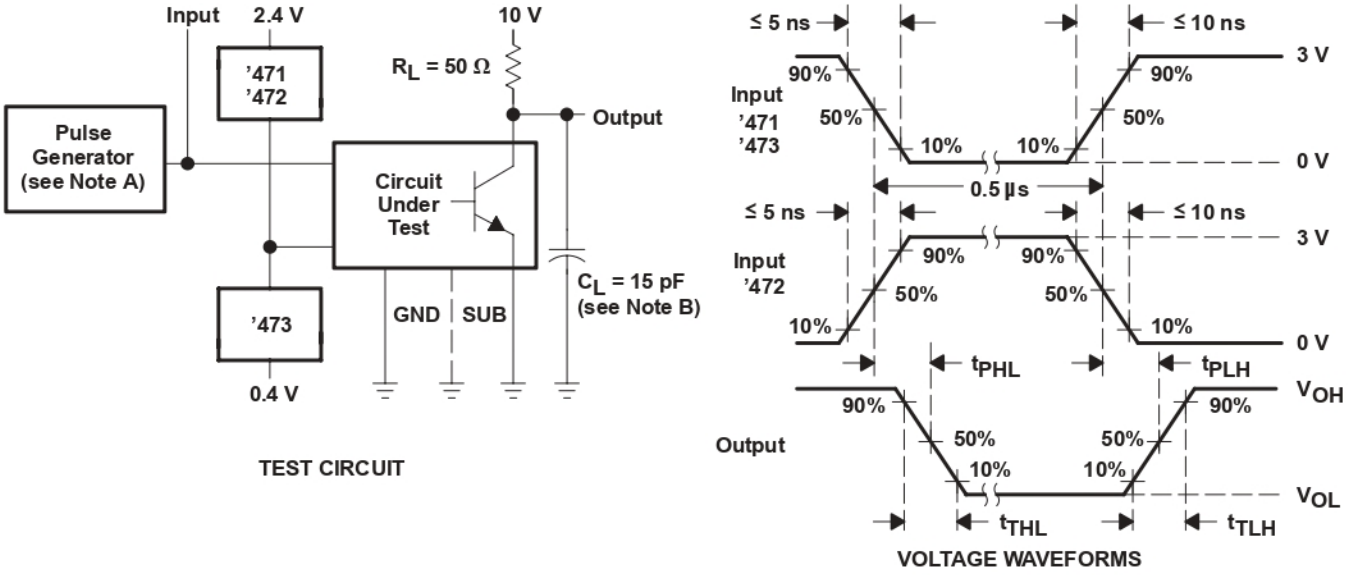
| PARAMETER | | TEST CONDITIONS | | | SN75473 MIN | SN75473 TYP‡ | SN75473 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, | $I_I$ = –12 mA | | | –1.2 | –1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, | $V_{IH}$ = 2 V, | $V_{OH}$ = 70 V | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, | $V_{IL}$ = 0.8 V, | $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, | $V_{IL}$ = 0.8 V, | $I_{OL}$ = 300 mA | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, | $V_I$ = 5.5 V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, | $V_I$ = 2.4 V | | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, | $V_I$ = 0.4 V | | | –1 | –1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, | $V_I$ = 5 V | | | 8 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, | $V_I$ = 0 | | | 58 | 76 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

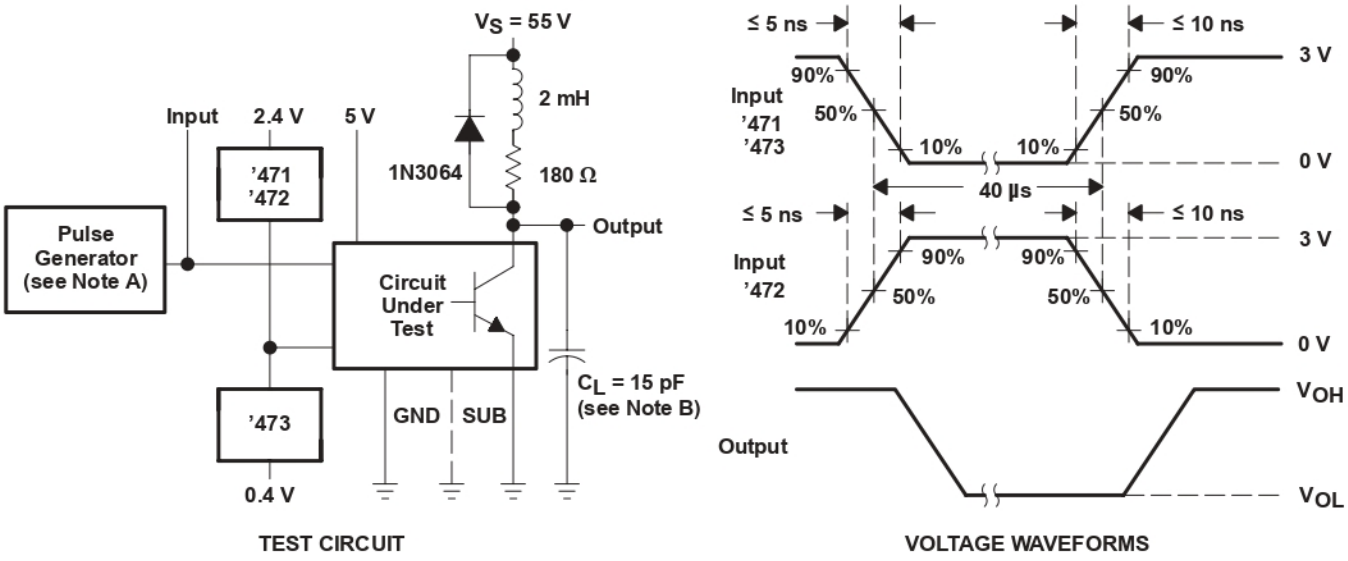
| PARAMETER | | TEST CONDITIONS | | | SN75473 MIN | SN75473 TYP | SN75473 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O$ ≈ 200 mA, | $C_L$ = 15 pF, | | | 30 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $R_L$ = 50 Ω, | See Figure 1 | | | 25 | 40 | |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | | 8 | 25 | |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | | 10 | 25 | |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, | $I_O$ ≈ 300 mA, | See Figure 2 | $V_S$ –18 | | | mV |

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_O$ ≈ 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 1. Switching Times**




NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, $Z_O$ ≈ 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 2. Latch-Up Test**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN75471D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75471DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75471DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75471DR | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI |
| SN75471DRE4 | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI |
| SN75471DRG4 | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI |
| SN75471P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75471PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75472D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75472DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75472DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75472P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75472PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75473D | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI |
| SN75473P | OBSOLETE | PDIP | P | 8 | | TBD | Call TI | Call TI |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

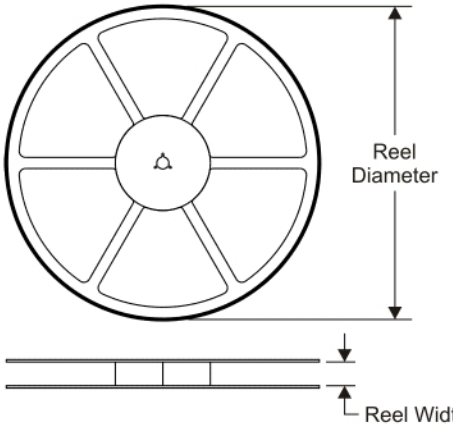
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

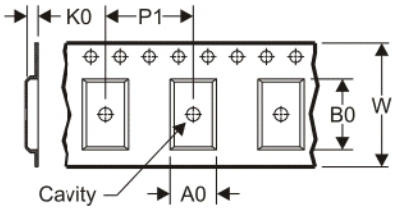
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

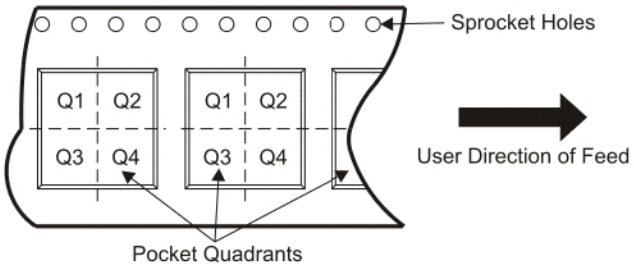



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

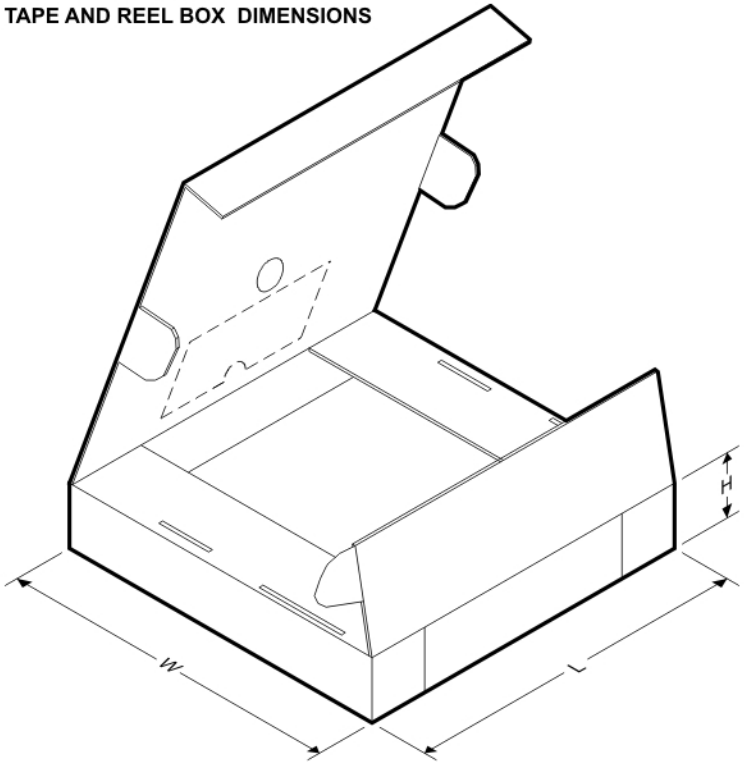
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75471DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

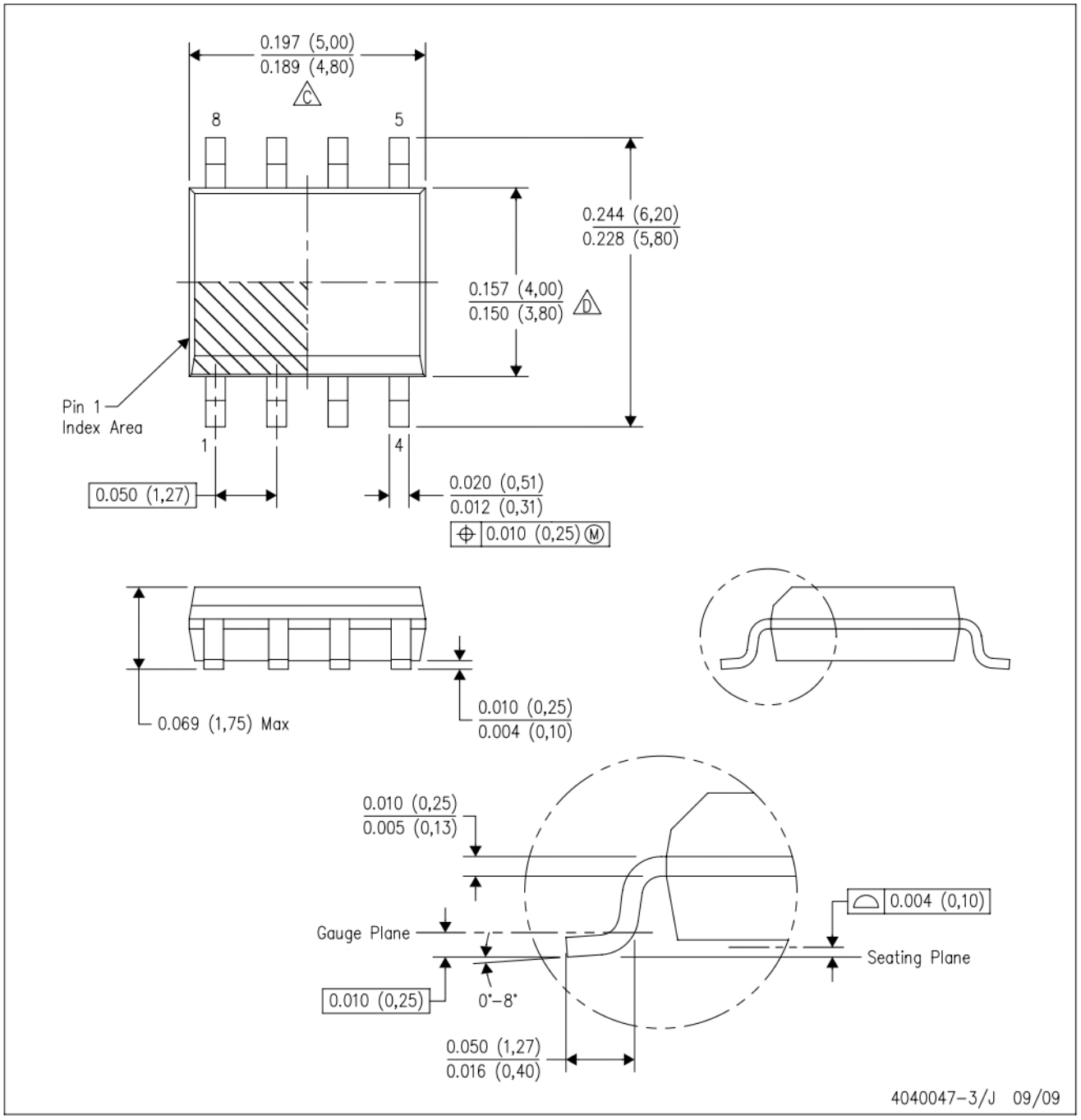
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75471DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

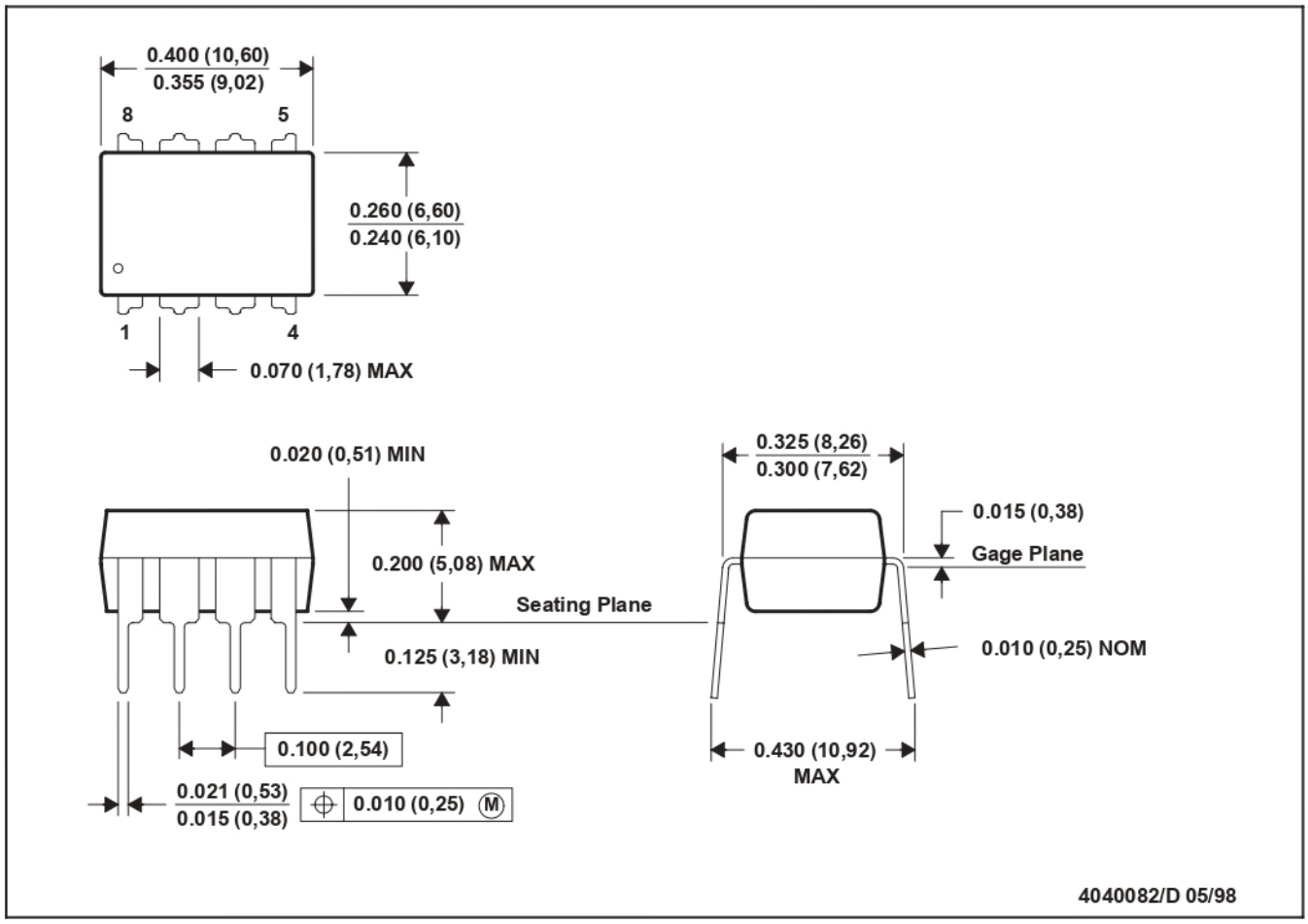
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

**P (R-PDIP-T8)** **PLASTIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm