MC54/74HC354

8-Input Data Selector/ Multiplexer With Data and Address Latches and 3-State Outputs

High–Performance Silicon–Gate CMOS

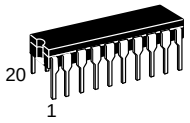
The MC54/74HC354 is identical in pinout to the LS354. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC354 selects one of eight latched binary Data Inputs, as determined by the Address Inputs. The information at the Data Inputs is stored in the transparent 8–bit Data Latch when the Data–Latch Enable pin is held high. The Address information may be stored in the transparent Address Latch, which is enabled by the active–high Address–Enable pin.

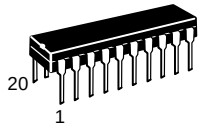
The device outputs are placed in high–impedance states when Output Enable 1 is high, Output Enable 2 is high, or Output Enable 3 is low.

The HC354 has a clocked Data Latch that is not transparent.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 326 FETs or 81.5 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 732–03



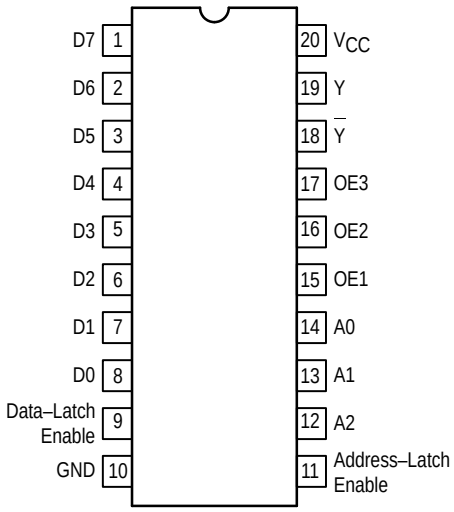
N SUFFIX
PLASTIC PACKAGE
CASE 738–03

DW SUFFIX
SOIC PACKAGE
CASE 751D–04

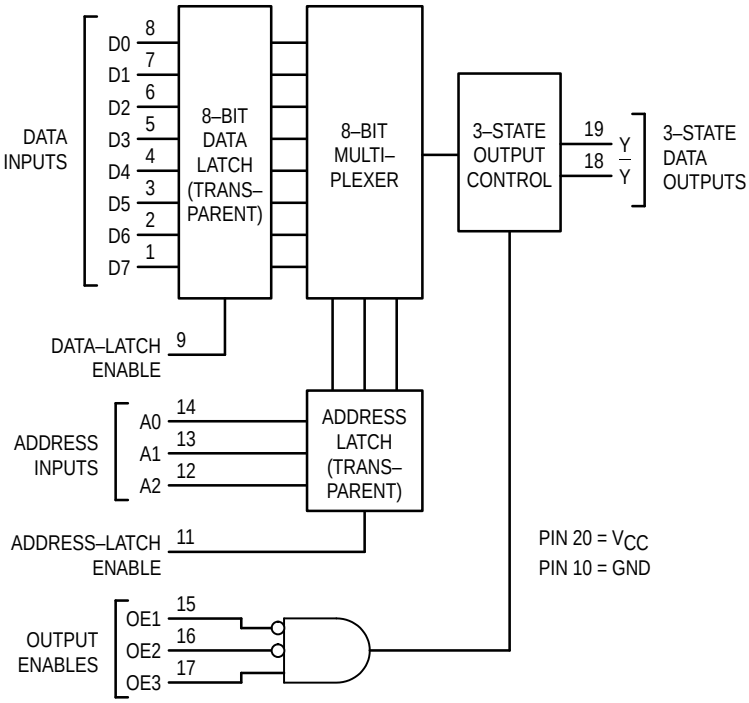
ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXDW	SOIC

Pinout: 20–Lead Package (Top View)



LOGIC DIAGRAM



MOTOROLA

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package Ceramic DIP	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0mA $\|I_{out}\|$ ≤ 7.8mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0mA $\|I_{out}\|$ ≤ 7.8mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D0–D7 to Y or $\overline{Y}$ (Figures 2 and 6)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Data–Latch Enable to Y or $\overline{Y}$ (Figures 3 and 6)	2.0 4.5 6.0	260 52 44	325 65 55	390 78 66	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A0–A2 to Y or $\overline{Y}$ (Figures 2 and 6)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Address–Latch Enable to Y or $\overline{Y}$ (Figures 3 and 6)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, OE1–OE3 to Y or $\overline{Y}$ (Figures 4 and 7)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, OE1–OE3 to Y or $\overline{Y}$ (Figures 4 and 7)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	48	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

D0–D7 (Pins 8–1) DATA INPUTS

These eight data bits are stored in a transparent latch when the Data–Latch Enable pin is active (high). Once enabled, changing inputs will not change the contents of the latch.

A0, A1, A2 (Pins 14,13,12) ADDRESS INPUTS

Selects which data bit stored in the Data Latch is routed to the outputs Y and Y.

DATA–LATCH ENABLE (Pin 9)

The latch is transparent to D0–D7 when enable is inactive (low). The Data–Latch contents are unaffected when enable is held active (high).

ADDRESS–LATCH ENABLE (Pin 11)

The latch is transparent to A0, A1 and A2 when enable is inactive (low). The Address–Latch contents are unaffected when enable is held active (high).

OE1, OE2, OE3 (Pins 15,16,17) OUTPUT ENABLES

Any of the output enable pins inactive (OE1=High or OE2=High or OE3=Low) causes the outputs (Y and Y) to be in high–impedance states.

Y, $\overline{Y}$ (Pins 19,18)

These 3–state outputs (when not 3–stated) represent the data bit in the Data Latch selected by the Address Latch.

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, D0–D7 to Data–Latch Enable (Figure 5)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_{su}	Minimum Setup Time, A0–A2 to Address–Latch Enable (Figure 5)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_h	Minimum Hold Time, Data–Latch Enable to D0–D7 (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_h	Minimum Hold Time, Address–Latch Enable to A0–A2 (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Data–Latch Enable (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Address–Latch Enable (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

FUNCTION TABLE

Address Latch Contents #			Inputs				Outputs		
A2	**A1**	**A0**	**Data–Latch Enable**	**OE1**	**OE2**	**OE3**	**Y**	**$\overline{Y}$**	**Description**
X X X	X X X	X X X	X X X	H X X	X H X	X X L	Z Z Z	Z Z Z	Outputs in High–Impedance States
L L L L H H H H	L L H H L L H H	L H L H L H L H	L	L	L	H	D0 D1 D2 D3 D4 D5 D6 D7	$\overline{D0}$ $\overline{D1}$ $\overline{D2}$ $\overline{D3}$ $\overline{D4}$ $\overline{D5}$ $\overline{D6}$ D7	Data–Latch is Transparent
L L L L H H H H	L L H H L L H H	L H L H L H L H	H	L	L	H	$D0_n$ $D1_n$ $D2_n$ $D3_n$ $D4_n$ $D5_n$ $D6_n$ $D7_n$	$\overline{D0}_n$ $\overline{D1}_n$ $\overline{D2}_n$ $\overline{D3}_n$ $\overline{D4}_n$ $\overline{D5}_n$ $\overline{D6}_n$ $\overline{D7}_n$	New Data is Stored in Data–Latch and is Not Alterable

# Represents bits in Address–Latch. See Address–Latch Enable pin description.
X = Don't Care; Z = High Impedance; D0–D7 = the data at inputs D0 through D7; $D0_n$–$D7_n$ = the data present at inputs D0 through D7 when the Data–Latch Enable pin was taken high.

SWITCHING WAVEFORMS

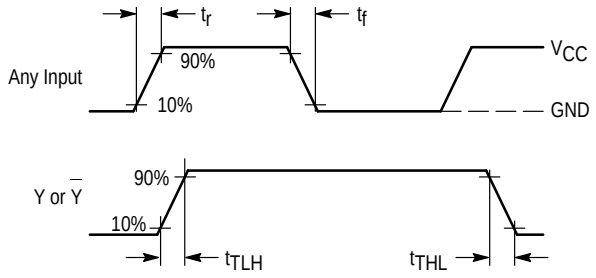


Figure 1.

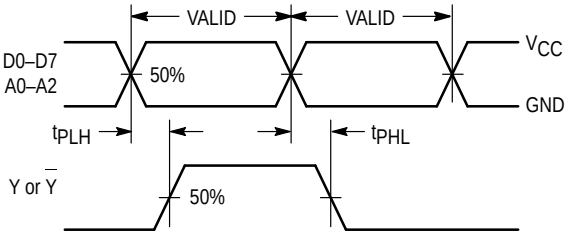


Figure 2.

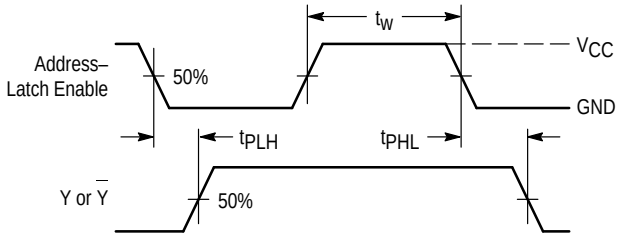


Figure 3.

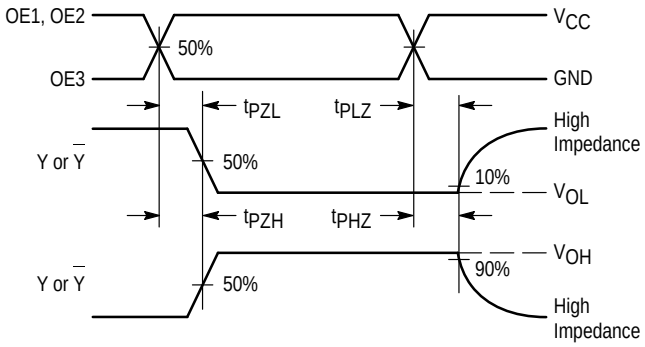


Figure 4.

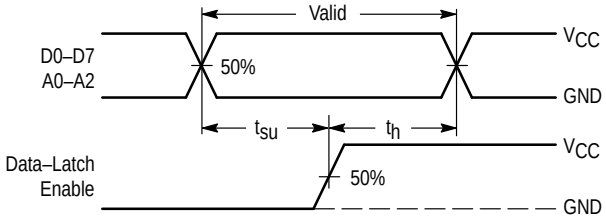
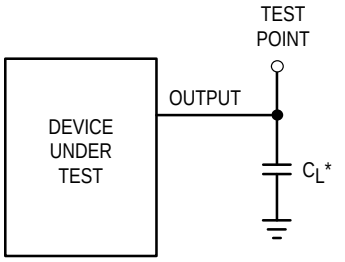


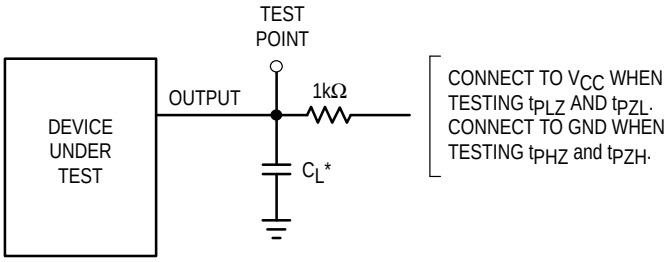
Figure 5.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 6.



*Includes all probe and jig capacitance

Figure 7.

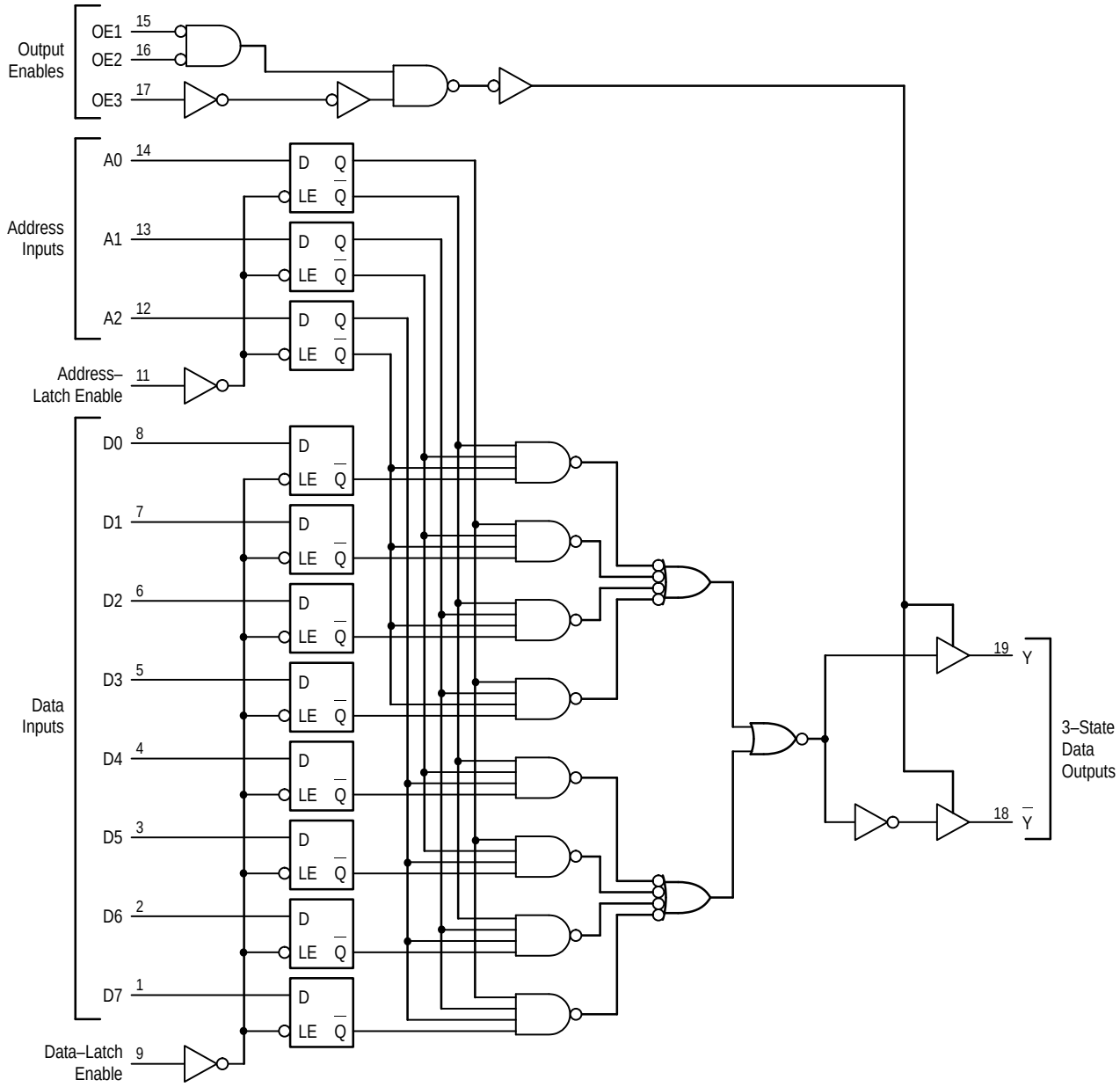
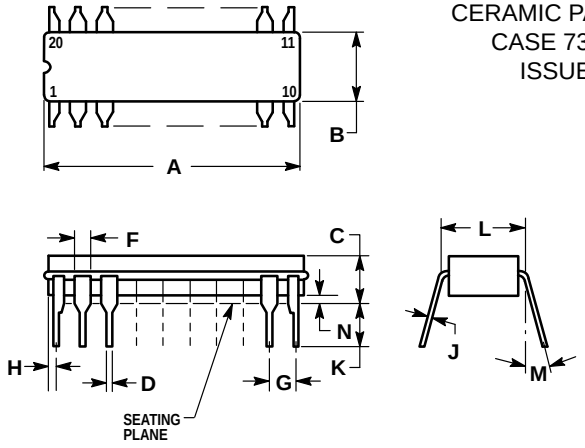


Figure 8. Expanded Logic Diagram

OUTLINE DIMENSIONS

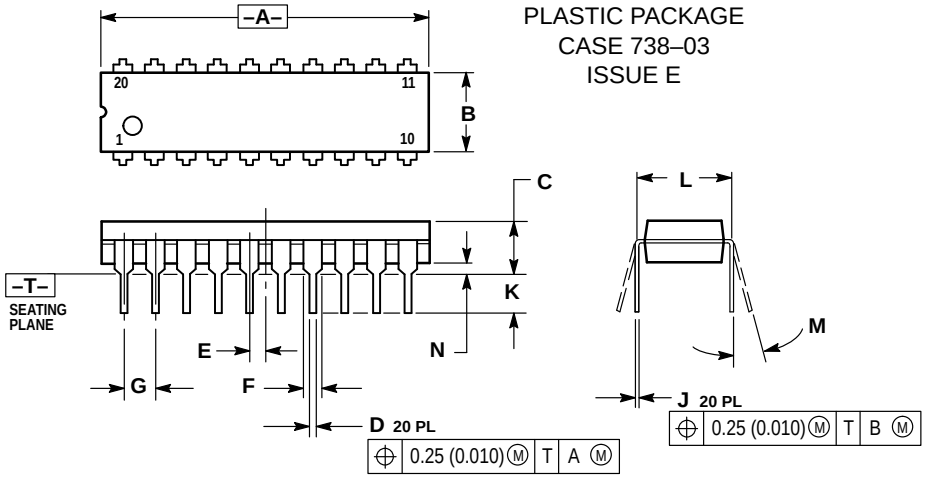
J SUFFIX
CERAMIC PACKAGE
CASE 732–03
ISSUE E



NOTES:
1. LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0 °	15 °	0 °	15 °
N	0.25	1.02	0.010	0.040

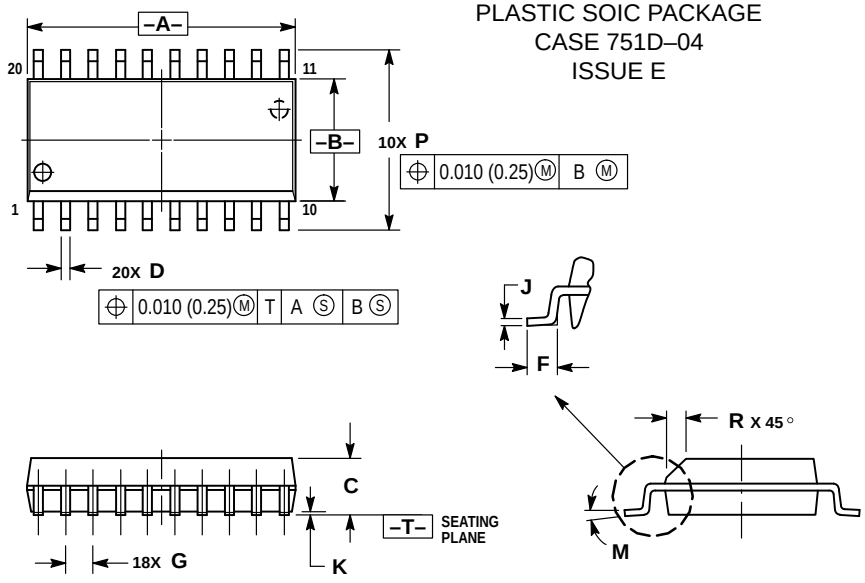
N SUFFIX
PLASTIC PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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