MC54/74HC158

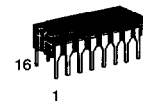
Quad 2-Input Data Selector/Multiplexer

High–Performance Silicon–Gate CMOS

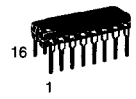
The MC54/74HC158 is identical in pinout to the LS158. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices route 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in inverted form for the HC158. A high level on the Output Enable input sets all four Y outputs to a high level for the HC158.

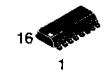
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6V
- Low Input Current: 1μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 74 FETs or 18.5 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620–10



N SUFFIX
PLASTIC PACKAGE
CASE 648–08

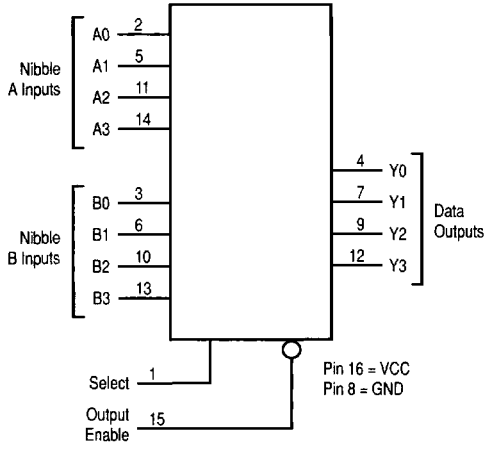


D SUFFIX
SOIC PACKAGE
CASE 751B–05

ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

LOGIC DIAGRAM

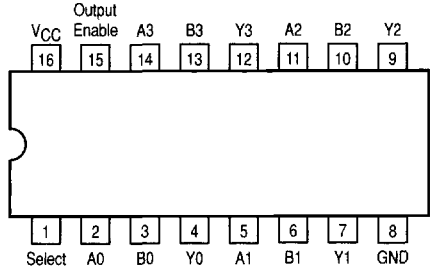


FUNCTION TABLE

Inputs		Outputs
Output Enable	**Select**	**Y0–Y3**
H	X	H
L	L	$\overline{A0}$–$\overline{A3}$
L	H	$\overline{B0}$–$\overline{B3}$

X = Don't Care
A0–A3, B0–B3 = the levels of the respective Data–Word inputs.

Pinout: 16–Lead Plastic Package (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 3 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 5)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2.

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	35	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

SWITCHING WAVEFORMS

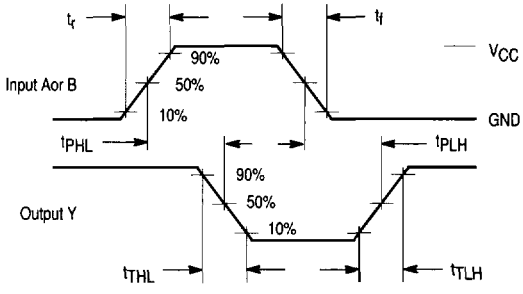


Figure 1.

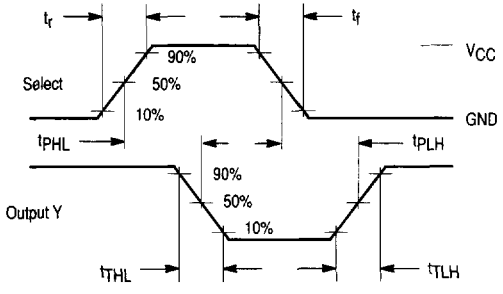


Figure 2. Y versus Select, Inverted

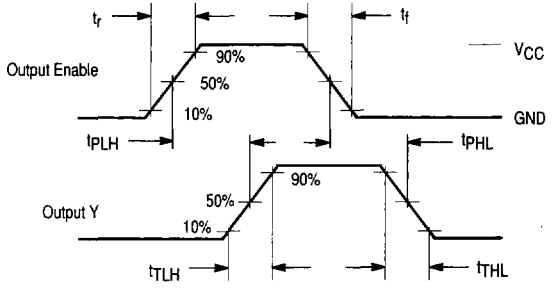
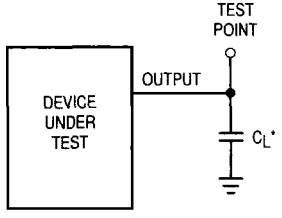


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

PIN DESCRIPTIONS

INPUTS

A0–A3 (Pins 2,5,11,14)

Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in inverted form for the HC158.

B0–B3 (Pins 3,6,10,13)

Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in inverted form for the HC158.

OUTPUTS

Y0–Y3 (Pins 4,7,9,12)

Data outputs. The selected input nibble is presented at these outputs when the Output Enable input is at a low level. The data present on these pins is in its inverted form for the HC158. For the Output Enable input at a high level, the outputs are at a high level for the HC158.

CONTROL INPUTS

Select (Pin 1)

Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

Output Enable (Pin 15)

Output Enable input. A low level on thisinput allows the selected data to be presented at the outputs. A high level on this input sets all of the outputs to a high level for the HC158.

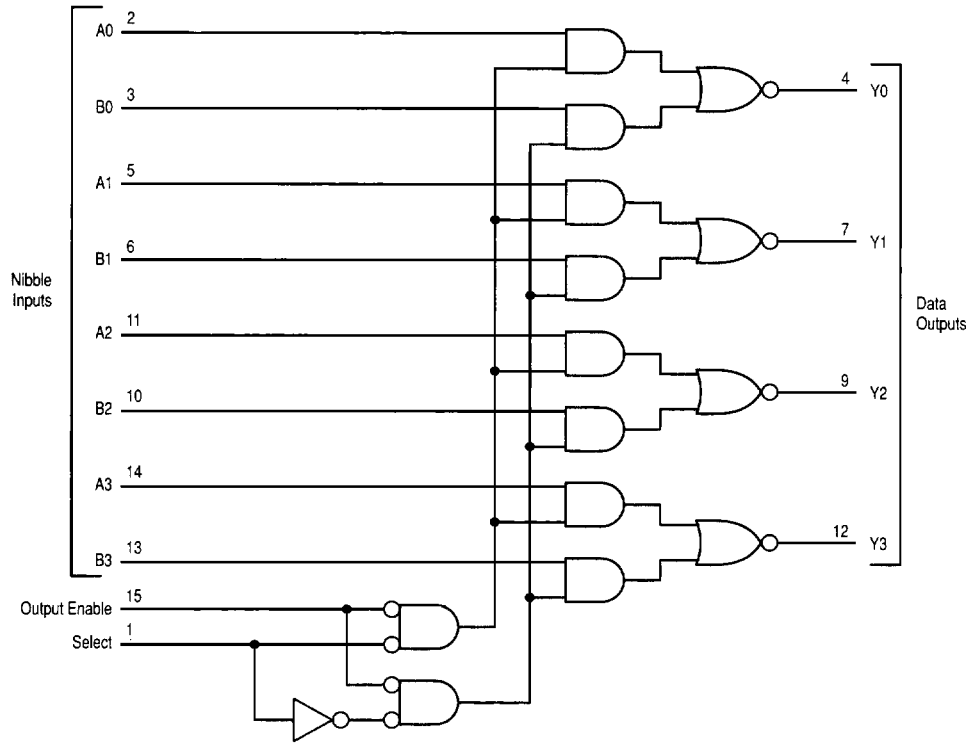


Figure 5. Expanded Logic Diagram