M74LS03P

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS03P is a semiconductor integrated circuit containing four dual-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in AND-Tie connection
- High breakdown input voltage ($V_I \geqq 15V$)
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power dissipation (P_d = 8mW typical)
- High speed (t_{pd} = 10ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

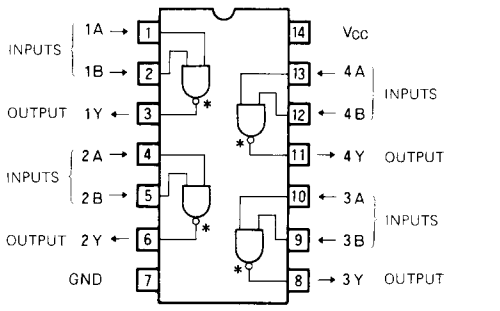
With use of open collector outputs and SBD inputs featuring a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

When inputs A and B are high, output Y is low and when one or both inputs are low, the output Y is high.

FUNCTION TABLE

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

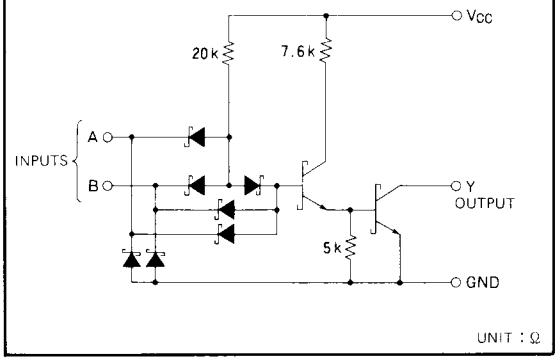
PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_O = 5.5V$	0		100	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

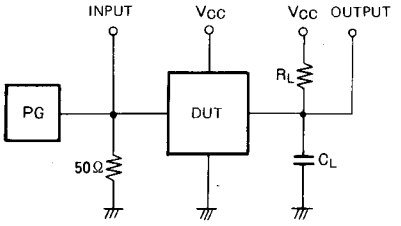
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
I_{OH}	High-level output current	$V_{CC}=4.75V$, $V_I=0.8V$, $V_O=5.5V$				100	μA
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{CCH}	Supply current, all inputs high	$V_{CC}=5.25V$, $V_I=0V$			0.8	1.6	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			2.4	4.4	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

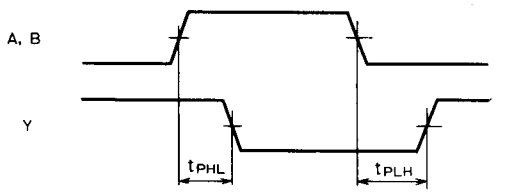
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level/high-to-low-level output propagation time	$R_L = 2\ k\Omega$, $C_L = 15\ pF$ (Note 1)		10	32	ns
t_{PHL}				10	28	ns

Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



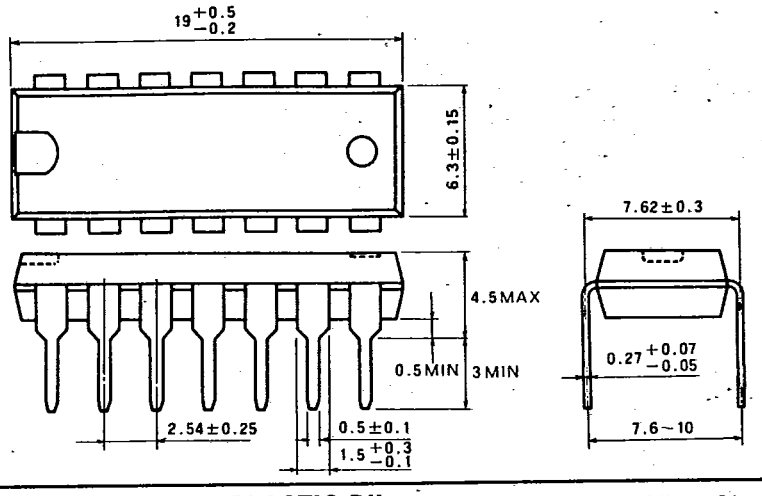
MITSUBISHI ELECTRIC

MITSUBISHI {DGTL LOGIC} 07E D 6249827 0013561 3

T-90-20

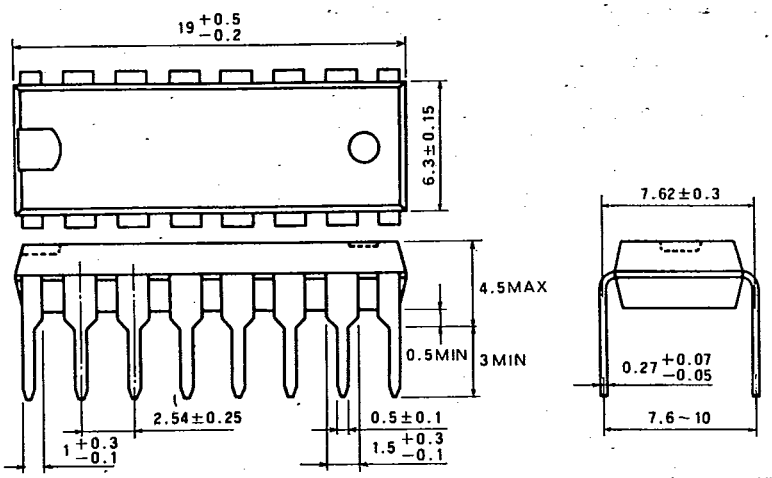
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm