

SN54HC51, SN74HC51

AND-OR-INVERT Gates

The 'HC51 provides 2-wide, 2-input, and 2-wide, 3-input AND-OR-INVERT gates. The device performs the following Boolean functions: $1Y = \overline{(1A \cdot 1B \cdot 1C)} + \overline{(1D \cdot 1E \cdot 1F)}$, $2Y = \overline{(2A \cdot 2B)} + \overline{(2C \cdot 2D)}$

The SN54HC51 is characterized for operation over the full military temperature range of -55°C to 125°C while the SN74HC51 is characterized for operation from -40°C to 85°C.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54HC51, SN74HC51 AND-OR-INVERT GATES

D2684, DECEMBER 1982 - REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'HC51 provides 2-wide, 2-input, and 2-wide, 3-input AND-OR-INVERT gates. The device performs the following Boolean functions:

$$1Y = (\overline{1A \cdot 1B \cdot 1C}) + (1D \cdot 1E \cdot 1F)$$

$$2Y = (\overline{2A \cdot 2B}) + (2C \cdot 2D)$$

The SN54HC51 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC51 is characterized for operation from -40°C to 85°C.

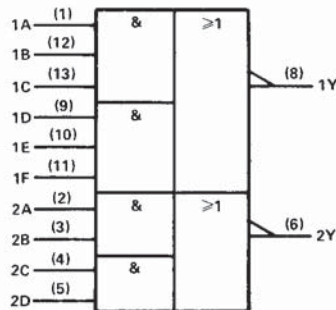
FUNCTION TABLES

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

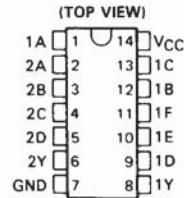
H = high level, L = low level, X = irrelevant

logic symbol†

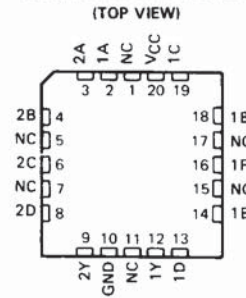


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

SN54HC51 . . . J PACKAGE SN74HC51 . . . D OR N PACKAGE

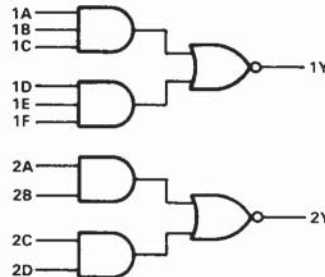


SN54HC51 . . . FK PACKAGE



NC—No internal connection

logic diagram (positive logic)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN54HC51, SN74HC51 AND-OR-INVERT GATES

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC51			SN74HC51			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	$V_{CC} = 2$ V				1.5			V
	$V_{CC} = 4.5$ V	3.15			3.15			
	$V_{CC} = 6$ V	4.2			4.2			
V_{IL} Low-level input voltage	$V_{CC} = 2$ V	0	0.3		0	0.3		V
	$V_{CC} = 4.5$ V	0	0.9		0	0.9		
	$V_{CC} = 6$ V	0	1.2		0	1.2		
V_I Input voltage		0	V_{CC}		0	V_{CC}		V
V_O Output voltage		0	V_{CC}		0	V_{CC}		V
t_t Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000		0	1000		ns
	$V_{CC} = 4.5$ V	0	500		0	500		
	$V_{CC} = 6$ V	0	400		0	400		
T_A Operating free-air temperature		-55	125		-40	85		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC51		SN74HC51		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20$ μA	2 V	1.9	1.998		1.9	1.9		V	
		4.5 V	4.4	4.499		4.4	4.4			
		6 V	5.9	5.999		5.9	5.9			
	4.5 V	3.98	4.30		3.7	3.84				
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -5.2$ mA	6 V	5.48	5.80		5.2	5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20$ μA	2 V		0.002	0.1		0.1	0.1	V	
		4.5 V		0.001	0.1		0.1	0.1		
		6 V		0.001	0.1		0.1	0.1		
	4.5 V		0.17	0.26		0.4	0.33			
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 5.2$ mA	6 V		0.15	0.26		0.4	0.33		
I_I	$V_I = V_{CC}$ or 0	6 V		± 0.1	± 100		± 1000	± 1000	nA	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			2		40	20	μA	
C_i		2 to 6 V		3	10		10	10	pF	

**SN54HC51, SN74HC51
AND-OR-INVERT GATES**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25 °C			SN54HC51		SN74HC51		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Any	Y	2 V		54	140		210		175	ns
			4.5 V		15	28		42		35	
			6 V		12	24		36		30	
t _t		Y	2 V		28	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		8	13		19		16	

C _{pd}	Power dissipation capacitance per AOI gate	No load, T _A = 25 °C	25 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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HCMOS Devices