PLESSEY
Semiconductors

SP1672

TRIPLE 2-INPUT EXCLUSIVE-OR GATE

This three gate ECL array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which ensures that the threshold point remains in the centre of the transition region over the temperature range (0° C to +75° C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

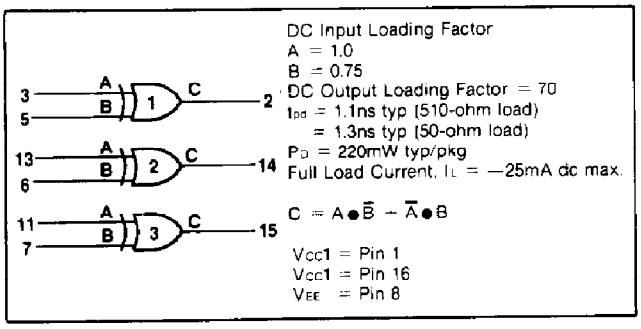

Fig.1 Logic diagram of SP1672

ORDERING INFORMATION

SP1672DG (Commercial-ceramic package)

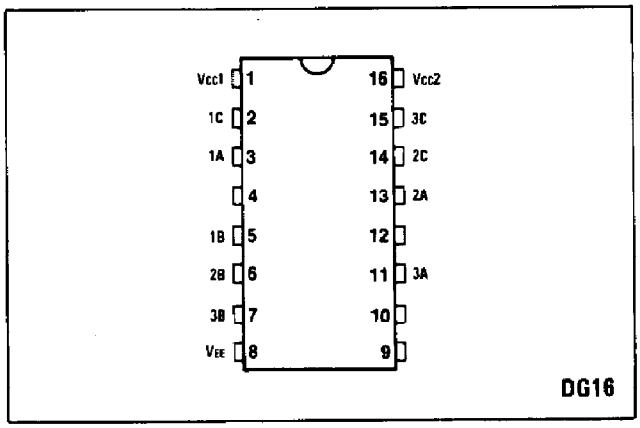

Fig.2 Pin connections (top view)

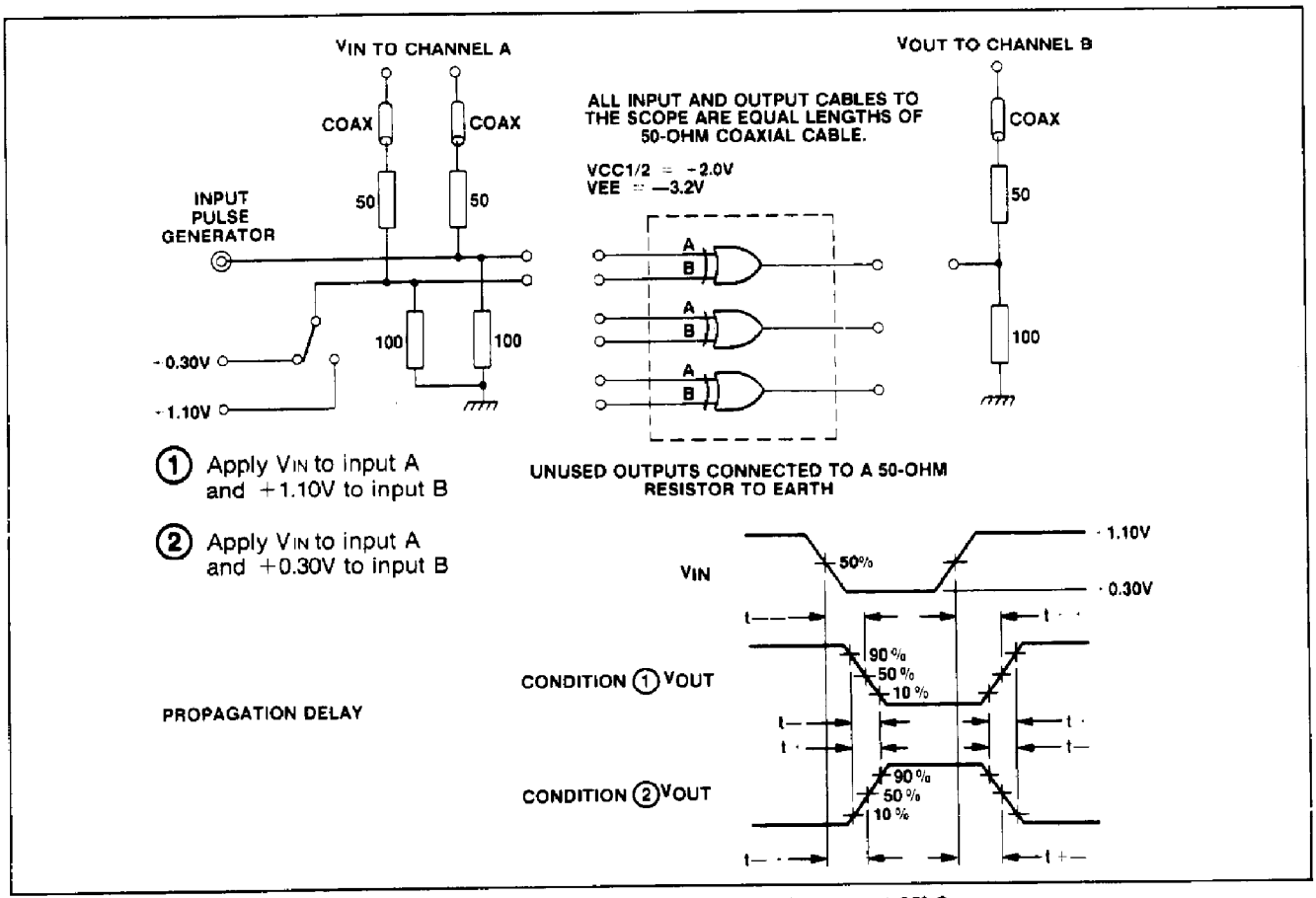

Fig.3 Switching time test circuit and waveforms at +25° C

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Outputs are tested with a 50Ω resistor to -2.0V dc.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Input voltages	V_{CC} to V_{EE}
Output source current	<40mA
Storage temperature range	-55° C to +150° C

Thermal characteristics
DG16
θ_{JA} = 107° C/W
θ_{JC} = 31° C/W

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
0° C	-0.840	-1.870	-1.350		-1.500
+25° C	-0.810	-1.850	-1.095	-1.485	-5.2
+75° C	-0.720	-1.830	-1.035	-1.460	-5.2

Characteristic	Symbol	Pin under test	SP1672 Test Limits 0° C Min.	0° C Max.	+25° C Min.	+25° C Max.	+75° C Min.	+75° C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	GND
POWER SUPPLY															
Drain current	I_E	8	-	-	-	55	-	-	mAdc	All inputs	-	-	-	8	1,16
Input current	I_{INH}	3,11,13	-	-	-	350	-	-	μAdc	*	-	-	-	8	1,16
	0.75 I_{INH}	5,6,7	-	-	-	270	-	-	μAdc	*	-	-	-	8	1,16
	I_{INL}	*	-	-	0.5	-	-	-	μAdc	-	*	-	-	8	1,16
Logic '1' output voltage	V_{OH}	2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	3	5	-	-	8	1,16
		2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	5	3	-	-	8	1,16
Logic '0' output voltage	V_{OL}	2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	3,5	-	-	-	8	1,16
		2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	-	3.5	-	-	8	1,16
Logic '0' threshold voltage	V_{OHA}	2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	3	5	8	1,16
		2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	5	3	8	1,16
Logic '0' threshold voltage	V_{OLA}	2	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	3.5	-	8	1,16
		2	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	-	3,5	8	1,16
SWITCHING TIME (50 ohm load)			Typ.	Max.	Typ.	Max.	Typ.	Max.			-	Pulse in	Pulse out	-3.2V	+2.0V
Propagation delay	t_{3+2+}	2	1.3	1.8	1.3	1.8	1.5	2.2	ns	-	-	3	2	8	1,16
	t_{3-2+}	2	1.3	1.8	1.3	1.8	1.5	2.2		-	-				
	t_{3+2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		-	-				
	t_{3-2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		-	-				
	t_{5+5+}	2	1.7	2.3	1.7	2.3	1.9	2.7		-	-	5			
	t_{5-2+}	2								-	-				
	t_{5+2-}	2								-	-				
	t_{5-2-}	2								-	-				
Rise time	t_{2+}	2	1.9	2.5	1.9	2.5	2.1	2.8	ns	-	-	3	2	8	1,16
Fall time	t_{2-}	2	1.6	2.2	1.6	2.2	1.8	2.5	ns	-	-	3	2	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test.