

# SN54HC7008, SN74HC7008 6-SECTION MULTIFUNCTION (NAND, INVERT, NOR) CIRCUITS

D2880, MARCH 1985—REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

### description

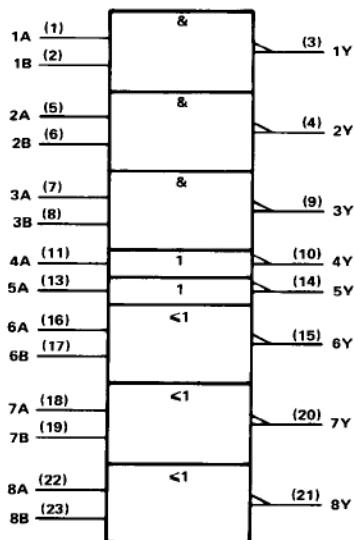
The SN54HC7008 and SN74HC7008 are each comprised of the following sections:

- Three 2-input NAND gates
- Three 2-input NOR gates
- Two inverters

They perform the Boolean functions shown under each function table.

The SN54HC7008 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC7008 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### logic symbol<sup>†</sup>



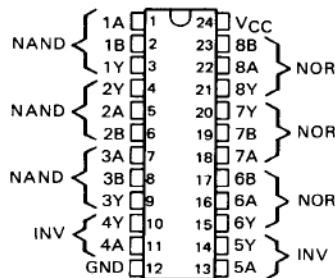
<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

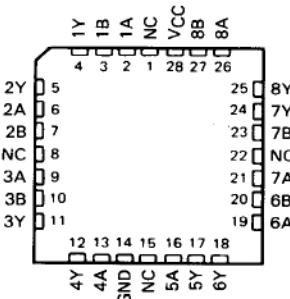
**PRODUCTION DATA** documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**SN54HC7008 . . . JT PACKAGE**  
**SN74HC7008 . . . DW OR NT PACKAGE**

(TOP VIEW)



**SN54HC7008 . . . FK PACKAGE**  
(TOP VIEW)

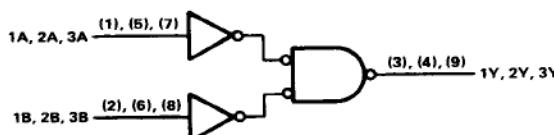


NC—No internal connection

**SN54HC7008, SN74HC7008  
6-SECTION MULTIFUNCTION (NAND, INVERT, NOR) CIRCUITS**

logic diagrams (positive logic)

**2-INPUT NAND GATES**



FUNCTION TABLE

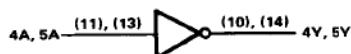
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

positive logic:  $Y = \overline{A} \cdot \overline{B}$  or  
 $Y = \overline{A + B}$

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**HCMOS Devices**

**INVERTERS**

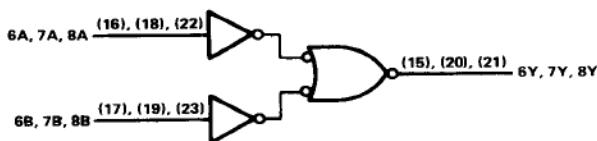


FUNCTION TABLE  
(EACH INVERTER)

INPUT	OUTPUT
A	Y
H	L
L	H

positive logic:  $Y = \overline{A}$

**2-INPUT NOR GATES**



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

positive logic:  $Y = \overline{A + B}$  or  
 $Y = \overline{A} \cdot \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

**absolute maximum ratings over operating free-air temperature range<sup>†</sup>**

Supply voltage, V <sub>CC</sub> .....	-0.5 V to 7 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> ) .....	± 20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) .....	± 20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> ) .....	± 25 mA
Continuous current through V <sub>CC</sub> or GND pins .....	± 50 mA
Lead temperature 1.6 mm (1/16 in) from case for 60 s: FK or JT package .....	300°C
Lead temperature 1.6 mm (1/16 in) from case for 10 s: DW or NT package .....	260°C
Storage temperature range .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54HC7008			SN74HC7008			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage		2	5	6	2	5	6	V
V <sub>IH</sub> High-level input voltage	V <sub>CC</sub> = 2 V	1.5			1.5			
	V <sub>CC</sub> = 4.5 V	3.15			3.15			
	V <sub>CC</sub> = 6 V	4.2			4.2			
V <sub>IL</sub> Low-level input voltage	V <sub>CC</sub> = 2 V	0	0.3	0	0	0.3	0.3	V
	V <sub>CC</sub> = 4.5 V	0	0.9	0	0	0.9	0.9	
	V <sub>CC</sub> = 6 V	0	1.2	0	0	1.2	1.2	
V <sub>I</sub> Input voltage		0	V <sub>CC</sub>	0	0	V <sub>CC</sub>	0	V
V <sub>O</sub> Output voltage		0	V <sub>CC</sub>	0	0	V <sub>CC</sub>	0	V
t <sub>t</sub> Input transition (rise and fall) times	V <sub>CC</sub> = 2 V	0	1000	0	0	1000	0	ns
	V <sub>CC</sub> = 4.5 V	0	500	0	0	500	0	
	V <sub>CC</sub> = 6 V	0	400	0	0	400	0	
T <sub>A</sub> Operating free-air temperature		-55		125	-40		85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC7008	SN74HC7008	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9	1.9	1.9	V
		4.5 V	4.4	4.499	4.4	4.4	4.4	
		6 V	5.9	5.999	5.9	5.9	5.9	
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.30	3.7	3.84		
		6 V	5.48	5.80	5.2	5.34		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -5.2 mA	2 V	0.002	0.1	0.1	0.1	0.1	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 20 μA	4.5 V	0.001	0.1	0.1	0.1	0.1	V
		6 V	0.001	0.1	0.1	0.1	0.1	
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26	0.4	0.4	0.33	
		6 V	0.15	0.26	0.4	0.4	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	± 0.1	± 100	± 1000	± 1000	± 1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V		2	40	20	20	μA
C <sub>i</sub>		2 to 6 V	3	10	10	10	10	pF



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50 \text{ pF}$  (see Note 1)

## NAND/NOR gates

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC7008		SN74HC7008		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	2 V	45	90		135		115		ns
			4.5 V	9	18		27		23		
			6 V	8	15		23		20		
t <sub>t</sub>		Y	2 V	38	75		110		95		ns
			4.5 V	8	15		22		19		
			6 V	6	13		19		16		

C <sub>pd</sub>	Power dissipation capacitance per gate	No load, T <sub>A</sub> = 25°C	20 pF typ
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## inverters

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC7008		SN74HC7008		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2 V	45	95		145		120		ns
			4.5 V	9	19		29		24		
			6 V	8	16		25		20		
t <sub>t</sub>		Y	2 V	38	75		110		95		ns
			4.5 V	8	15		22		19		
			6 V	6	13		19		16		

C <sub>pd</sub>	Power dissipation capacitance per inverter	No load, T <sub>A</sub> = 25°C	20 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.