

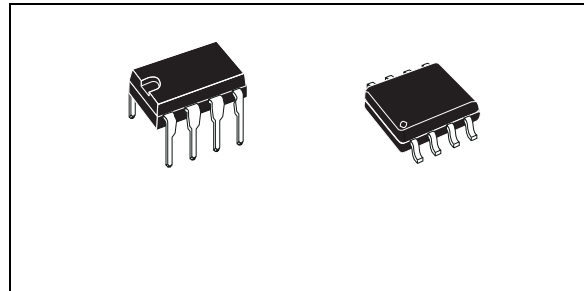


UC2842B/3B/4B/5B

UC3842B/3B/4B/5B

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLER

- TRIMMED OSCILLATOR FOR PRECISE FREQUENCY CONTROL
- OSCILLATOR FREQUENCY GUARANTEED AT 250kHz
- CURRENT MODE OPERATION TO 500kHz
- AUTOMATIC FEED FORWARD COMPENSATION **Minidip SO8**
- LATCHING PWM FOR CYCLE-BY-CYCLE CURRENT LIMITING
- INTERNALLY TRIMMED REFERENCE WITH UNDERVOLTAGE LOCKOUT

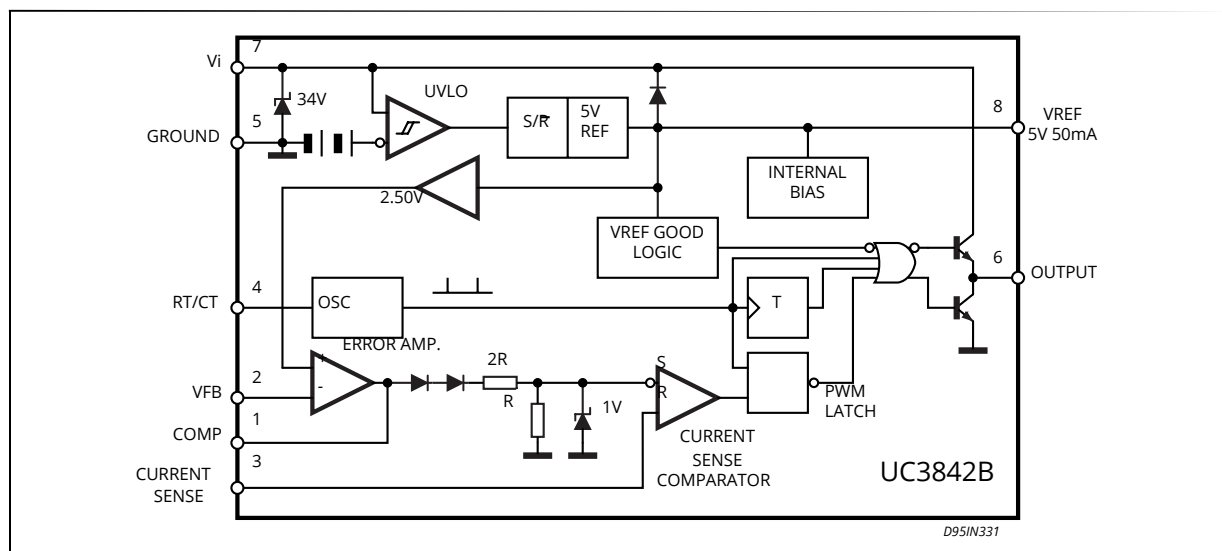


- HIGH CURRENT TOTEM POLE OUTPUT comparator which also provides current limit control, UNDERVOLTAGE LOCKOUT WITH HYSTER- and a totem pole output stage designed to source ESIS or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

DESCRIPTION

The UC384xB family of control ICs provides the necessary features to implement off-line or DC to DC conversion schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise frequency control, a current mode control scheme with automatic feed forward compensation, a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise frequency control, a current mode control scheme with automatic feed forward compensation, a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise frequency control, a current mode control scheme with automatic feed forward compensation, a minimal external parts count.

BLOCK DIAGRAM (toggle flip flop used only in UC3844B and UC3845B)



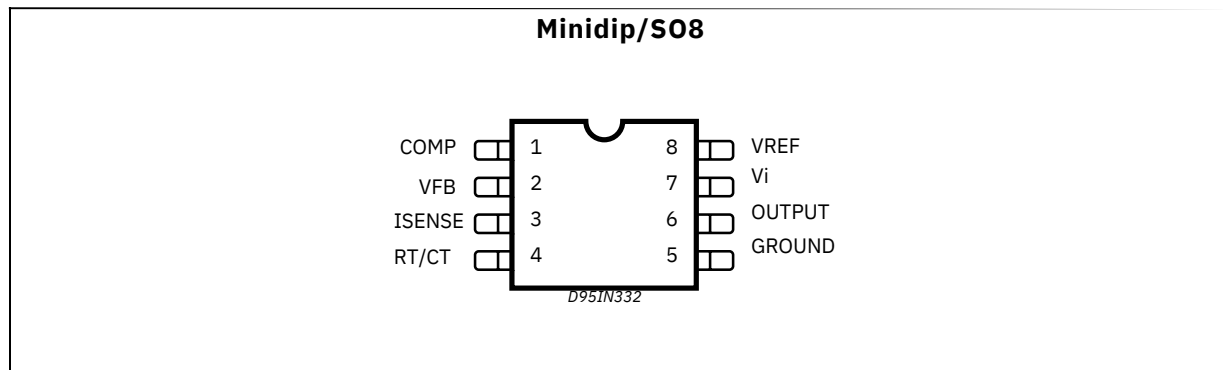
UC2842B/3B/4B/5B - UC3842B/3B/4B/5B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage ($I_i < 30\text{mA}$)	Self Limiting	
I_O	Output Current	± 1	A
E_O	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins 2, 3)	-0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (Minidip)	1.25	W
P_{tot}	Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (SO8)	800	mW
T_{st}	Storage Temperature Range	-65 to 150	$^\circ\text{C}$
T_{gJ}	Junction Operating Temperature	-40 to 150	$^\circ\text{C}$
T_L	Lead Temperature (soldering 10s)	300	$^\circ\text{C}$

*All voltages are with respect to pin 5, all currents are positive into the specified terminal.

PIN CONNECTION (top view)



PIN FUNCTIONS

No	Function	Description
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	VFB	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	ISENSE	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	RT/CT	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	VCC	This pin is the positive supply of the control IC.
8	Vref	This is the reference output. It provides charging current for capacitor CT through resistor RT.

ORDERING NUMBERS

SO8	Minidip
UC2842BD1; UC3842BD1 UC2843BD1; UC3843BD1 UC2844BD1; UC3844BD1 UC2845BD1; UC3845BD1	UC2842BN; UC3842BN UC2843BN; UC3843BN UC2844BN; UC3844BN UC2845BN; UC3845BN

THERMAL DATA

Symbol	Description	Minidip	SO8	Unit
$\theta_{Rth j-amb}$	Thermal Resistance Junction-ambient. max.100		150	°C/W

ELECTRICAL CHARACTERISTICS ([note 1] Unless otherwise stated, these specifications apply for $-25 \leq T_{amb} < 85^\circ\text{C}$ for UC284XB; $0 < T_{amb} < 70^\circ\text{C}$ for UC384XB; $V_i = 15\text{V}$ (note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$)

Symbol Parameter		Test Conditions			UC284XB			UC384XB			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.					
REFERENCE SECTION												
VREFOutput Voltage		Tj = 25°C Io = 1mA4.955.005.054.905.005.10V										
ΔVREFLine Regulation		12V ≤ Vi ≤ 25V220220mV										
ΔVREFLoad Regulation		1 ≤ Io ≤ 20mA325325mV										
ΔVREF/ΔT Temperature Stability		(Note 2)0.20.2mV/°C										
Total Output Variation		Line, Load, Temperature4.95.14.825.18V										
enOutput Noise Voltage		10Hz ≤ f ≤ 10KHz Tj = 25°C5050μV (note 2)										
Long Term Stability		Tamb = 125°C, 1000Hrs525525mV										
ISOutput Short Circuit		(note 2) -30 -100 -180 -30 -100 -180 mA										
OSCILLATOR SECTION												
fOSC Frequency												
Tj = 25°C TA = Tlow to Thigh		Tj = 25°C (RT = 6.2k, CT = 1nF)				49 48 22 5	52 - 250	55 56 27 5	49 48 22 5	52 - 250	55 56 27 5	KHz KHz KHz
ΔfOSC/ΔV Frequency Change with Volt. VCC = 12V to 25V						-	0.2	1	-	0.2	1	%
ΔfOSC/ΔT Frequency Change with Temp. TA = Tlow to Thigh						-	1	1	-	0.5	1	%
VOSC Oscillator Voltage Swing (peak to peak)						-	1.6	-	-	1.6	-	V
Idischg Discharge Current (VOSC = 2V) Tj = 25°C TA = Tlow to Thigh						-	8.3	-	-	8.3	-	mA mA
ERROR AMP SECTION												
V2 Input Voltage VPIN1 = 2.5V						2.45	2.5	2.55	2.42	2.5	2.58	V
Ib Input Bias Current VFB = 5V							0	-1		0	-2	μA
AVOL 2V ≤ Vo ≤ 4V						65	-0.1		65	-0.1		dB
BW/Unity Gain Bandwidth Tj = 25°C						0.7	90		0.7	90		MHz
PSRR Power Supply Rejec. Ratio 12V ≤ Vi ≤ 25V						60	1		60	1		dB
Io Output Sink Current VPIN2 = 2.7V VPIN1 = 1.1V						2	70		2	70		mA
Io Output Source Current VPIN2 = 2.3V VPIN1 = 5V						-0.5	12		-0.5	12		mA
VOUT High VPIN2 = 2.3V; RL = 15KΩ to Ground						5	-1		5	-1		V
VOUT Low VPIN2 = 2.7V; RL = 15KΩ to Pin 8							6.2			6.2		V
CURRENT SENSE SECTION												
GV Gain (note 3 & 4)							0.8	1.1		0.8		
V3 Maximum Input Signal VPIN1 = 5V (note 3)						2.8	3	3.1	2.8	3	3.1	V/V
SVR Supply Voltage Rejection 12 ≤ Vi ≤ 25V (note 3)						5	1	5	5	1	5	V
Ib Input Bias Current						0.9	70	1.1	0.9	70	1.1	dB
Delay to Output							-2	-10		-2	-10	μA
							15	30		15	30	ns
						0	0		0	0		

ELECTRICAL CHARACTERISTICS (continued)

Notes :

- 1.Max package power dissipation limits must be respected; low duty cycle pulse techniques are used during test mainly in Tj as close to Tamb as possible.
- 2.These parameters, although guaranteed, are not 100% tested in production.
- 3.Parameter measured at trip point of latch with VPIN2 = 0.
- 4.Gain defined as :

$$A = \frac{\Delta VPIN1}{\Delta VPIN3} \geq 0.8 \text{ V}$$
- 5.Adjust Vi above the start threshold before setting at 15 V.

Figure 4: Oscillator Discharge Current vs. Temperature.

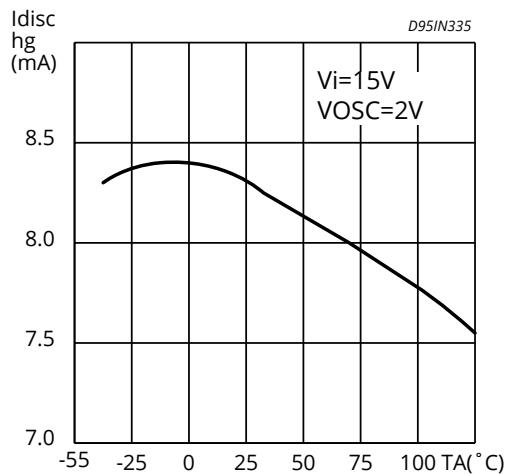


Figure 6: Error Amp Open-Loop Gain and Phase vs. Frequency.

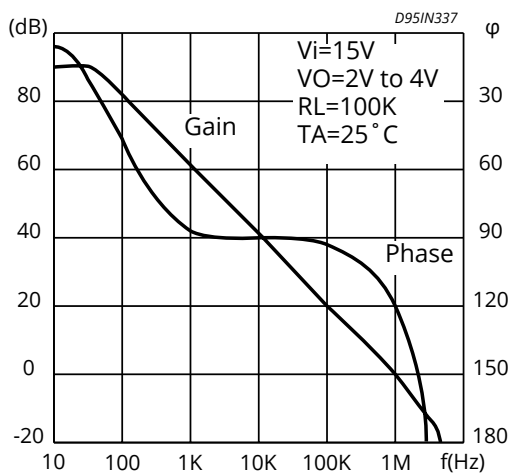


Figure 8: Reference Voltage Change vs. Source Current.

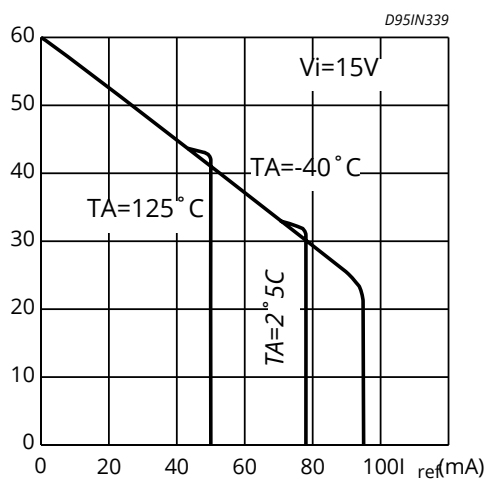


Figure 5: Maximum Output Duty Cycle vs. Timing Resistor.

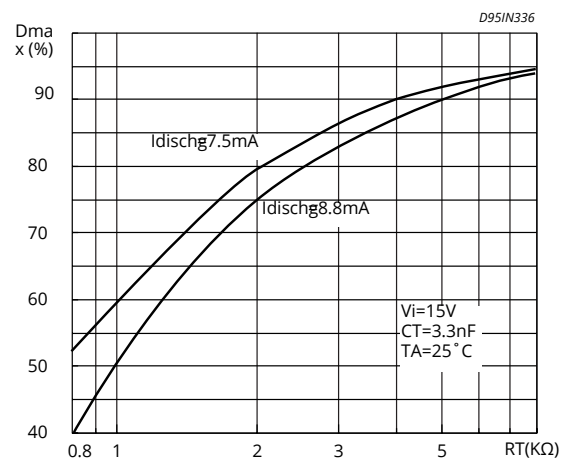


Figure 7: Current Sense Input Threshold vs. Error Amp Output Voltage.

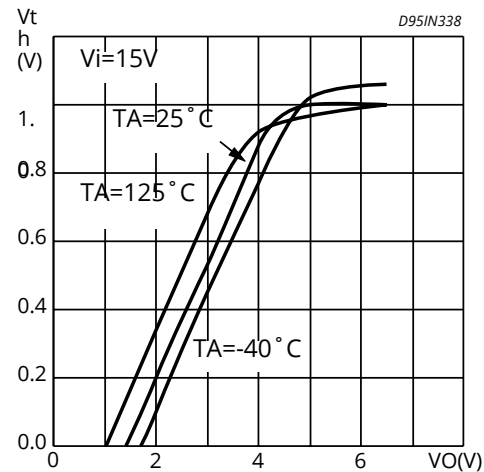


Figure 9: Reference Short Circuit Current vs. Temperature.

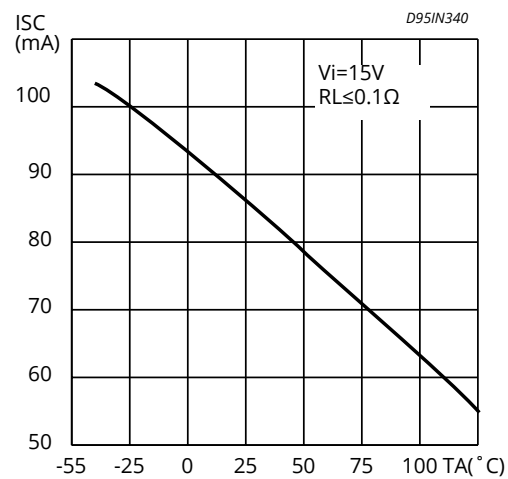


Figure 10: Output Saturation Voltages vs. Load Current.

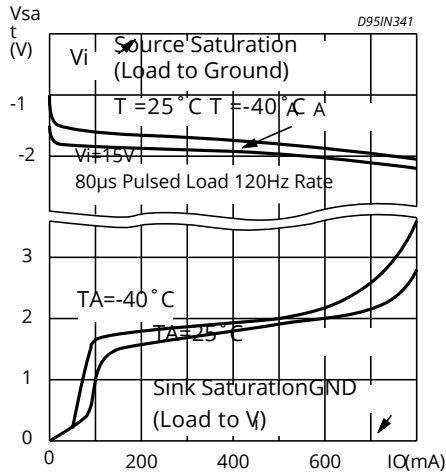


Figure 12: Output Waveform.

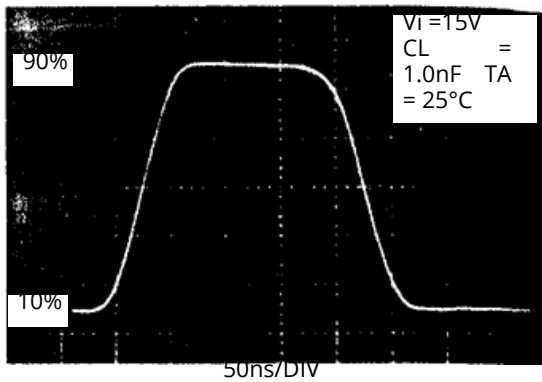


Figure 11: Supply Current vs. Supply Voltage.

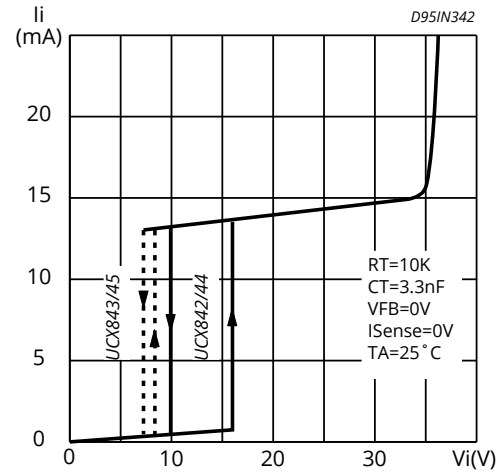


Figure 13: Output Cross Conduction

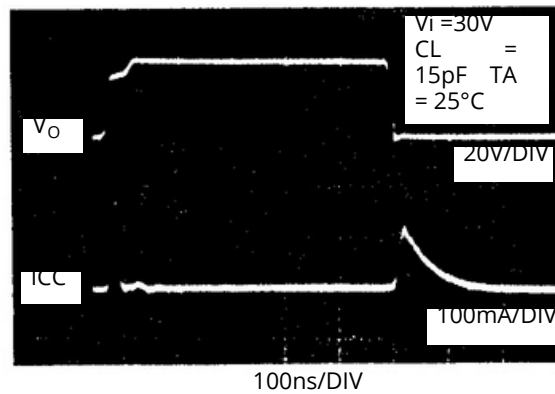
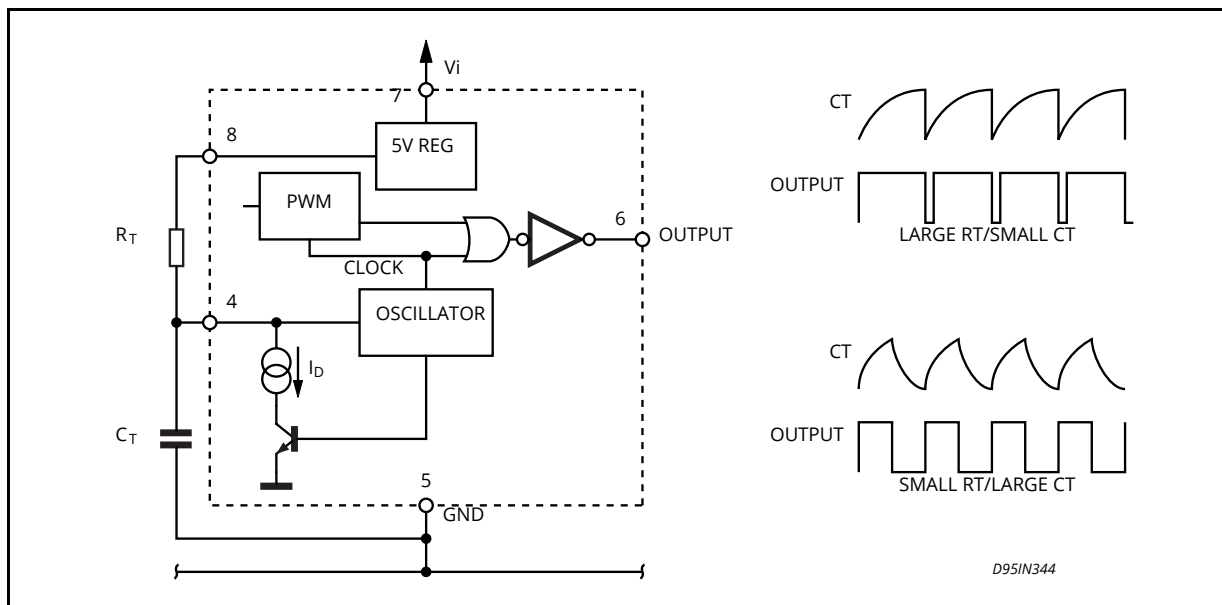


Figure 14: Oscillator and Output Waveforms.



UC2842B/3B/4B/5B - UC3842B/3B/4B/5B

Figure 15 : Error Amp Configuration.

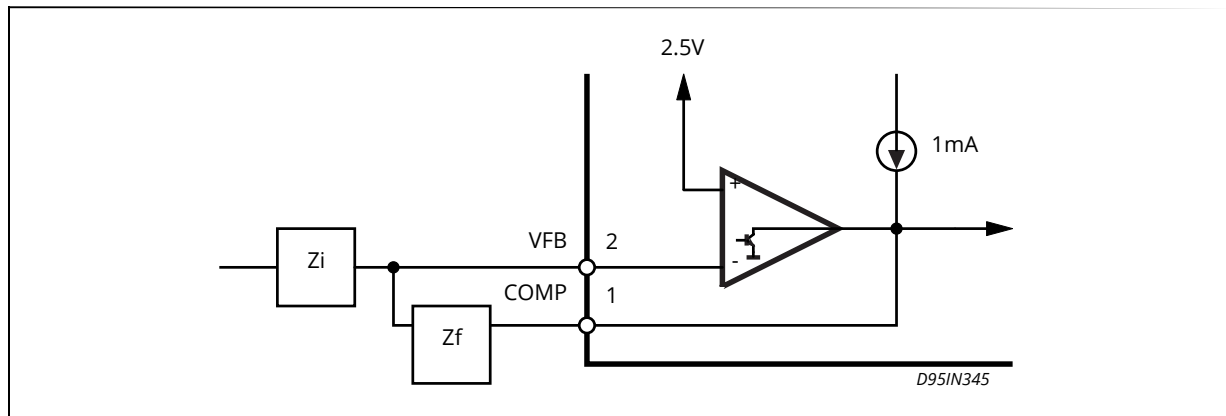


Figure 16 : Under Voltage Lockout.

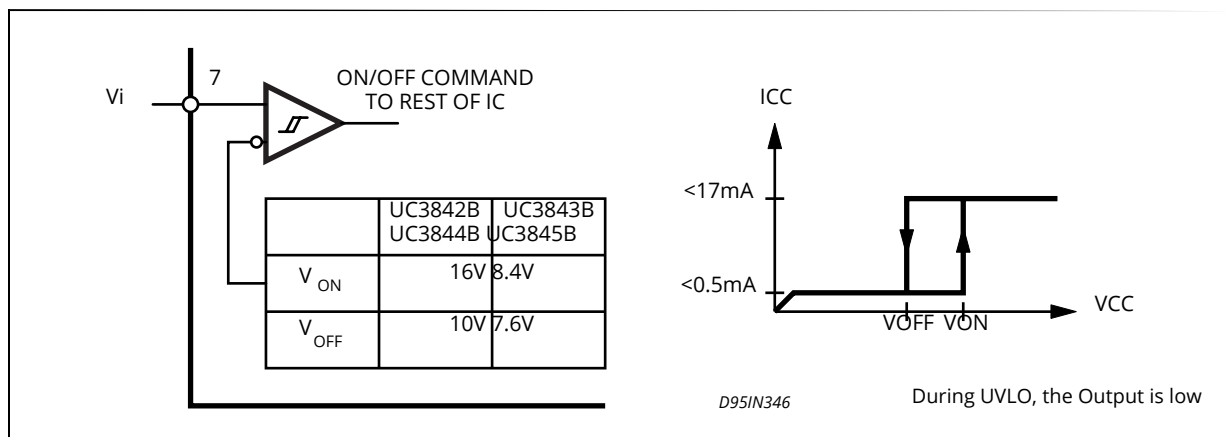
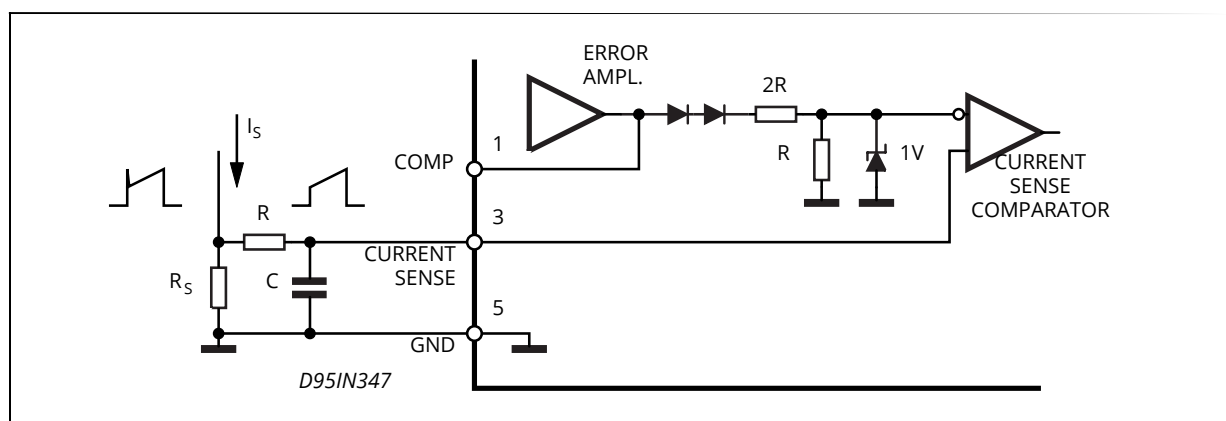


Figure 17 : Current Sense Circuit .



Peak current (i_s) is determined by the formula

$$I_{S \text{ max}} \approx \frac{1.0V}{R_S}$$

R_S

A small RC filter may be required to suppress switch transients.

Figure 18 : Slope Compensation Techniques.

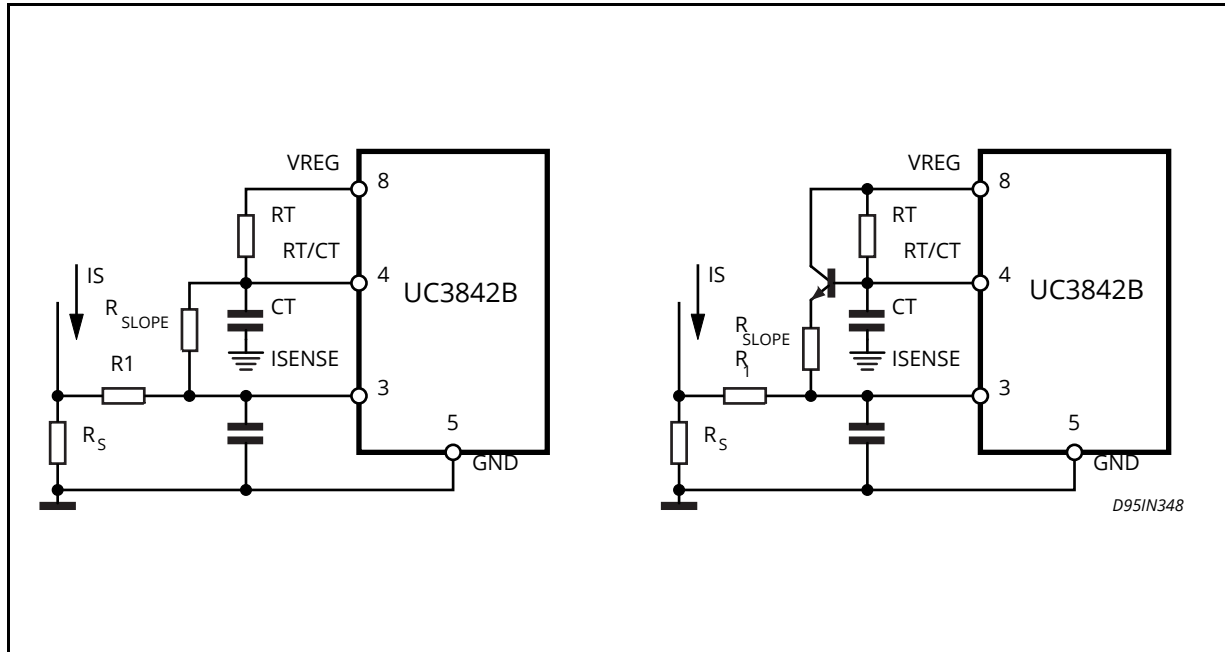


Figure 19 : Isolated MOSFET Drive and Current Transformer Sensing.

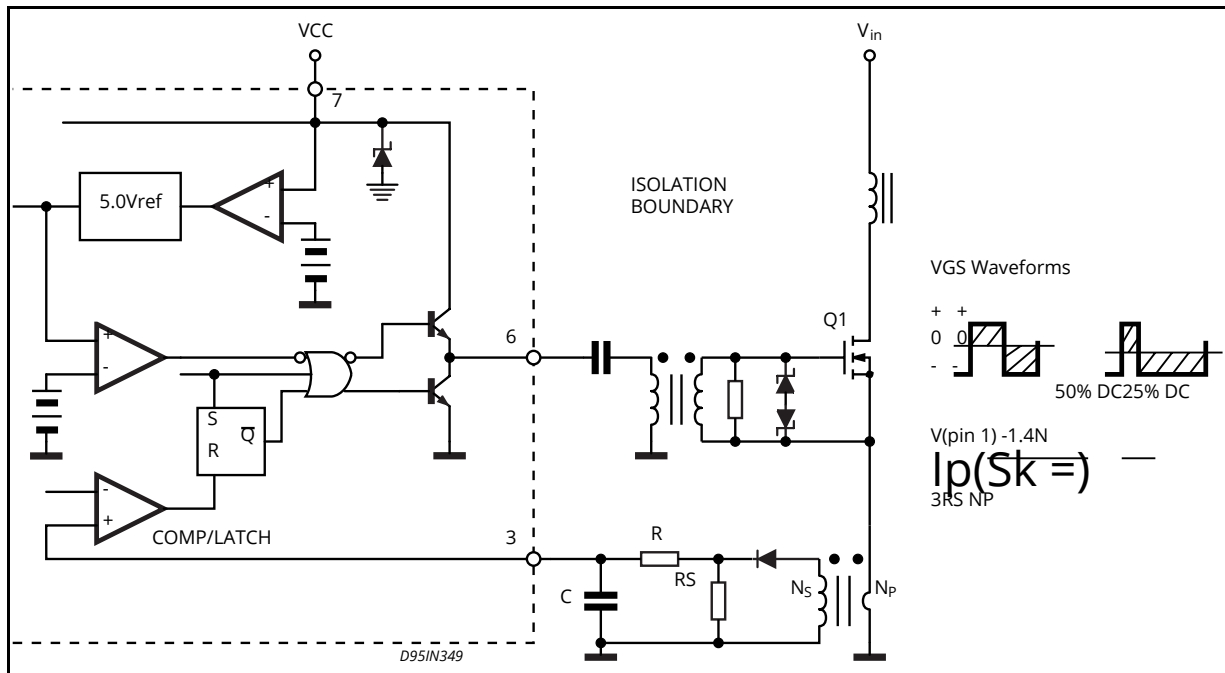


Figure 20 : Latched Shutdown.

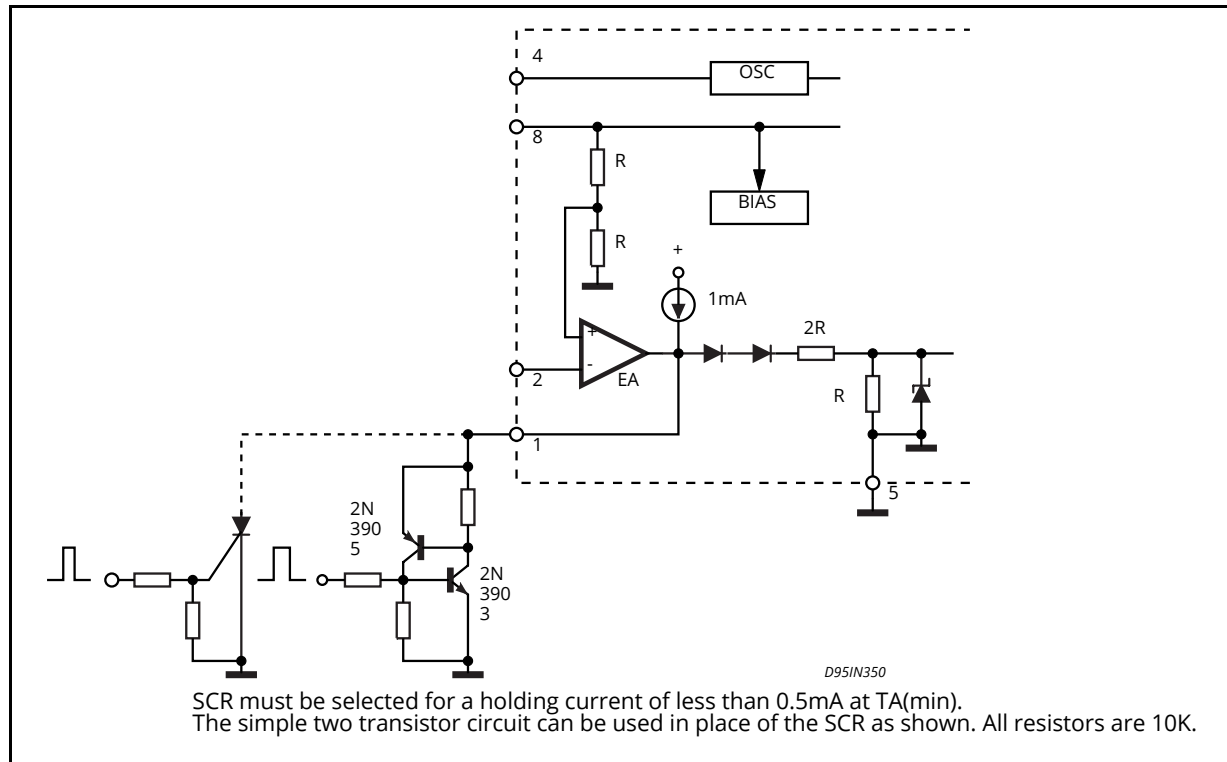


Figure 21: Error Amplifier Compensation

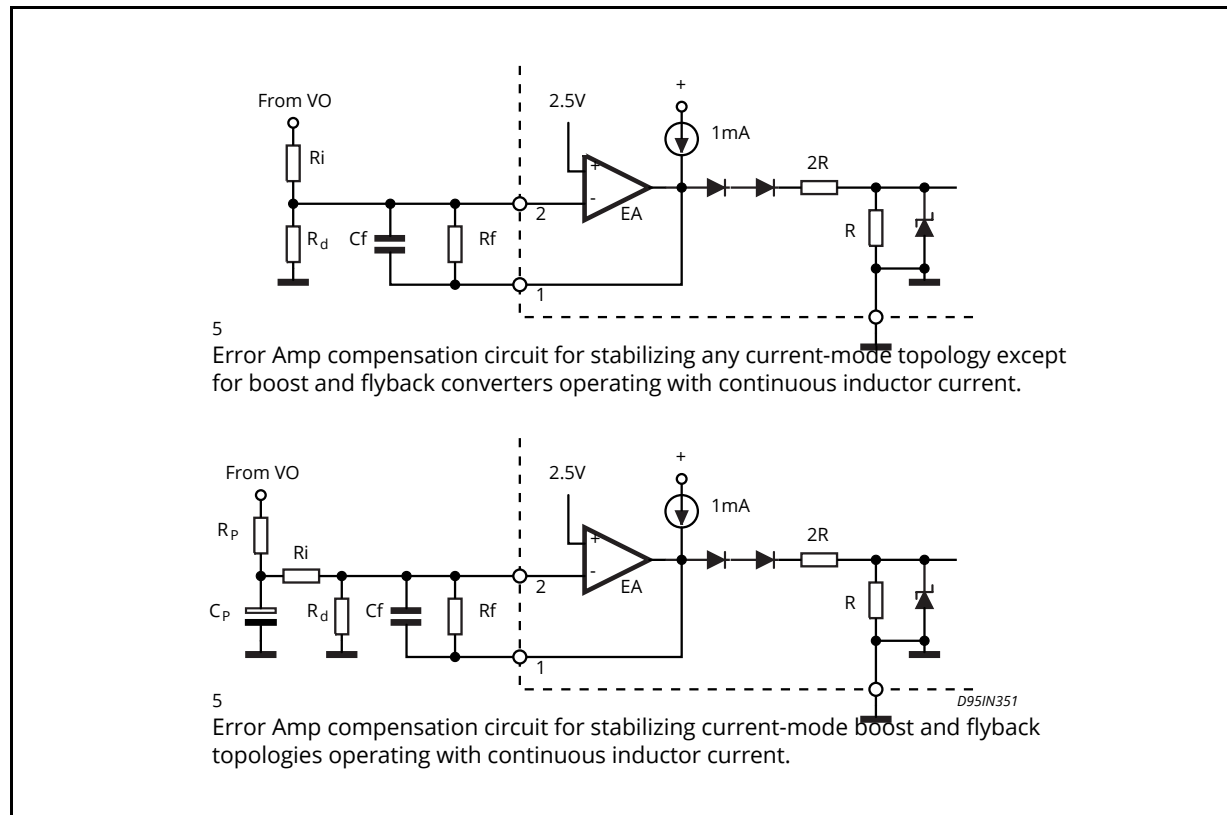


Figure 22: External Clock Synchronization.

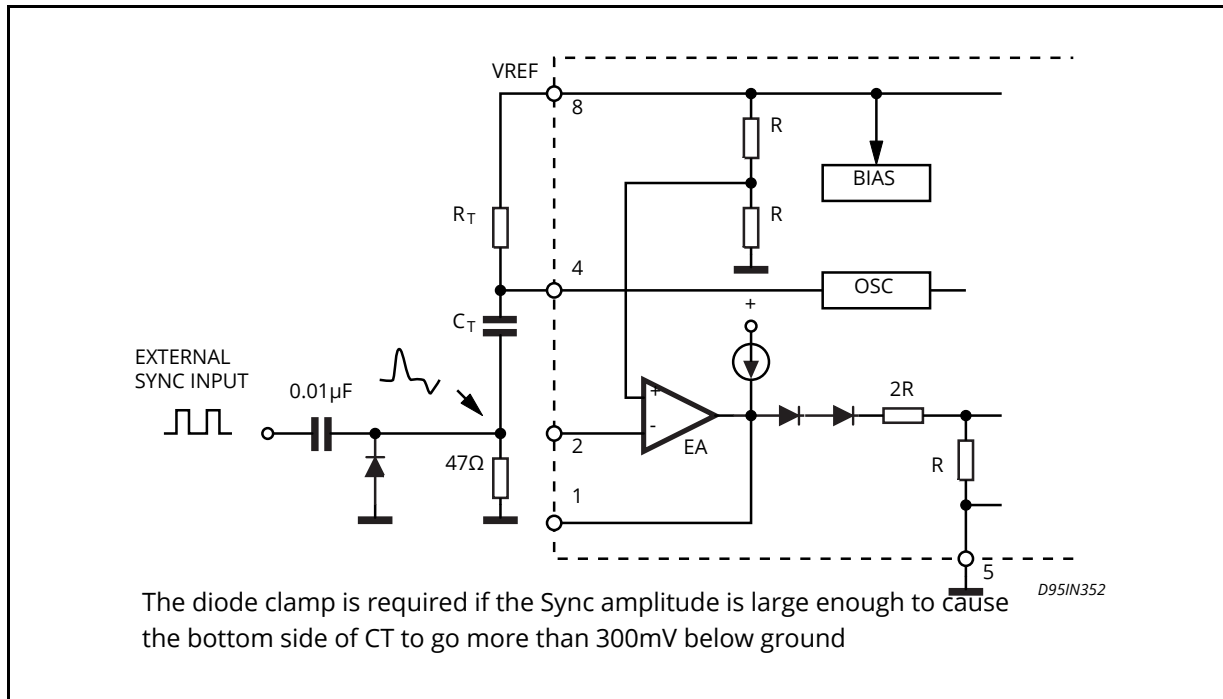
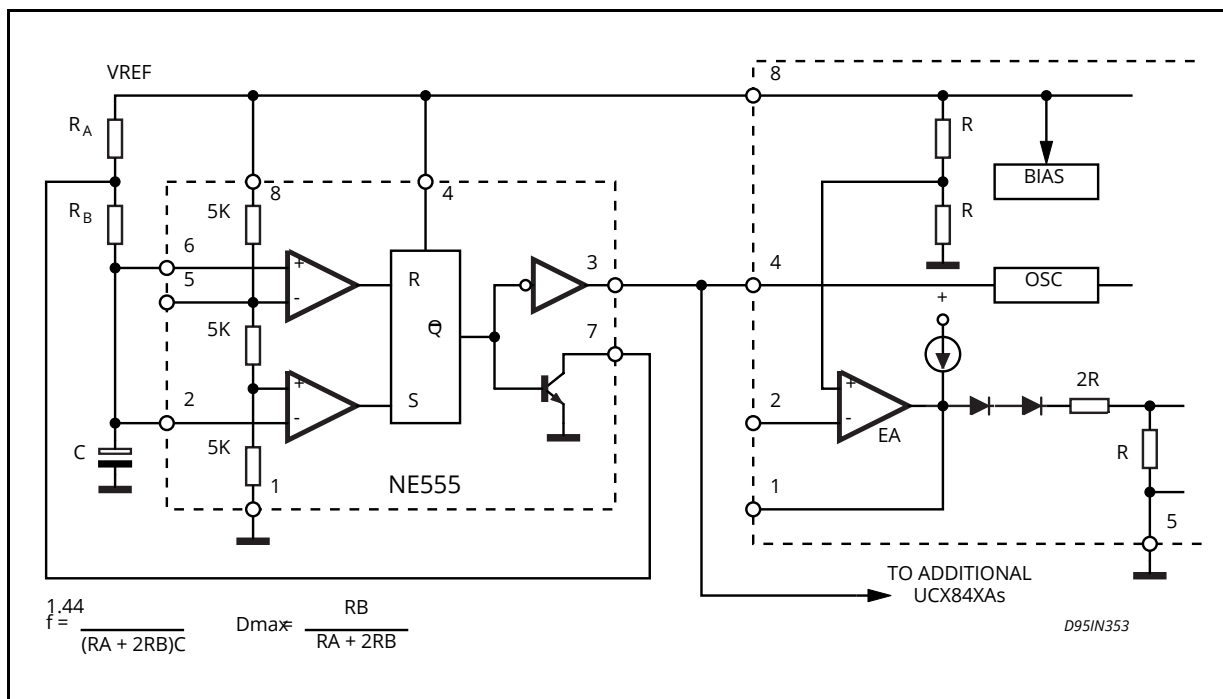


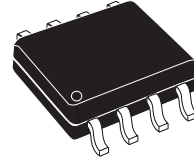
Figure 23: External Duty Cycle Clamp and Multi Unit Synchronization.



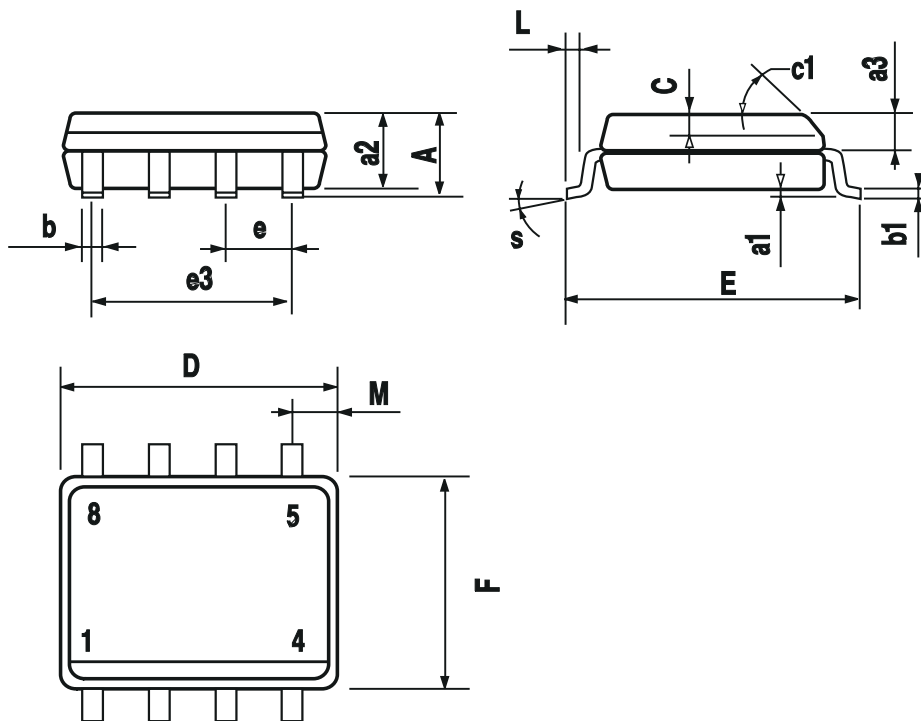
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189	6.2	0.197
E	5.8			0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15	1.27	0.157
L	0.4		0.016	0.6		0.050
M			8° (max.)			0.024
S						

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA



S08

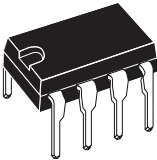


UC2842B/3B/4B/5B - UC3842B/3B/4B/5B

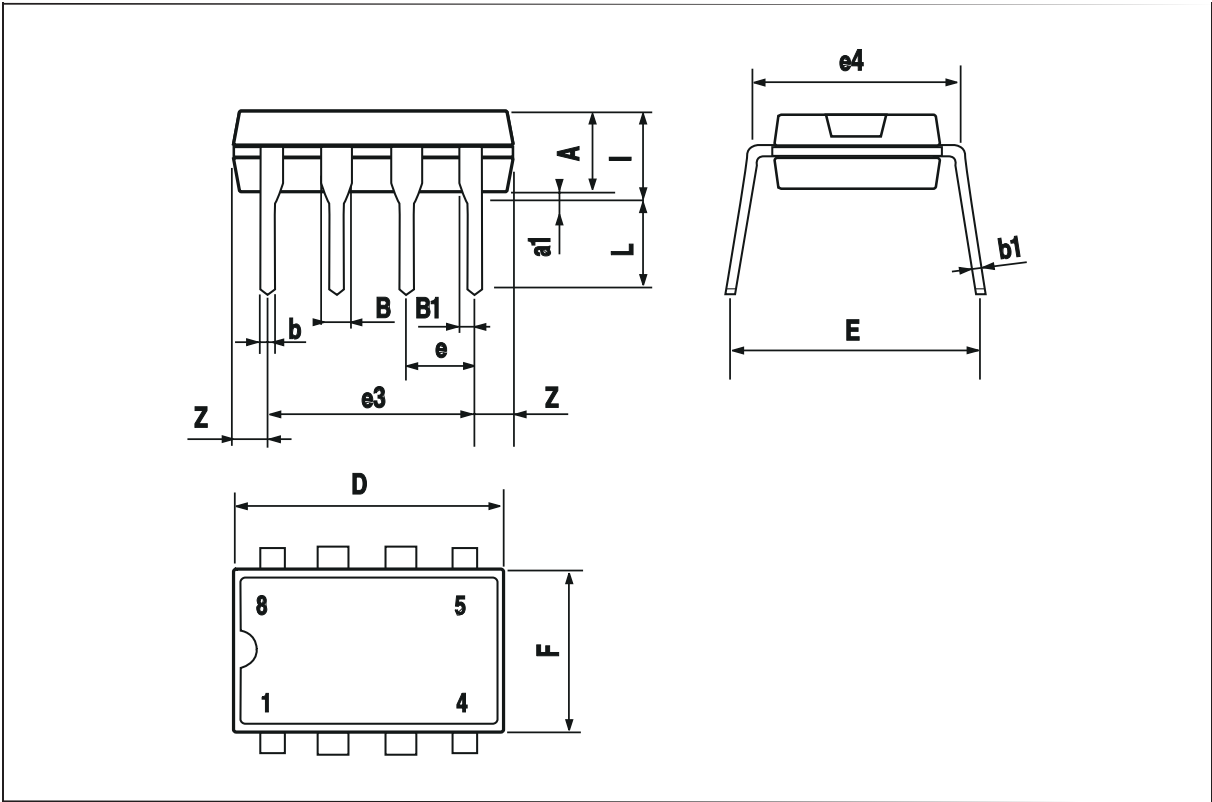
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b	0.204		0.304	0.008		0.012
1			10.92			0.430
D	7.95		9.75	0.313		0.384
E		2.54			0.100	
e		7.62			0.300	
e3		7.62			0.300	
e4			6.6			0.260
F			5.08			0.200
I	3.18		3.81	0.125		0.150
L			1.52			0.060

Z

OUTLINE AND MECHANICAL DATA



Minidip



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics
© 1999 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands -
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

http://www.st.com