



**24-Bit Delta Sigma A/D + LCD Flash MCU**

**HT67F5650/HT67F5660**

Revision: V1.50 Date: November 13, 2019

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## Table of Contents

<b>Features</b> .....	<b>7</b>
CPU Features .....	7
Peripheral Features.....	8
<b>General Description</b> .....	<b>9</b>
<b>Selection Table</b> .....	<b>9</b>
<b>Block Diagram</b> .....	<b>10</b>
<b>Pin Assignment</b> .....	<b>10</b>
<b>Pin Description</b> .....	<b>14</b>
<b>Absolute Maximum Ratings</b> .....	<b>19</b>
<b>D.C. Characteristics</b> .....	<b>20</b>
<b>A.C. Characteristics</b> .....	<b>23</b>
<b>LDO+PGA+ADC+VCM Electrical Characteristics</b> .....	<b>24</b>
<b>Comparator Electrical Characteristics</b> .....	<b>26</b>
<b>LCD Electrical Characteristics</b> .....	<b>27</b>
<b>Power-on Reset Characteristics</b> .....	<b>27</b>
<b>System Architecture</b> .....	<b>28</b>
Clocking and Pipelining.....	28
Program Counter.....	29
Stack .....	30
Arithmetic and Logic Unit – ALU .....	30
<b>Flash Program Memory</b> .....	<b>31</b>
Structure.....	31
Special Vectors .....	31
Look-up Table .....	32
Table Program Example.....	32
In Circuit Programming – ICP .....	33
On Chip Debug Support – OCDS .....	34
In Application Programming – IAP .....	35
<b>RAM Data Memory</b> .....	<b>44</b>
Structure .....	44
Data Memory Addressing.....	45
General Purpose Data Memory .....	45
Special Purpose Data Memory .....	45
<b>Special Function Register Description</b> .....	<b>48</b>
Indirect Addressing Registers – IAR0, IAR1, IAR2 .....	48
Memory Pointers – MP0, MP1L, MP1H, MP2L, MP2H.....	48
Program Memory Bank Pointer – PBP.....	50
Accumulator – ACC .....	50
Program Counter Low Register – PCL .....	50

Look-up Table Registers – TBLP, TBHP, TBLH .....	50
Status Register – STATUS .....	51
<b>EEPROM Data memory .....</b>	<b>53</b>
EEPROM Data Memory Structure .....	53
EEPROM Registers .....	53
Reading Data from the EEPROM .....	55
Writing Data to the EEPROM.....	55
Write Protection.....	55
EEPROM Interrupt .....	55
Programming Considerations.....	56
<b>Oscillators .....</b>	<b>57</b>
Oscillator Overview .....	57
System Clock Configurations .....	57
External Crystal/Ceramic Oscillator – HXT .....	58
Internal RC Oscillator – HIRC .....	59
Internal 32kHz Oscillator – LIRC .....	59
External 32.768kHz Crystal Oscillator – LXT .....	59
Supplementary Oscillators .....	60
<b>Operating Modes and System Clocks .....</b>	<b>61</b>
System Clocks .....	61
System Operation Modes .....	63
Control Register .....	64
Fast Wake-up .....	66
Operating Mode Switching .....	67
Standby Current Considerations .....	71
Wake-up .....	71
Programming Considerations .....	72
<b>Watchdog Timer.....</b>	<b>73</b>
Watchdog Timer Clock Source.....	73
Watchdog Timer Control Register .....	73
Watchdog Timer Operation .....	74
<b>Reset and Initialisation .....</b>	<b>76</b>
Reset Functions .....	76
Reset Initial Conditions .....	78
<b>Input/Output Ports .....</b>	<b>82</b>
Pull-high Resistors .....	82
Port A Wake-up .....	83
I/O Port Control Registers .....	84
I/O Pin Structures.....	85
Programming Considerations .....	85
<b>Timer Modules – TM .....</b>	<b>86</b>
Introduction .....	86
TM Operation .....	86
TM Clock Source.....	87

TM Interrupts .....	87
TM External Pins .....	87
TM Input/Output Pin Control Registers .....	88
Programming Considerations.....	89
<b>Compact Type TM – CTM (TM0).....</b>	<b>90</b>
Compact TM Operation .....	90
Compact Type TM Register Description.....	91
Compact Type TM Operating Modes .....	95
<b>Periodic Type TM – PTM (TM1, TM2).....</b>	<b>101</b>
Periodic TM Operation .....	101
Periodic Type TM Register Description.....	102
Periodic Type TM Operating Modes.....	106
<b>Standard Type TM – STM (TM3).....</b>	<b>115</b>
Standard TM Operation.....	115
Standard Type TM Register Description .....	116
Standard Type TM Operating Modes .....	120
<b>Internal Power Supply .....</b>	<b>130</b>
<b>Analog to Digital Converter – ADC.....</b>	<b>132</b>
A/D Overview .....	132
A/D Data Rate Definition.....	133
A/D Converter Register Description .....	133
Programmable Gain Amplifier – PGA.....	133
A/D Converter Data Registers – ADRL, ADRM, ADRH.....	135
A/D Converter Control Registers – ADCR0, ADCR1, ADCS.....	136
A/D Operation .....	138
Summary of A/D Conversion Steps.....	139
Programming Considerations.....	140
A/D Transfer Function .....	140
A/D Converted Data .....	141
A/D Converted data to voltage.....	141
A/D Programming Example.....	142
<b>Temperature sensor .....</b>	<b>143</b>
<b>Comparators .....</b>	<b>143</b>
Comparator Operation .....	143
Comparator Register.....	143
Comparator Interrupt.....	146
Programming Considerations.....	146
<b>Serial Interface Module – SIM.....</b>	<b>147</b>
SPI Interface .....	147
I <sup>2</sup> C Interface .....	153

<b>UART Module Serial Interface with IR Carrier .....</b>	<b>163</b>
UART Module Features.....	163
UART Module Overview.....	163
UART External Pin Interfacing .....	163
UART Data Transfer Scheme.....	164
UART Status and Control Registers.....	164
Baud Rate Generator .....	170
UART Setup and Control.....	171
UART Transmitter.....	173
UART Receiver .....	174
Managing Receiver Errors .....	175
UART Module Interrupt Structure.....	176
UART Module Power Down and Wake-up .....	178
IR Modulation Interface .....	178
<b>Interrupts .....</b>	<b>180</b>
Interrupt Registers.....	180
Interrupt Operation .....	185
External Interrupt.....	187
Comparator Interrupt.....	187
A/D Converter Interrupt.....	187
Multi-function Interrupt .....	188
Serial Interface Module Interrupt.....	188
Time Base Interrupts .....	189
I <sup>2</sup> C Time Out Interrupt .....	190
UART Interrupt .....	190
EEPROM Interrupt .....	190
LVD Interrupt.....	191
TM Interrupts.....	191
Interrupt Wake-up Function.....	191
Programming Considerations.....	192
<b>Low Voltage Detector – LVD .....</b>	<b>193</b>
LVD Register .....	193
LVD Operation.....	194
<b>LCD Driver .....</b>	<b>195</b>
LCD Display Memory .....	197
LCD Clock Source .....	197
LCD Registers.....	198
LCD Voltage Source and Biasing.....	201
LCD Driver Output.....	203
LCD Charge Pump.....	206
Programming Considerations.....	207
<b>Configuration Option.....</b>	<b>208</b>

<b>Application Circuits</b> .....	<b>209</b>
<b>Instruction Set</b> .....	<b>210</b>
Introduction .....	210
Instruction Timing .....	210
Moving and Transferring Data .....	210
Arithmetic Operations.....	210
Logical and Rotate Operation .....	211
Branches and Control Transfer .....	211
Bit Operations .....	211
Table Read Operations .....	211
Other Operations.....	211
<b>Instruction Set Summary</b> .....	<b>212</b>
Table Conventions.....	212
Extended Instruction Set.....	214
<b>Instruction Definition</b> .....	<b>216</b>
Extended Instruction Definition .....	225
<b>Package Information</b> .....	<b>232</b>
64-pin LQFP (7mm×7mm) Outline Dimensions .....	233
80-pin LQFP (10mm×10mm) Outline Dimensions .....	234

## Features

### CPU Features

- Operating Voltage
  - ◆  $f_{SYS}=8\text{MHz}$ : 2.2V~5.5V
  - ◆  $f_{SYS}=12\text{MHz}$ : 2.7V~5.5V
  - ◆  $f_{SYS}=16\text{MHz}$ : 3.3V~5.5V
  - ◆  $f_{SYS}=20\text{MHz}$ : 4.5V~5.5V
- Up to 0.2 $\mu\text{s}$  instruction cycle with 20MHz system clock at  $V_{DD}=5\text{V}$
- Power down and wake-up functions to reduce power consumption
- Four oscillators
  - ◆ External Crystal – HXT
  - ◆ External 32.768kHz Crystal – LXT
  - ◆ Internal RC – HIRC
  - ◆ Internal 32kHz RC – LIRC
- Multi-mode operation: NORMAL, SLOW, IDLE and SLEEP
- Fully integrated internal 4.9152MHz, 4.9152 $\times$ 2MHz and 4.9152 $\times$ 3MHz oscillator requires no external components
- All instructions executed in 1~3 instruction cycles
- Table read instructions
- 115 powerful instructions
- 8-level subroutine nesting
- Bit manipulation instruction

### Peripheral Features

- Flash Program Memory: 8K×16 ~ 16K×16
- RAM Data Memory: 512×8 ~ 1024×8
- True EEPROM Memory: 128×8 ~ 256×8
- In Application Programming function – IAP
- Watchdog Timer function
- LCD COM driver with 1/3 bias
- Up to 32 bidirectional I/O lines
- 4 pin-shared external interrupts
- Multiple Timer Modules for time measure, input capture, compare match output, PWM output or single pulse output function
- Dual Time-Base functions for generation of fixed time interrupt signals
- 2 differential and 4 single-end channels 24-bit resolution Delta Sigma A/D converter
- Low voltage reset function
- Low voltage detect function
- Internal LDO with bypass function for PGA, ADC or external sensor power supply
- Serial Interfaces Module -- SIM for SPI or I<sup>2</sup>C
- UART with IR carrier
- Two comparators
- Flash program memory can be re-programmed up to 10,000 times
- Flash program memory data retention > 10 years
- True EEPROM data memory can be re-programmed up to 100,000 times
- True EEPROM data memory data retention > 10 years
- Package type: 64-pin LQFP and 80-pin LQFP

## General Description

This series of devices are Flash Memory A/D type 8-bit high performance RISC architecture microcontrollers which include a multi-channel 24-bit Delta Sigma A/D converter and fully integrated LCD driver. The devices are there suitable for use in products which require a low noise and high accuracy analog to digital converter and which also need to drive LCD panels. Offering users the convenience of Flash Memory multi-programming features, these devices also include a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of true EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc.

Analog features include a multi-channel with 24-bit Delta Sigma A/D converter and programmable gain amplifier (PGA) functions. An extremely flexible Timer Module provides timing, pulse generation and PWM generation functions. Communication with the outside world is catered for by including fully integrated SPI or I<sup>2</sup>C interface functions, two popular interfaces which provide designers with a means of easy communication with external peripheral hardware. In addition, an internal LDO function provides various power options to the internal and external devices. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

A full choice of HXT, LXT, HIRC and LIRC oscillator functions are provided including a fully integrated system oscillator which requires no external components for its implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimise microcontroller operation and minimise power consumption.

The inclusion of flexible I/O programming features, a fully integrated LCD driver and Time-Base functions along with many other features ensure that the devices will find excellent use in applications such as weight scales, electronic metering, environmental monitoring, handheld instruments, household appliances, electronically controlled tools, motor driving in addition to many others.

## Selection Table

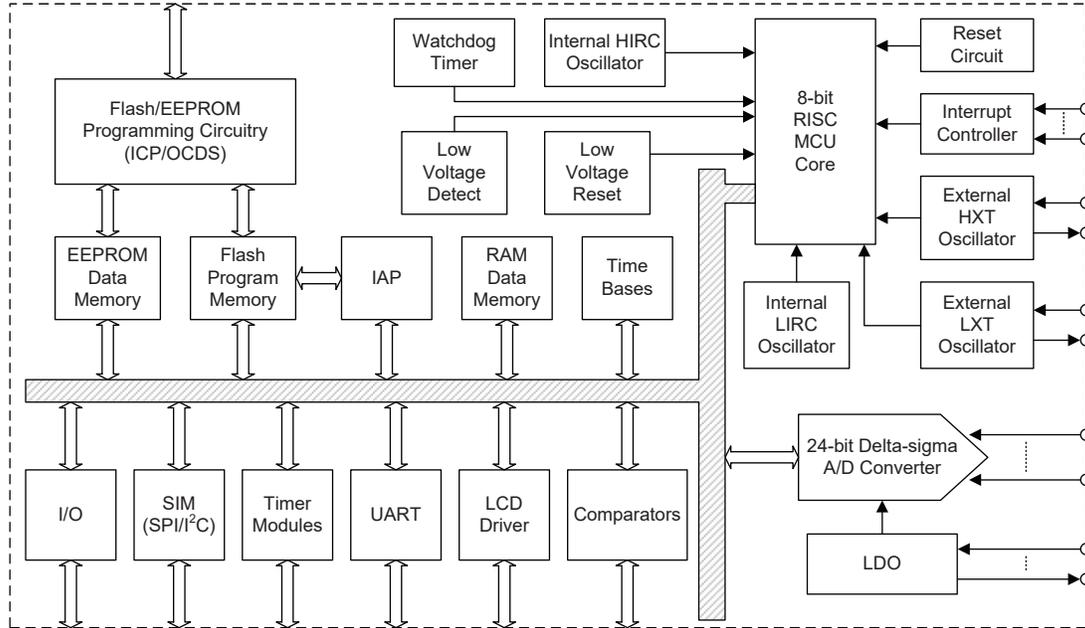
Most features are common to all devices, the main feature distinguishing them are Memory capacity and the number of LCD driver output. The following table summarises the main features of each device.

Part No.	Program Memory	Data Memory	Data EEPROM	I/O	External Interrupt	A/D Converter	Timer Module
HT67F5650	8K×16	512×8	128×8	32	4	24-bit×8	10-bit CTM×1 10-bit PTM×2 16-bit STM×1
HT67F5660*	16K×16	1024×8	256×8	32	4	24-bit×8	10-bit CTM×1 10-bit PTM×2 16-bit STM×1

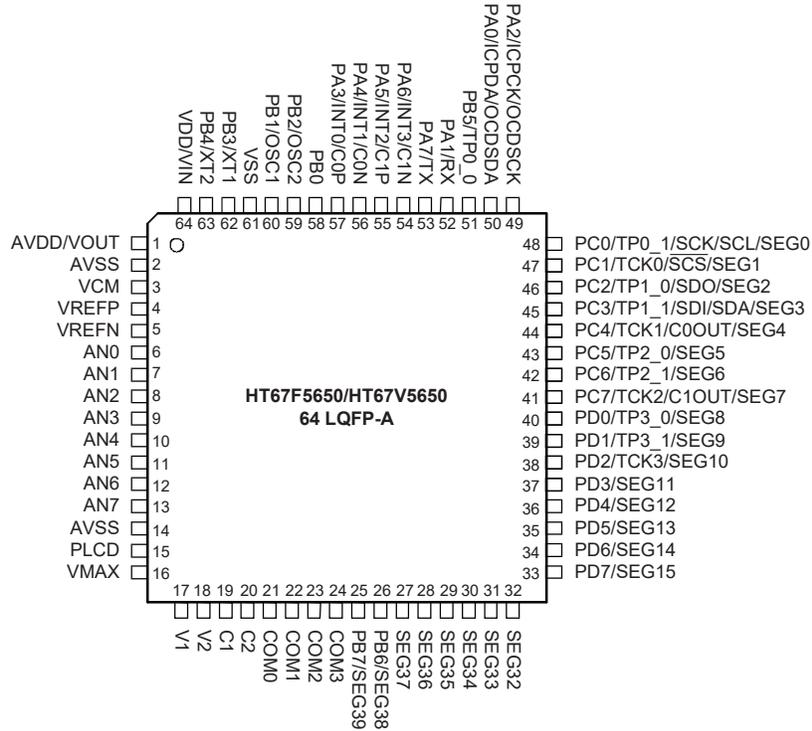
Part No.	Time Base	SIM	UART	LCD Driver	LDO	PGA	Comparator	Stack	Package
HT67F5650	2	√	√	40×4	√	√	2	8	64/80LQFP
HT67F5660	2	√	√	48×4	√	√	2	8	64/80LQFP

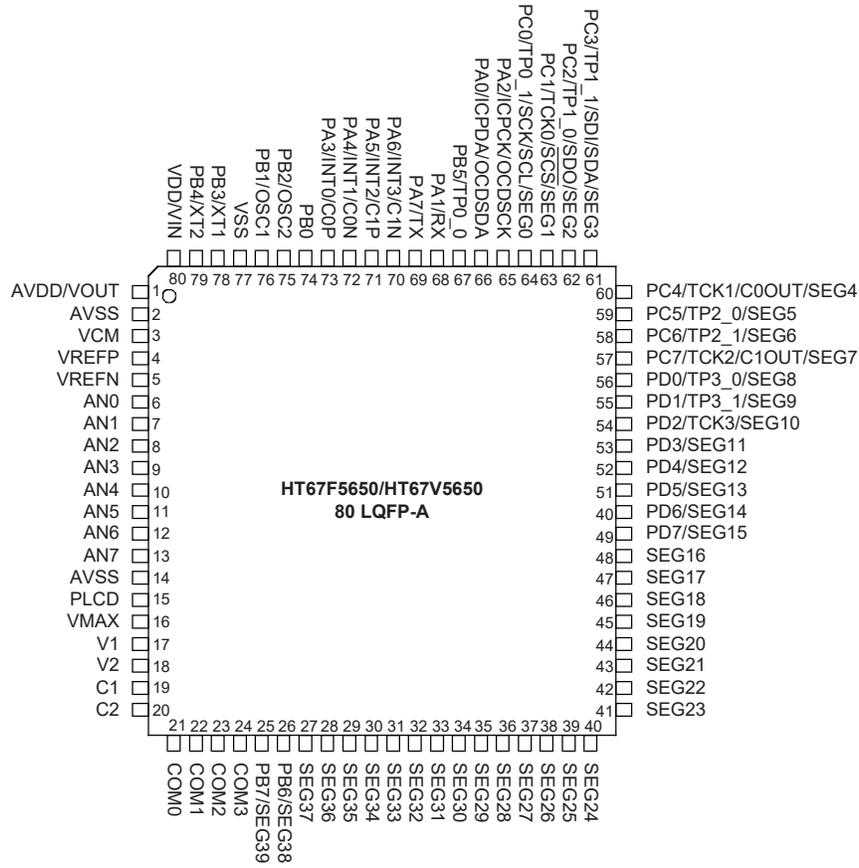
Note: As devices exist in more than one package format, the table reflects the situation for the package with the most pins.

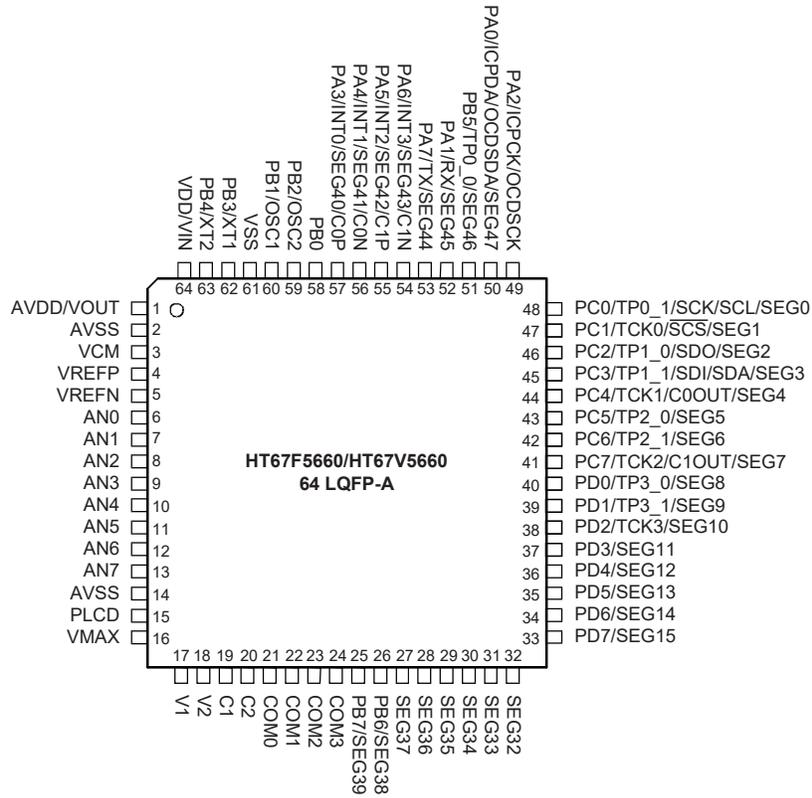
### Block Diagram

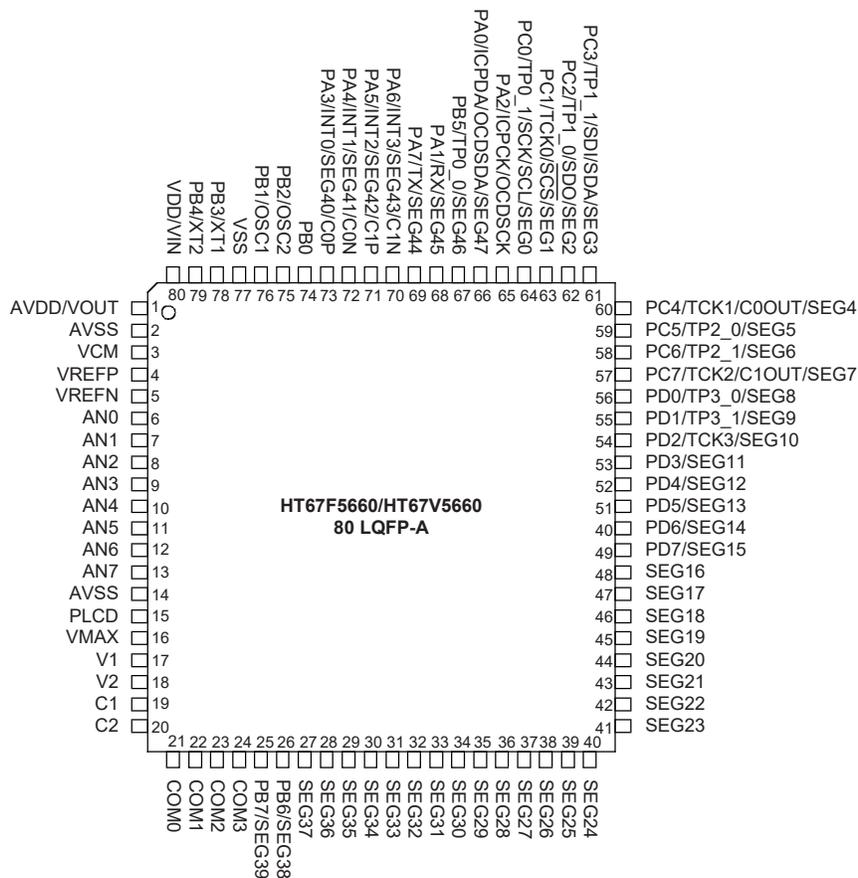


### Pin Assignment









- Note: 1. If the pin-shared pin functions have multiple outputs simultaneously, its pin names at the right side of the "/" sign can be used for higher priority.
2. The OCSDA and OCDSCCK pins are the OCDS dedicated pins and only available for the HT67V5650/HT67V5660 device which is the OCDS EV chip for the HT67F5650/HT67F5660 device.
3. For less pin-count package types there will be unbonded pins which should be properly configured to avoid unwanted current consumption resulting from floating input conditions. Refer to the "Standby Current Considerations" and "Input/Output Ports" sections.

## Pin Description

The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet.

### HT67F5650

Pin Name	Function	OPT	I/T	O/T	Descriptions
PA0/ICPDA/ OCDSDA	PA0	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	ICPDA	—	ST	CMOS	ICP address/data
	OCDSDA	—	ST	CMOS	OCDS address/data, for EV chip only.
PA1/RX	PA1	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	RX	—	ST	—	UART receiver pin
PA2/ICPCK/ OCDSCK	PA2	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	ICPCK	—	ST	—	ICP clock
	OCDSCK	—	ST	—	OCDS clock, for EV chip only.
PA3/INT0/C0P	PA3	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT0	—	ST	—	External Interrupt 0 input
	C0P	CP0C	AN	—	Comparator 0 positive input
PA4/INT1/C0N	PA4	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT1	—	ST	—	External Interrupt 1 input
	C0N	CP0C	AN	—	Comparator 0 negative input
PA5/INT2/C1P	PA5	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT2	—	ST	—	External Interrupt 2 input
	C1P	CP1C	AN	—	Comparator 1 positive input
PA6/INT3/C1N	PA6	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT3	—	ST	—	External Interrupt 3 input
	C1N	CP1C	AN	—	Comparator 1 negative input
PA7/TX	PA7	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	TX	—	—	CMOS	UART transceiver pin
PB0	PB0	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
PB1/OSC1	PB1	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	OSC1	CO	HXT	—	HXT Oscillator input
PB2/OSC2	PB2	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	OSC2	CO	—	HXT	HXT Oscillator output
PB3/XT1	PB3	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	XT1	CO	LXT	—	LXT Oscillator input
PB4/XT2	PB4	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	XT2	CO	—	LXT	LXT Oscillator output
PB5/TP0_0	PB5	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP0_0	CTRL0 TM0CO	—	CMOS	TM0 (10-bit CTM) output

Pin Name	Function	OPT	I/T	O/T	Descriptions
PC0/TP0_1/ SCK/SCL/SEG0	PC0	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP0_1	CTRL0 TM0C0	—	CMOS	TM0 (10-bit CTM) output
	SCK	SIMC2	ST	CMOS	SPI serial clock
	SCL	SIMC0	ST	CMOS	I <sup>2</sup> C clock line
	SEG0	LCD1	—	SEG	LCD Segment output
PC1/TCK0/ $\overline{\text{SCS}}$ / SEG1	PC1	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TCK0	—	ST	—	TM0 (10-bit CTM) clock input
	$\overline{\text{SCS}}$	SIMC2	ST	CMOS	SPI slave select pin
	SEG1	LCD1	—	SEG	LCD Segment output
PC2/TP1_0/ SDO/SEG2	PC2	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP1_0	CTRL0 PTM1C0	ST	CMOS	TM1 (10-bit PTM) input/output
	SDO	SIMC2	—	CMOS	SPI serial data output
	SEG2	LCD1	—	SEG	LCD Segment output
PC3/TP1_1/ SDI/SDA/SEG3	PC3	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP1_1	CTRL0 PTM1C0	ST	CMOS	TM1 (10-bit PTM) input/output
	SDI	SIMC2	ST	—	SPI serial data input
	SDA	SIMC0	ST	CMOS	I <sup>2</sup> C data line
	SEG3	LCD1	—	SEG	LCD Segment output
PC4/TCK1/ C0OUT/SEG4	PC4	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TCK1	—	ST	—	TM1 (10-bit PTM) clock input
	C0OUT	CP0C	—	CMOS	Comparator 0 output pin
	SEG4	LCD1	—	SEG	LCD Segment output
PC5/TP2_0/ SEG5	PC5	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP2_0	CTRL0 PTM2C0	ST	CMOS	TM2 (10-bit PTM) input/output
PC6/TP2_1/ SEG6	PC6	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP2_1	CTRL0 PTM2C0	ST	CMOS	TM2 (10-bit PTM) input/output
	SEG6	LCD1	—	SEG	LCD Segment output
PC7/TCK2/ C1OUT/SEG7	PC7	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TCK2	—	ST	—	TM2 (10-bit PTM) clock input
	C1OUT	CP1C	—	CMOS	Comparator 1 output pin
	SEG7	LCD1	—	SEG	LCD Segment output
PD0/TP3_0/ SEG8	PD0	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP3_0	CTRL0 STM3C0	ST	CMOS	TM3 (16-bit STM) input/output
PD1/TP3_1/ SEG9	PD1	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP3_1	CTRL0 STM3C0	ST	CMOS	TM3 (16-bit STM) input/output
	SEG9	LCD2	—	SEG	LCD Segment output
PD2/TCK3/ SEG10	PD2	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TCK3	—	ST	—	TM3 (16-bit STM) clock input
	SEG10	LCD2	—	SEG	LCD Segment output
PD3/SEG11	PD3	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG11	LCD2	—	SEG	LCD Segment output

Pin Name	Function	OPT	I/T	O/T	Descriptions
PD4/SEG12	PD4	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG12	LCD2	—	SEG	LCD Segment output
PD5/SEG13	PD5	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG13	LCD2	—	SEG	LCD Segment output
PD6/SEG14	PD6	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG14	LCD2	—	SEG	LCD Segment output
PD7/SEG15	PD7	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG15	LCD2	—	SEG	LCD Segment output
SEG16~SEG37	SEGn	—	—	SEG	LCD Segment output
PB6/SEG38	PB6	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG38	LCD3	—	SEG	LCD Segment output
PB7/SEG39	PB7	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG39	LCD3	—	SEG	LCD Segment output
COM0~COM3	COMn	—	—	COM	LCD Common output
V1, V2	V1, V2	—	AN	—	LCD voltage pump
C1, C2	C1, C2	—	AN	—	LCD voltage pump
PLCD	PLCD	—	PWR	—	LCD power supply
VMAX	VMAX	—	PWR	—	IC maximum voltage, connect to VDD or V1
AN0~AN7	ANn	—	AN	—	ADC input channel
VREFP	VREFP	—	PWR	—	ADC positive reference input
VREFN	VREFN	—	PWR	—	ADC negative reference input
VCM	VCM	—	—	PWR	ADC internal Common mode voltage output
VDD/VIN	VDD	—	PWR	—	Digital positive power supply
	VIN	—	PWR	—	LDO input pin
AVDD/VOUT	AVDD	—	PWR	—	Analog power supply
	VOUT	—	—	PWR	LDO output pin
VSS	VSS	—	PWR	—	Digital negative power supply
AVSS	AVSS	—	PWR	—	A/D negative power supply

**HT67F5660**

Pin Name	Function	OPT	I/T	O/T	Descriptions
PA0/ICPDA/ OCSDA/ SEG47	PA0	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	ICPDA	—	ST	CMOS	ICP address/data
	OCSDA	—	ST	CMOS	OCDS address/data, for EV chip only.
	SEG47	LCD4	—	SEG	LCD Segment output
PA1/RX/SEG45	PA1	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	RX	—	ST	—	UART receiver pin
	SEG45	LCD4	—	SEG	LCD Segment output
PA2/ICPCK/ OCDSCK	PA2	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	ICPCK	—	ST	—	ICP clock
	OCDSCK	—	ST	—	OCDS clock, for EV chip only.
PA3/INT0/ SEG40/COP	PA3	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT0	—	ST	—	External Interrupt 0 input
	SEG40	LCD4	—	SEG	LCD Segment output
	COP	CP0C	AN	—	Comparator 0 positive input

Pin Name	Function	OPT	I/T	O/T	Descriptions
PA4/INT1/ SEG41/CON	PA4	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT1	—	ST	—	External Interrupt 1 input
	SEG41	LCD4	—	SEG	LCD Segment output
	C0N	CP0C	AN	—	Comparator 0 negative input
PA5/INT2/ SEG42/C1P	PA5	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT2	—	ST	—	External Interrupt 2 input
	SEG42	LCD4	—	SEG	LCD Segment output
	C1P	CP1C	AN	—	Comparator 1 positive input
PA6/INT3/ SEG43/C1N	PA6	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	INT3	—	ST	—	External Interrupt 3 input
	SEG43	LCD4	—	SEG	LCD Segment output
	C1N	CP1C	AN	—	Comparator 1 negative input
PA7/TX/SEG44	PA7	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	TX	—	—	CMOS	UART transceiver pin
	SEG44	LCD4	—	SEG	LCD Segment output
PB0	PB0	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
PB1/OSC1	PB1	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	OSC1	CO	HXT	—	HXT Oscillator input
PB2/OSC2	PB2	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	OSC2	CO	—	HXT	HXT Oscillator output
PB3/XT1	PB3	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	XT1	CO	LXT	—	LXT Oscillator input
PB4/XT2	PB4	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	XT2	CO	—	LXT	LXT Oscillator output
PB5/TP0_0/ SEG46	PB5	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP0_0	CTRL0 TM0C0	—	CMOS	TM0 (10-bit CTM) output
	SEG46	LCD4	—	SEG	LCD Segment output
PC0/TP0_1/ SCK/SCL/ SEG0	PC0	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP0_1	CTRL0 TM0C0	—	CMOS	TM0 (10-bit CTM) output
	SCK	SIMC2	ST	CMOS	SPI serial clock
	SCL	SIMC0	ST	CMOS	I <sup>2</sup> C clock line
	SEG0	LCD1	—	SEG	LCD Segment output
PC1/TCK0/SCS/ SEG1	PC1	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TCK0	—	ST	—	TM0 (10-bit CTM) clock input
	SCS	SIMC2	ST	CMOS	SPI slave select pin
	SEG1	LCD1	—	SEG	LCD Segment output
PC2/TP1_0/ SDO/SEG2	PC2	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP1_0	CTRL0 PTM1C0	ST	CMOS	TM1 (10-bit PTM) input/output
	SDO	SIMC2	—	CMOS	SPI serial data output
	SEG2	LCD1	—	SEG	LCD Segment output

Pin Name	Function	OPT	I/T	O/T	Descriptions
PC3/TP1_1/ SDI/SDA/SEG3	PC3	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP1_1	CTRL0 PTM1C0	ST	CMOS	TM1 (10-bit PTM) input/output
	SDI	SIMC2	ST	—	SPI serial data input
	SDA	SIMC0	ST	CMOS	I <sup>2</sup> C data line
	SEG3	LCD1	—	SEG	LCD Segment output
PC4/TCK1/ C0OUT/SEG4	PC4	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TCK1	—	ST	—	TM1 (10-bit PTM) clock input
	C0OUT	CP0C	—	CMOS	Comparator 0 output pin
	SEG4	LCD1	—	SEG	LCD Segment output
PC5/TP2_0/ SEG5	PC5	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP2_0	CTRL0 PTM2C0	ST	CMOS	TM2 (10-bit PTM) input/output
	SEG5	LCD1	—	SEG	LCD Segment output
PC6/TP2_1/ SEG6	PC6	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TP2_1	CTRL0 PTM2C0	ST	CMOS	TM2 (10-bit PTM) input/output
	SEG6	LCD1	—	SEG	LCD Segment output
PC7/TCK2/ C1OUT/SEG7	PC7	PCPU	ST	CMOS	General purpose I/O. Register enabled pull-up
	TCK2	—	ST	—	TM2 (10-bit PTM) clock input
	C1OUT	CP1C	—	CMOS	Comparator 1 output pin
	SEG7	LCD1	—	SEG	LCD Segment output
PD0/TP3_0/ SEG8	PD0	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP3_0	CTRL0 STM3C0	ST	CMOS	TM3 (16-bit STM) input/output
	SEG8	LCD2	—	SEG	LCD Segment output
PD1/TP3_1/ SEG9	PD1	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TP3_1	CTRL0 STM3C0	ST	CMOS	TM3 (16-bit STM) input/output
	SEG9	LCD2	—	SEG	LCD Segment output
PD2/TCK3/ SEG10	PD2	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	TCK3	—	ST	—	TM3 (16-bit STM) clock input
	SEG10	LCD2	—	SEG	LCD Segment output
PD3/SEG11	PD3	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG11	LCD2	—	SEG	LCD Segment output
PD4/SEG12	PD4	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG12	LCD2	—	SEG	LCD Segment output
PD5/SEG13	PD5	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG13	LCD2	—	SEG	LCD Segment output
PD6/SEG14	PD6	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG14	LCD2	—	SEG	LCD Segment output
PD7/SEG15	PD7	PDPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG15	LCD2	—	SEG	LCD Segment output
SEG16~SEG37	SEGn	—	—	SEG	LCD Segment output
PB6/SEG38	PB6	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG38	LCD3	—	SEG	LCD Segment output
PB7/SEG39	PB7	PBPU	ST	CMOS	General purpose I/O. Register enabled pull-up.
	SEG39	LCD3	—	SEG	LCD Segment output
COM0~COM3	COMn	—	—	COM	LCD Common output

Pin Name	Function	OPT	I/T	O/T	Descriptions
V1, V2	V1, V2	—	AN	—	LCD voltage pump
C1, C2	C1, C2	—	AN	—	LCD voltage pump
PLCD	PLCD	—	PWR	—	LCD power supply
VMAX	VMAX	—	PWR	—	IC maximum voltage, connect to VDD or V1
AN0~AN7	ANn	—	AN	—	ADC input channel
VREFP	VREFP	—	PWR	—	ADC positive reference input
VREFN	VREFN	—	PWR	—	ADC negative reference input
VCM	VCM	—	—	PWR	ADC internal Common mode voltage output
VDD/VIN	VDD	—	PWR	—	Digital positive power supply
	VIN	—	PWR	—	LDO input pin
AVDD/VOUT	AVDD	—	PWR	—	Analog power supply
	VOUT	—	—	PWR	LDO output pin
VSS	VSS	—	PWR	—	Digital negative power supply
AVSS	AVSS	—	PWR	—	A/D negative power supply

Note: I/T: Input type; O/T: Output type;  
 OPT: Optional by configuration option (CO) or register option;  
 PWR: Power; CO: Configuration option;  
 ST: Schmitt Trigger input; CMOS: CMOS output; AN: Analog signal;  
 SEG: LCD SEG output; COM: LCD COM output;  
 HXT: High frequency crystal oscillator;  
 LXT: Low frequency crystal oscillator.

## Absolute Maximum Ratings

Supply Voltage .....	$V_{SS}-0.3V$ to $V_{SS}+6.0V$
Input Voltage .....	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature.....	$-50^{\circ}C$ to $125^{\circ}C$
Operating Temperature.....	$-40^{\circ}C$ to $85^{\circ}C$
$I_{OL}$ Total .....	150mA
$I_{OH}$ Total .....	-100mA
Total Power Dissipation .....	500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect devices reliability.

### D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>DD</sub>	Operating Voltage (HXT)	—	f <sub>sys</sub> =8MHz	2.2	—	5.5	V
			f <sub>sys</sub> =12MHz	2.7	—	5.5	V
			f <sub>sys</sub> =16MHz	3.3	—	5.5	V
			f <sub>sys</sub> =20MHz	4.5	—	5.5	V
	Operating Voltage (HIRC)	—	f <sub>sys</sub> =4.9152MHz	2.2	—	5.5	V
I <sub>DD</sub>	Operating Current (HXT, f <sub>sys</sub> =f <sub>H</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, f <sub>H</sub> =8MHz,	—	1.0	1.5	mA
		5V	LDO ,LCD, ADC off, WDT enable	—	2.5	4	mA
		3V	No load, f <sub>H</sub> =10MHz,	—	1.2	2.0	mA
		5V	LDO, LCD, ADC off, WDT enable	—	2.8	4.5	mA
		3V	No load, f <sub>H</sub> =12MHz,	—	1.5	2.5	mA
		5V	LDO, LCD, ADC off, WDT enable	—	3.5	5.5	mA
		3.3V	No load, f <sub>H</sub> =16MHz,	—	2.0	3.0	mA
		5V	LDO, LCD, ADC off, WDT enable	—	4.5	7.0	mA
	Operating Current (HIRC, f <sub>sys</sub> =f <sub>H</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, f <sub>H</sub> =4.9152MHz,	—	0.7	1.2	mA
		5V	LDO, LCD, ADC off, WDT enable	—	1.5	2.5	mA
		3V	No load, f <sub>H</sub> =4.9152×2MHz,	—	1.2	2.0	mA
		5V	LDO, LCD, ADC off, WDT enable	—	2.8	4.5	mA
		3V	No load, f <sub>H</sub> =4.9152×3MHz,	—	1.8	3.0	mA
		5V	LDO, LCD, ADC off, WDT enable	—	4.0	6.0	mA
	Operating Current (HXT, f <sub>sys</sub> =f <sub>L</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, f <sub>H</sub> =12MHz, f <sub>L</sub> =f <sub>H</sub> /2,	—	0.9	1.5	mA
		5V	LDO, LCD, ADC off, WDT enable	—	2.1	3.3	mA
		3V	No load, f <sub>H</sub> =12MHz, f <sub>L</sub> =f <sub>H</sub> /4,	—	0.6	1.0	mA
		5V	LDO, LCD, ADC off, WDT enable	—	1.6	2.5	mA
		3V	No load, f <sub>H</sub> =12MHz, f <sub>L</sub> =f <sub>H</sub> /8,	—	0.48	0.8	mA
		5V	LDO, LCD, ADC off, WDT enable	—	1.2	2.0	mA
		3V	No load, f <sub>H</sub> =12MHz, f <sub>L</sub> =f <sub>H</sub> /16,	—	0.42	0.7	mA
		5V	LDO, LCD, ADC off, WDT enable	—	1.1	1.7	mA
		3V	No load, f <sub>H</sub> =12MHz, f <sub>L</sub> =f <sub>H</sub> /32,	—	0.38	0.6	mA
		5V	LDO, LCD, ADC off, WDT enable	—	1.0	1.5	mA
		3V	No load, f <sub>H</sub> =12MHz, f <sub>L</sub> =f <sub>H</sub> /64,	—	0.36	0.55	mA
		5V	LDO, LCD, ADC off, WDT enable	—	1.0	1.5	mA
	Operating Current (LXT, f <sub>sys</sub> =f <sub>sub</sub> =f <sub>LXT</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> )	3V	No load, LDO, LCD, ADC off,	—	10	20	μA
		5V	WDT enable, LXTLP=0	—	30	50	μA
		3V	No load, LDO , LCD, ADC off,	—	10	20	μA
		5V	WDT enable, LXTLP=1	—	30	50	μA
	Operating Current (LIRC, f <sub>sys</sub> =f <sub>sub</sub> =f <sub>LIRC</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LIRC</sub> )	3V	No load, LDO, LCD, ADC off,	—	10	20	μA
		5V	WDT enable	—	30	50	μA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
	Standby Current (Sleep0) (HXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT disable, f <sub>sys</sub> =12MHz	—	0.2	0.8	μA
		5V		—	0.5	1.0	μA
	Standby Current (Sleep0) (LXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT disable, f <sub>sys</sub> =32768Hz	—	0.2	0.8	μA
		5V		—	0.5	1.0	μA
	Standby Current (Sleep1) (HXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =12MHz	—	1.3	5	μA
		5V		—	2.2	10	μA
	Standby Current (Sleep1) (HXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, ADC off, WDT enable, f <sub>sys</sub> =12MHz	—	1.3	5	μA
		5V		—	2.2	10	μA
	Standby Current (Sleep1) (LXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> )	3V	No load, system HALT, LDO, ADC off, WDT enable, f <sub>sys</sub> =32768Hz	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Sleep1) (HXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	—	No load, system HALT, LDO, LCD, ADC off, WDT disable, f <sub>sys</sub> =12MHz, LVR enable and LVDEN=1	—	90	120	μA
	Standby Current (Idle0) (HXT, f <sub>sys</sub> =off, f <sub>s</sub> =T1)	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =12MHz	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Idle0) (HXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =12MHz	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Idle0) (HIRC, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =4.9152×3MHz	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Idle0) (HXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =12MHz/64	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Idle0) (LXT, f <sub>sys</sub> =off, f <sub>s</sub> =T1)	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =32768Hz	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Idle0) (LXT, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =32768Hz	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Idle0) (LIRC, f <sub>sys</sub> =off, f <sub>s</sub> =f <sub>sub</sub> =f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =32kHz	—	1.3	3.0	μA
		5V		—	2.2	5.0	μA
	Standby Current (Idle1) (LXT, f <sub>sys</sub> =f <sub>sub</sub> =f <sub>LXT</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =32768Hz	—	1.9	4.0	μA
		5V		—	3.3	7.0	μA
	Standby Current (Idle1) (HXT, f <sub>sys</sub> =f <sub>L</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =12MHz/64	—	0.34	0.6	mA
		5V		—	0.85	1.2	mA
	Standby Current (Idle1) (HXT, f <sub>sys</sub> =f <sub>H</sub> , f <sub>s</sub> =f <sub>sub</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	3V	No load, system HALT, LDO, LCD, ADC off, WDT enable, f <sub>sys</sub> =12MHz	—	0.6	1.0	mA
		5V		—	1.2	2.0	mA
V <sub>IL</sub>	Input Low Voltage for I/O Ports, TCK, TP, INT0 and INT1	—	—	0	—	0.2V <sub>DD</sub>	V
		5V	—	0	—	1.5	V
V <sub>IH</sub>	Input High Voltage for I/O Ports, TCK, TP, INT0 and INT1	—	—	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	V
		5V	—	3.5	—	5	V
V <sub>LVR</sub>	Low Voltage Reset Voltage	—	LVR enable, 2.10V option	-5%	2.1	+5%	V
			LVR enable, 2.55V option		2.55		V
			LVR enable, 3.15V option		3.15		V
			LVR enable, 3.80V option		3.8		V
I <sub>LVR</sub>	Low Voltage Reset Current	—	LVR enable, LVDEN=0	—	60	90	μA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>LVD</sub>	Low Voltage Detector Voltage	—	LVDEN=1, V <sub>LVD</sub> =2.0V	-5%	2.0	+5%	V
			LVDEN=1, V <sub>LVD</sub> =2.2V		2.2		V
			LVDEN=1, V <sub>LVD</sub> =2.4V		2.4		V
			LVDEN=1, V <sub>LVD</sub> =2.7V		2.7		V
			LVDEN=1, V <sub>LVD</sub> =3.0V		3.0		V
			LVDEN=1, V <sub>LVD</sub> =3.3V		3.3		V
			LVDEN=1, V <sub>LVD</sub> =3.6V		3.6		V
			LVDEN=1, V <sub>LVD</sub> =4.0V		4.0		V
I <sub>LVD</sub>	Low Voltage Detector Current	—	LVR disable, LVDEN=1	—	75	120	μA
			LVR enable, LVDEN=1	—	90	150	μA
I <sub>OL</sub>	I/O Port Sink Current (PA, PB, PC, PD)	3V	V <sub>OL</sub> =0.1V <sub>DD</sub>	4	8	—	mA
		5V	V <sub>OL</sub> =0.1V <sub>DD</sub>	10	20	—	mA
	LCD Sink Current (SEG)	—	PLCD=3V, V <sub>OL</sub> =0.1PLCD	210	420	—	μA
		—	PLCD=5V, V <sub>OL</sub> =0.1PLCD	350	700	—	μA
I <sub>OH</sub>	I/O Port Source Current (PA, PB, PC, PD)	3V	V <sub>OH</sub> =0.9V <sub>DD</sub>	-2	-4	—	mA
		5V	V <sub>OH</sub> =0.9V <sub>DD</sub>	-5	-10	—	mA
	LCD Source Current (SEG)	—	PLCD=3V, V <sub>OH</sub> =0.9PLCD	-80	-160	—	μA
		—	PLCD=5V, V <sub>OH</sub> =0.9PLCD	-180	-360	—	μA
R <sub>PH</sub>	Pull-high Resistance of I/O Ports	3V	—	20	60	100	kΩ
		5V	—	10	30	50	kΩ

## A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Condition				
f <sub>sys</sub>	System Clock (HXT)	2.2V~5.5V	—	0.4	—	8	MHz
		2.7V~5.5V		0.4	—	12	MHz
		3.3V~5.5V		0.4	—	16	MHz
		4.5V~5.5V		0.4	—	20	MHz
	System Clock (HIRC)	5V	Ta=25°C	-2%	4.9152 x2	+2%	MHz
	System Clock (LXT)	—	—	—	32768	—	Hz
System Clock (LIRC)	5V	Ta=25°C	-10%	32	+10%	kHz	
	2.2V~5.5V	Ta=-40°C~+85°C	-50%	32	+60%	kHz	
t <sub>SST</sub>	System Start-up Timer Period (Wake-up from HALT)	—	f <sub>sys</sub> =HXT or LXT	—	1024	—	t <sub>sys</sub>
			f <sub>sys</sub> =HIRC	—	16	—	
			f <sub>sys</sub> =LIRC	—	1~2	—	
t <sub>RSTD</sub>	System Reset Delay Time (Power On Reset)	—	—	25	50	100	ms
	System Reset Delay Time (Any Reset except Power On Reset)	—	—	8.3	16.7	33.3	ms
t <sub>INT</sub>	Interrupt pulse width	—	—	10	—	—	μs
t <sub>LVR</sub>	Low Voltage Width to Reset	—	—	120	240	480	μs
t <sub>LVD</sub>	Low Voltage Width to Interrupt	—	—	60	120	240	μs
t <sub>LVDS</sub>	LVDO Stable Time	—	For LVR enable, LVD off → on	—	—	15	μs
		—	For LVR disable, LVD off → on	—	—	150	μs
t <sub>EERD</sub>	EEPROM Read Time	—	—	—	—	4	t <sub>sys</sub>
t <sub>EEWR</sub>	EEPROM Write Time	—	—	1	2	4	ms
t <sub>TIMER</sub>	TCKn and Timer Capture Input Pulse Width	—	—	0.3	—	—	μs

Note: t<sub>sys</sub> = 1/f<sub>sys</sub>

**LDO+PGA+ADC+VCM Electrical Characteristics**

 LDO + VCM Test conditions: MCU halt, other function disable,  $V_{DD}=V_{IN}$ ,  $T_a=25^{\circ}\text{C}$ 

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		$V_{DD}$	Conditions				
$V_{IN}$	LDO Input Voltage	—	—	2.6	—	5.5	V
$I_Q$	LDO Quiescent Current	—	LDOVS[1:0]=00B, $V_{IN}=3.6\text{V}$ , No load	—	400	520	$\mu\text{A}$
$V_{OUT\_LDO}$	LDO Output Voltage (VOUT/AVDD Pin)	—	LDOVS[1:0]=00B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=0.1\text{mA}$	-5%	2.4	+5%	V
		—	LDOVS[1:0]=01B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=0.1\text{mA}$		2.6		
		—	LDOVS[1:0]=10B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=0.1\text{mA}$		2.9		
		—	LDOVS[1:0]=11B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=0.1\text{mA}$		3.3		
$\Delta V_{LOAD}$	LDO Load Regulation <sup>(Note 1)</sup>	—	LDOVS[1:0]=00B, $V_{IN}=V_{OUT\_LDO} + 0.2\text{V}$ , $0\text{mA} \leq I_{LOAD} \leq 10\text{mA}$	—	0.105	0.21	%/mA
$V_{DROF\_LDO}$	LDO Dropout Voltage <sup>(Note2)</sup>	—	LDOVS[1:0]=00B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=10\text{mA}$ , $\Delta V_{OUT\_LDO}=2\%$	—	—	100	mV
		—	LDOVS[1:0]=01B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=10\text{mA}$ , $\Delta V_{OUT\_LDO}=2\%$	—	—	130	mV
		—	LDOVS[1:0]=10B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=10\text{mA}$ , $\Delta V_{OUT\_LDO}=2\%$	—	—	180	mV
		—	LDOVS[1:0]=11B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=10\text{mA}$ , $\Delta V_{OUT\_LDO}=2\%$	—	—	200	mV
$TC_{LDO}$	LDO Temperature Coefficient	—	$T_a=-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ , LDOVS[1:0]=00B, $V_{IN}=3.6\text{V}$ , $I_{LOAD}=100\mu\text{A}$	—	—	0.48	$\text{mV}/^{\circ}\text{C}$
$\Delta V_{LINE\_LDO}$	LDO Line Regulation	—	LDOVS[1:0]=00B, $2.6\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $I_{LOAD}=100\mu\text{A}$	—	—	0.3	%/V
$V_{OUT\_VCM}$	Vcm Output Voltage (VCM Pin)	—	VCMS=0, $AV_{DD}=3.3\text{V}$ , No load	-5%	1.05	+5%	V
		—	VCMS=1, $AV_{DD}=3.3\text{V}$ , No load	-5%	1.25	+5%	V
$TC_{VCM}$	VCM Temperature Coefficient	—	$T_a=-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ , VCMS=1, $AV_{DD}=3.3\text{V}$ , $I_{LOAD}=10\mu\text{A}$	—	—	0.24	$\text{mV}/^{\circ}\text{C}$
$\Delta V_{LINE\_VCM}$	VCM Line Regulation	—	VCMS=1, $2.4\text{V} \leq AV_{DD} \leq 3.3\text{V}$ , No load	—	—	0.3	%/V
$t_{VCMs}$	VCM Turn On Stable Time	—	VCMS=1, $AV_{DD}=3.3\text{V}$ , No load	—	—	10	ms
$I_{OH}$	Source Current for VCM Pin	—	VCMS=1, $AV_{DD}=3.3\text{V}$ , $\Delta V_{OUT\_VCM}=-2\%$	1	—	—	mA
$I_{OL}$	Sink Current for VCM Pin	—	VCMS=1, $AV_{DD}=3.3\text{V}$ , $\Delta V_{OUT\_VCM}=+2\%$	1	—	—	mA
<b>ADC &amp; ADC Internal Reference Voltage (Delta Sigma ADC)</b>							
$AV_{DD}$	Supply Voltage for VCM, ADC, PGA	—	—	2.4	—	3.3	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
I <sub>ADC</sub>	Additional Current for ADC Enable	—	VCM enable, VRBUIFP=1 and VRBUFN=1	—	—	900	μA
		—	VCM enable, VRBUIFP=0 and VRBUFN=0	—	600	750	μA
		—	VCM disable, VRBUIFP=0 and VRBUFN=0	—	500	650	μA
I <sub>ADSTB</sub>	Standby Current	—	System halt, no load	—	—	1	μA
RS <sub>ADC</sub>	Resolution	—	—	—	—	24	Bit
INL	Integral Nonlinearity	—	AV <sub>DD</sub> =3.3V, V <sub>REF</sub> =1.25V, ΔSI=±450mV, PGA gain=1	—	±50	±200	ppm
NFB	Noise Free Bits	—	PGA gain=128 Data rate=12.5Hz	—	15.4	—	Bit
ENOB	Effective Number of Bits	—	PGA gain=128 Data rate=12.5Hz	—	18.1	—	Bit
f <sub>ADCK</sub>	ADC Clock Frequency	—	—	40	409.6	440	kHz
f <sub>ADO</sub>	ADC Output Data Rate	—	f <sub>MCLK</sub> =4.9152MHz, FLMS[2:0]=000B	5	—	640	Hz
		—	f <sub>MCLK</sub> =4.9152MHz, FLMS[2:0]=010B	12.5	—	1600	Hz
V <sub>REFP</sub>	Reference Input Voltage	—	VGS[1:0]=00B, VREFS=1, VRBUIFP=0, VRBUFN=0	0.96	1.25	2.2	V
V <sub>REFN</sub>		—	VRBUIFP=0, VRBUFN=0	0	0	1.0	V
V <sub>REF</sub>		—	VGS[1:0]=00B, V <sub>REF</sub> =V <sub>REFP</sub> - V <sub>REFN</sub>	0.96	1.25	1.44	V
<b>PGA</b>							
V <sub>CM</sub>	Common Mode Voltage Range	—	—	0.4	—	AV <sub>DD</sub> -1.1	V
ΔD <sub>i</sub>	Differential Input Voltage Range	—	Gain=PGS × AGS	-V <sub>REF</sub> /Gain	—	+V <sub>REF</sub> /Gain	V
<b>Temperature Sensor</b>							
TC <sub>TS</sub>	Temperature Sensor Temperature Coefficient	—	T <sub>a</sub> =-40°C~85°C, V <sub>REF</sub> =1.25V, VGS[1:0]=00B (Gain=1), VRBUIFP=0, VRBUFN=0	—	175	—	μV/°C

Note: 1. Load regulation is measured at a constant junction temperature, using pulse testing with a low ON time and is guaranteed up to the maximum power dissipation. Power dissipation is determined by the input/output differential voltage and the output current. Guaranteed maximum power dissipation will not be available over the full input/output range. The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_a) / \theta_{JA}$ .

2. Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at appointed V<sub>IN</sub>.

**Effective Number of Bits (ENOB)**

AV<sub>DD</sub>=3.3V, V<sub>REF</sub>=1.25V, FLMS[2:0]=000

DATA RATE (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
5	19.7	19.8	19.6	19.7	19.7	19.6	19.2	18.6
10	19.4	19.3	19.3	19.3	19.3	19.1	18.7	18.1
20	19.0	18.8	18.7	18.9	18.8	18.6	18.2	17.5
40	18.4	18.3	18.3	18.3	18.3	18.1	17.7	17.0
80	18.1	17.9	18.0	17.9	17.9	17.6	17.2	16.5
160	17.6	17.4	17.4	17.4	17.3	17.1	16.6	15.9
320	15.8	15.8	15.9	15.8	15.9	15.9	15.8	15.3
640	14.1	14.0	14.0	14.1	14.1	14.0	14.1	14.4

AV<sub>DD</sub>=3.3V, V<sub>REF</sub>=1.25V, FLMS[2:0]=010

DATA RATE (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
12.5	19.4	18.8	18.7	18.8	18.8	18.7	18.9	18.1
25	19.0	18.3	18.3	18.3	18.3	18.2	17.9	17.3
50	18.5	17.8	17.8	17.8	17.9	17.7	17.4	16.8
100	18.2	18.2	18.1	18.2	18.1	17.8	17.2	16.4
200	17.9	17.8	17.8	17.8	17.6	17.3	16.7	15.9
400	17.4	17.2	17.2	17.2	17.1	16.8	16.2	15.4
800	16.2	16.1	16.1	16.1	16.1	15.9	15.5	14.8
1600	14.5	14.5	14.5	14.4	14.5	14.5	14.3	14.0

**Comparator Electrical Characteristics**

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>CMP</sub>	Comparator Operating Voltage	—	—	2.2	—	5.5	V
I <sub>CMP</sub>	Comparator Operating Current	3V	—	—	37	56	μA
		5V	—	—	130	200	
V <sub>CMPOS</sub>	Comparator Input Offset Voltage	—	—	-10	—	10	mV
V <sub>HYS</sub>	Hysteresis Width	—	—	20	40	60	mV
V <sub>CM</sub>	Comparator Common Mode Voltage Range	—	—	V <sub>SS</sub>	—	V <sub>DD</sub> -1.4V	V
A <sub>OL</sub>	Comparator Open Loop Gain	—	—	60	80	—	dB
t <sub>PD</sub>	Comparator Response Time	—	With 100mV overdrive <sup>(Note)</sup>	—	200	450	ns

Note: Measured with comparator one input pin at V<sub>CM</sub> = (V<sub>DD</sub>-1.4)/2 while the other pin input transition from V<sub>SS</sub> to (V<sub>CM</sub> + 100mV) or from V<sub>DD</sub> to (V<sub>CM</sub> - 100mV).

## LCD Electrical Characteristics

Ta=25°C

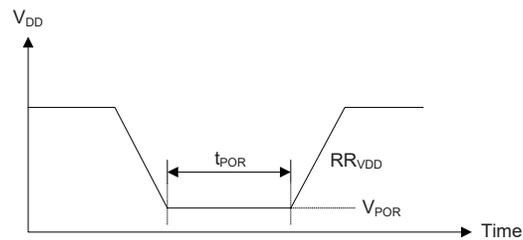
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	
		V <sub>DD</sub>	Conditions					
I <sub>LCD</sub>	Only LCD on Current, LCD Clock=4kHz	5V	PLCD=5V (R type) No load, 1/3 Bias, RCT=0, LCDPR=0,	LCDIS[1:0]=00B	—	25	37.5	μA
				LCDIS[1:0]=01B		50	75	
				LCDIS[1:0]=10B		100	150	
				LCDIS[1:0]=11B		200	300	
	Standby Current (Idle) (f <sub>SYS</sub> , f <sub>WDT</sub> off, f <sub>S</sub> =f <sub>SUB</sub> =f <sub>LXT</sub> or f <sub>LIRC</sub> )	5V	PLCD=5V (C type), RCT=1 No load, system HALT, LCD on, WDT off, C type, 1/3 Bias	—	3	6	μA	
V <sub>LCD</sub>	PLCD comes from PLCD pin	—	RCT=0,LCDPR=0	—	—	V <sub>DD</sub>	V	
	PLCD Comes from Charge Pump	2.6V~5.5V	RCT=0,LCDPR=1, CPVS[1:0]=00b	-10%	3.3	+10%	V	
		2.3V~5.5V	RCT=0,LCDPR=1, CPVS[1:0]=01b		3.0			
		2.2V~5.5V	RCT=0,LCDPR=1, CPVS[1:0]=10b		2.7			
3.8V~5.5V	RCT=0,LCDPR=1, CPVS[1:0]=11b	4.5						

Note: Users have to take care that V<sub>MAX</sub> must be greater than or equal to V<sub>LCD</sub>.

## Power-on Reset Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>POR</sub>	V <sub>DD</sub> Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR <sub>VDD</sub>	V <sub>DD</sub> Raising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t <sub>POR</sub>	Minimum Time for V <sub>DD</sub> Stays at V <sub>POR</sub> to Ensure Power-on Reset	—	—	1	—	—	ms

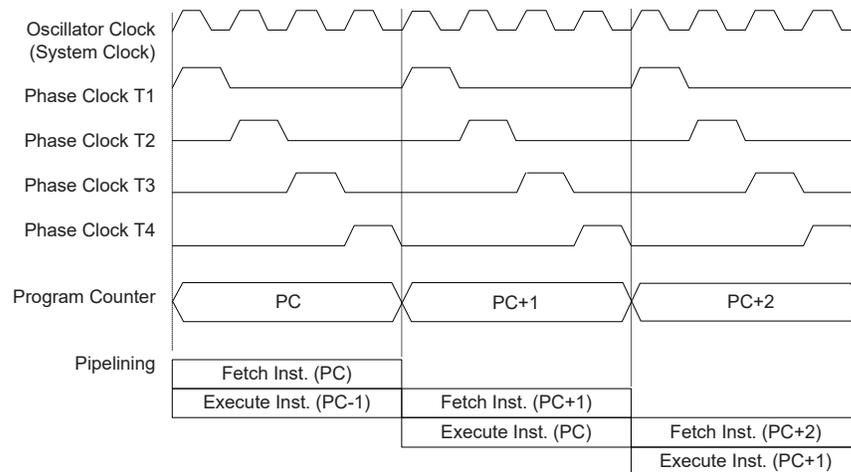


## System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to their internal system architecture. The range of these devices take advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one or two cycles for most of the standard or extended instructions respectively, with the exception of branch or call instructions which need one more cycle. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility. This makes these devices suitable for low-cost, high-volume production for controller applications.

## Clocking and Pipelining

The main system clock, derived from either a HXT, LXT, HIRC or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.



**System Clocking and Pipelining**

For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.



**Instruction Fetching**

### Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demands a jump to a non-consecutive Program Memory address. For the device whose memory capacity is greater than 8K words the Program Memory address may be located in a certain program memory bank which is selected by the program memory bank pointer bit, PBP0. Only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by the application program.

When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.

Device	Program Counter	
	Program Counter High Byte	PCL Register
HT67F5650	PC12~PC8	PCL7~PCL0
HT67F5660	PBP0, PC12~PC8	PCL7~PCL0

**Program Counter**

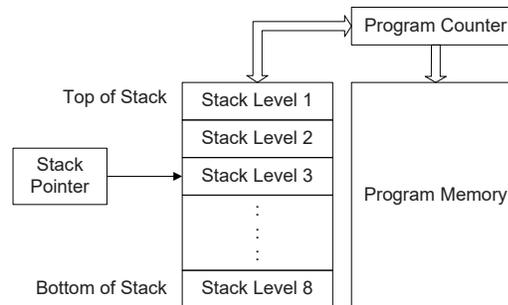
The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writeable register. By transferring data directly into this register, a short program jump can be executed directly; however, as only this low byte is available for manipulation, the jumps are limited to the present page of memory that is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted. Manipulating the PCL register may cause program branching, so an extra cycle is needed to pre-fetch.

## Stack

This is a special part of the memory which is used to save the contents of the Program Counter only. The stack is organized into 8 levels and neither part of the data nor part of the program space, and is neither readable nor writeable. The activated level is indexed by the Stack Pointer, and is neither readable nor writeable. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.

If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching.

If the stack is overflow, the first Program Counter save in the stack will be lost.



## Arithmetic and Logic Unit – ALU

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

- Arithmetic operations: ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA, LADD, LADDM, LADC, LADCM, LSUB, LSUBM, LSBC, LSBCM, LDAA
- Logic operations: AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA, LAND, LANDM, LOR, LORM, LXOR, LXORM, LCPL, LCPLA
- Rotation RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC, LRR, LRRR, LRRCA, LRRR, LRLA, LRL, LRLCA, LRLC
- Increment and Decrement INCA, INC, DECA, DEC, LINCA, LINC, LDECA, LDEC
- Branch decision, JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI, LSNZ, LSZ, LSZA, LSIZ, LSIZ, LSDZ, LSDZA

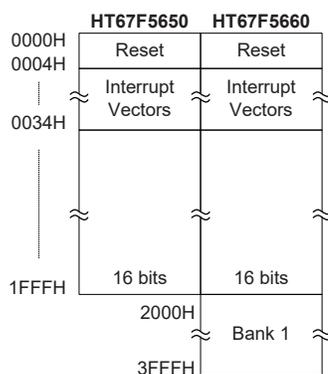
## Flash Program Memory

The Program Memory is the location where the user code or program is stored. For these devices the Program Memory is Flash type, which means it can be programmed and re-programmed a large number of times, allowing the user the convenience of code modification on the same device. By using the appropriate programming tools, these Flash devices offer users the flexibility to conveniently debug and develop their applications while also offering a means of field programming and updating.

Device	Capacity	Banks
HT67F5650	8K×16	—
HT67F5660	16K×16	0~1

### Structure

The Program Memory has a capacity of 8K×16 to 16K×16 bits. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by a separate table pointer register.



**Program Memory Structure**

### Special Vectors

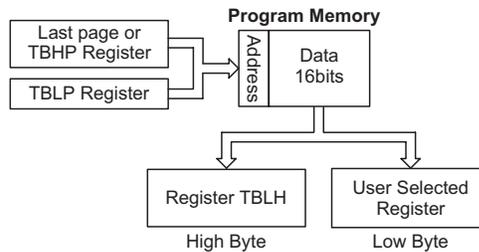
Within the Program Memory, certain locations are reserved for the reset and interrupts. The location 000H is reserved for use by these devices reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.

## Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, the table pointer must first be setup by placing the address of the look up data to be retrieved in the table pointer register, TBLP and TBHP. These registers define the total address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the Program Memory using the corresponding table read instruction such as "TABRD [m]" or "TABRDL [m]" respectively when the memory [m] is located in sector 0. If the memory [m] is located in other sectors, the data can be retrieved from the program memory using the corresponding extended table read instruction such as "LTABRD [m]" or "LTABRDL [m]" respectively. When the instruction is executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register.

The accompanying diagram illustrates the addressing data flow of the look-up table.



## Table Program Example

The following example shows how the table pointer and table data is defined and retrieved from the microcontroller. This example uses raw table data located in the Program Memory which is stored there using the ORG statement. The value at this ORG statement is "1F00H" which refers to the start address of the last page within the 8K Program Memory of the HT67F5650 device. The table pointer low byte register is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "1F06H" or 6 locations after the start of the last page. Note that the value for the table pointer is referenced to the first address specified by TBLP and TBHP if the "TABRD [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRD [m]" instruction is executed.

Because the TBLH register is a read/write register and can be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of the TBLH and subsequently cause errors if used again by the main routine. As a rule it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

**Table Read Program Example**

```

tempreg1 db ?      ; temporary register #1
tempreg2 db ?      ; temporary register #2
:
:
mov a,06h          ; initialise low table pointer - note that this address
                  ; is referenced
mov tblp,a        ; to the last page or the page that tbhp pointed
mov a,1Fh         ; initialise high table pointer
mov tbhp,a
:
:
tabrd tempreg1    ; transfers value in table referenced by table pointer data at program
                  ; memory address "1F06H" transferred to tempreg1 and TBLH
dec tblp          ; reduce value of table pointer by one
tabrd tempreg2    ; transfers value in table referenced by table pointer
                  ; data at program memory address "1F05H" transferred to
                  ; tempreg2 and TBLH in this example the data "1AH" is
                  ; transferred to tempreg1 and data "0FH" to register tempreg2
:
:
org 1F00h         ; sets initial address of program memory
dc 00Ah, 00Bh, 00Ch, 00Dh, 00Eh, 00Fh, 01Ah, 01Bh
:
:

```

**In Circuit Programming – ICP**

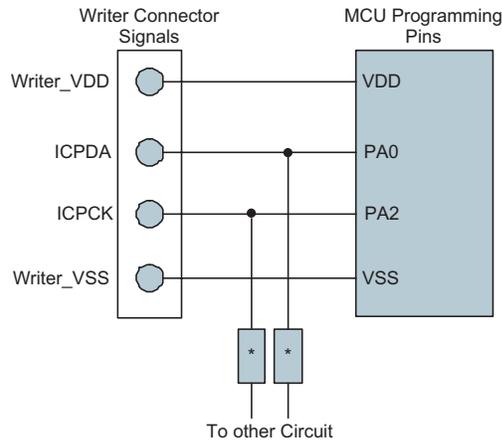
The provision of Flash type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device. As an additional convenience, Holtek has provided a means of programming the microcontroller in-circuit using a 4-pin interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of these devices.

The Holtek Flash MCU to Writer Programming Pin correspondence table is as follows:

Holtek Writer Pins	MCU Programming Pins	Pin Description
ICPDA	PA0	Programming Serial Data/Address
ICPCK	PA2	Programming Clock
VDD	VDD	Power Supply
VSS	VSS	Ground

The Program Memory and EEPROM data memory can be programmed serially in-circuit using this 4-wire interface. Data is downloaded and uploaded serially on a single pin with an additional line for the clock. Two additional lines are required for the power supply. The technical details regarding the in-circuit programming of these devices are beyond the scope of this document and will be supplied in supplementary literature.

During the programming process, the user must take care of the ICPDA and ICPCK pins for data and clock programming purposes to ensure that no other outputs are connected to these two pins.



Note: \* may be resistor or capacitor. The resistance of \* must be greater than 1k or the capacitance of \* must be less than 1nF.

### On Chip Debug Support – OCDS

There is an EV chip named HT67V5650/HT67V5660 which is used to emulate the real MCU device named HT67F5650/HT67F5660. The EV chip device also provides an "On-Chip Debug" function to debug the device during the development process. The EV chip and the actual MCU device are almost functionally compatible except for "On-Chip Debug" function. Users can use the EV chip device to emulate the real chip device behavior by connecting the OCSDA and OCDSCK pins to the Holtek HT-IDE development tools. The OCSDA pin is the OCDS Data/Address input/output pin while the OCDSCK pin is the OCDS clock input pin. When users use the EV chip for debugging, other functions which are shared with the OCSDA and OCDSCK pins in the actual MCU device will have no effect in the EV chip. However, the two OCDS pins which are pin-shared with the ICP programming pins are still used as the Flash Memory programming pins for ICP. For more detailed OCDS information, refer to the corresponding document named "Holtek e-Link for 8-bit MCU OCDS User's Guide".

Holtek e-Link Pins	EV Chip Pins	Pin Description
OCSDA	OCSDA	On-Chip Debug Support Data/Address input/output
OCDSCK	OCDSCK	On-Chip Debug Support Clock input
VDD	VDD	Power Supply
VSS	VSS	Ground

### In Application Programming – IAP

These devices offer IAP function to update data or application program to Flash ROM. Users can define any ROM location for IAP, but there are some features which user must notice in using IAP function.

IAP Features	HT67F5650 Configurations	HT67F5660 Configurations
Erase Page	32 words / page	64 words / page
Writing Word	32 words / time	64 words / time
Reading Word	1 word / time	1 word / time

### In Application Programming Control Register

The Address register, FARL and FARH, the Data registers, FD0L/FD0H, FD1L/FD1H, FD2L/FD2H and FD3L/FD3H, located in all Data Memory sectors, together with the Control registers, FC0, FC1 and FC2, located in Data Memory Sector 1, are the corresponding Flash access registers for IAP. If using the indirect addressing method to access the FC0, FC1 and FC2 registers, all read and write operations to the registers must be performed using the Indirect Addressing Register, IAR1 or IAR2, and the Memory Pointer pair, MP1L/MP1H or MP2L/MP2H. Because the FC0, FC1 and FC2 control registers are located at the address of 6DH~6FH in Data Memory sector 1, the desired value ranged from 6DH~6FH must first be written into the MP1L or MP2L Memory Pointer low byte and the value "01H" must also be written into the MP1H or MP2H Memory Pointer high byte.

Register Name	Bit							
	7	6	5	4	3	2	1	0
FC0	CFWEN	FMOD2	FMOD1	FMOD0	FWPEN	FWT	FRDEN	FRD
FC1	D7	D6	D5	D4	D3	D2	D1	D0
FC2	—	—	—	—	—	—	—	CLWB
FARL	A7	A6	A5	A4	A3	A2	A1	A0
FARH (HT67F5650)	—	—	—	A12	A11	A10	A9	A8
FARH (HT67F5660)	—	—	A13	A12	A11	A10	A9	A8
FD0L	D7	D6	D5	D4	D3	D2	D1	D0
FD0H	D15	D14	D13	D12	D11	D10	D9	D8
FD1L	D7	D6	D5	D4	D3	D2	D1	D0
FD1H	D15	D14	D13	D12	D11	D10	D9	D8
FD2L	D7	D6	D5	D4	D3	D2	D1	D0
FD2H	D15	D14	D13	D12	D11	D10	D9	D8
FD3L	D7	D6	D5	D4	D3	D2	D1	D0
FD3H	D15	D14	D13	D12	D11	D10	D9	D8

IAP Registers List

• **FC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	CFWEN	FMOD2	FMOD1	FMOD0	FWPEN	FWT	FRDEN	FRD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7      **CFWEN**: Flash Memory Write enable control  
             0: Flash memory write function is disabled  
             1: Flash memory write function has been successfully enabled  
 When this bit is cleared to 0 by application program, the Flash memory write function is disabled. Note that writing a "1" into this bit results in no action. This bit is used to indicate that the Flash memory write function status. When this bit is set to 1 by hardware, it means that the Flash memory write function is enabled successfully. Otherwise, the Flash memory write function is disabled as the bit content is zero.
- Bit 6~4    **FMOD2~FMOD0**: Mode selection  
             000: Write program memory  
             001: Page erase program memory  
             010: Reserved  
             011: Read program memory  
             100: Reserved  
             101: Reserved  
             110: FWEN mode – Flash memory write function enable mode  
             111: Reserved
- Bit 3      **FWPEN**: Flash Memory Write procedure enable control  
             0: Disable  
             1: Enable  
 When this bit is set to 1 and the FMOD field is set to "110", the IAP controller will execute the "Flash memory write function enable" procedure. Once the Flash memory write function is successfully enabled, it is not necessary to set the FWPEN bit any more.
- Bit 2      **FWT**: Flash ROM write control bit  
             0: Do not initiate Flash memory write or Flash memory write process is completed  
             1: Initiate Flash memory write process  
 This bit can be set by software only, when write process completed, hardware will clear "FWT" bit.
- Bit 1      **FRDEN**: Flash memory read enabled bit  
             0: Flash memory read disable  
             1: Flash memory read enable
- Bit 0      **FRD**: Flash memory read control bit  
             0: Do not initiate Flash memory read or Flash memory read process is completed  
             1: Initiate Flash memory read process  
 This bit can be set by software only, when read process completed, hardware will clear "FRD" bit.

• **FC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R/W						
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D7~D0**: whole chip reset  
 When user writes 55H to this register, it will generate a reset signal to reset whole chip.

• **FC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	CLWB
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1 Unimplemented, read as "0"  
 Bit 0 **CLWB**: Flash Memory Write buffer clear control  
 0: Do not initiate Write Buffer Clear or Write Buffer Clear process is completed  
 1: Initiate Write Buffer Clear process  
 This bit can be set by software only, when clear write buffer process completed, hardware will clear "CLWB" bit.

• **FARL Register**

Bit	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 Flash Memory Address [7:0]

• **FARH Register – HT67F5650**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	A12	A11	A10	A9	A8
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	0	0	0	0	0

Bit 7~5 Unimplemented, read as "0"  
 Bit 4~0 Flash Memory Address [12:8]

• **FARH Register – HT67F5660**

Bit	7	6	5	4	3	2	1	0
Name	—	—	A13	A12	A11	A10	A9	A8
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as "0"  
 Bit 5~0 Flash Memory Address [13:8]

• **FD0L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 The first Flash Memory data [7:0]

• **FD0H Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 The first Flash Memory data [15:8]

• **FD1L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 The second Flash Memory data [7:0]

• **FD1H Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 The second Flash Memory data [15:8]

• **FD2L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 The third Flash Memory data [7:0]

• **FD2H Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 The third Flash Memory data [15:8]

• **FD3L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 The fourth Flash Memory data [7:0]

• **FD3H Register**

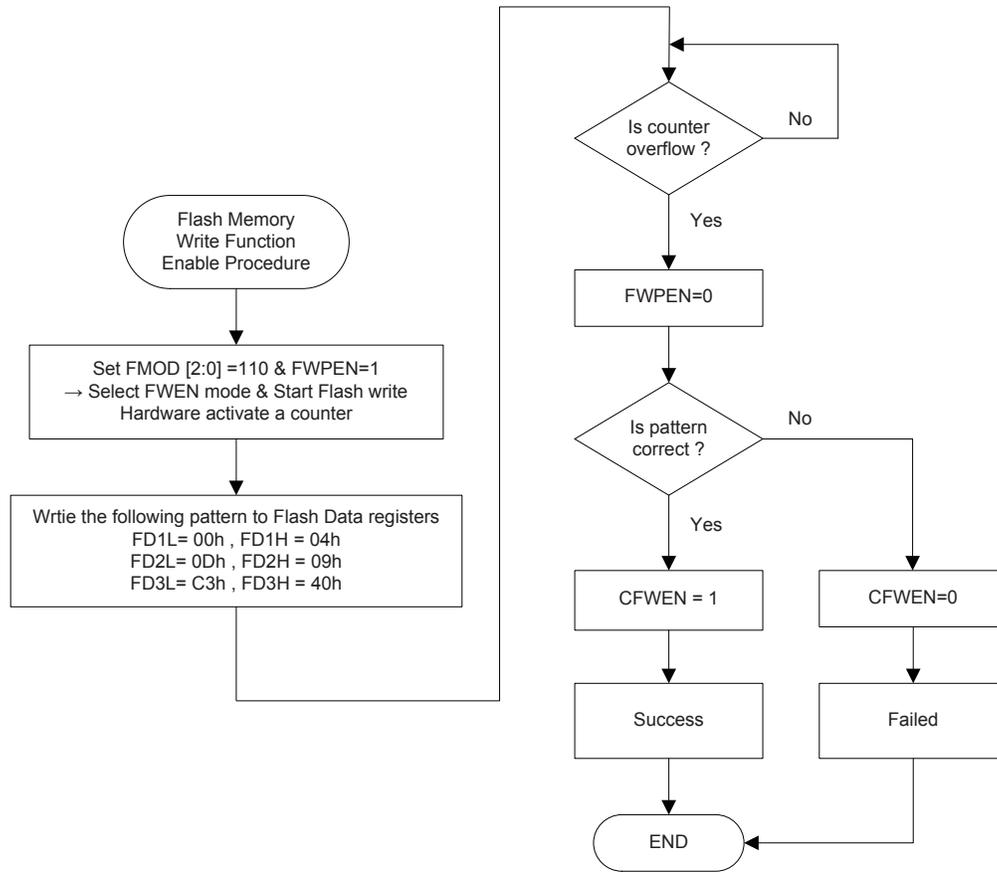
Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0      The fourth Flash Memory data [15:8]

**Flash Memory Write Function Enable Procedure**

In order to allow users to change the Flash memory data through the IAP control registers, users must first enable the Flash memory write operation by the following procedure:

- Step 1. Write "110" into the FMOD2~FMOD0 bits to select the FWEN mode.
- Step 2. Set the FWPEN bit to "1". The step 1 and step 2 can be executed simultaneously.
- Step 3. The pattern data with a sequence of 00H, 04H, 0DH, 09H, C3H and 40H must be written into the FD1L, FD1H, FD2L, FD2H, FD3L and FD3H registers respectively.
- Step 4. A counter with a time-out period of 300 $\mu$ s will be activated to allow users writing the correct pattern data into the FD1L/FD1H~FD3L/FD3H register pairs. The counter clock is derived from LIRC oscillator.
- Step 5. If the counter overflows or the pattern data is incorrect, the Flash memory write operation will not be enabled and users must again repeat the above procedure. Then the FWPEN bit will automatically be cleared to 0 by hardware.
- Step 6. If the pattern data is correct before the counter overflows, the Flash memory write operation will be enabled and the FWPEN bit will automatically be cleared to 0 by hardware. The CFWEN bit will also be set to 1 by hardware to indicate that the Flash memory write operation is successfully enabled.
- Step 7. Once the Flash memory write operation is enabled, the user can change the Flash ROM data through the Flash control register.
- Step 8. To disable the Flash memory write operation, the user can clear the CFWEN bit to 0.



**Flash Memory Write Function Enable Procedure**

**Flash Memory Read/Write Procedure**

After the Flash memory write function is successfully enabled through the preceding IAP procedure, users must first erase the corresponding Flash memory page and then initiate the Flash memory write operation. For the HT67F5650/HT67F5660 devices the number of the page erase operation is 32 and 64 words per page respectively, the available page erase address is specified by FARH register and the content of FARL[7:5] and FARL[7:6] bit field respectively.

Eraser Page	FARH	FARL[7:5]	FARL[4:0]
0	0000 0000	000	x xxxx
1	0000 0000	001	x xxxx
2	0000 0000	010	x xxxx
3	0000 0000	011	x xxxx
4	0000 0000	100	x xxxx
5	0000 0000	101	x xxxx
6	0000 0000	110	x xxxx
7	0000 0000	111	x xxxx
8	0000 0001	000	x xxxx
9	0000 0001	001	x xxxx
:	:	:	:
:	:	:	:
126	0000 1111	110	x xxxx
127	0000 1111	111	x xxxx
128	0001 0000	000	x xxxx
129	0001 0000	001	x xxxx
:	:	:	:
:	:	:	:
254	0001 1111	110	x xxxx
255	0001 1111	111	x xxxx

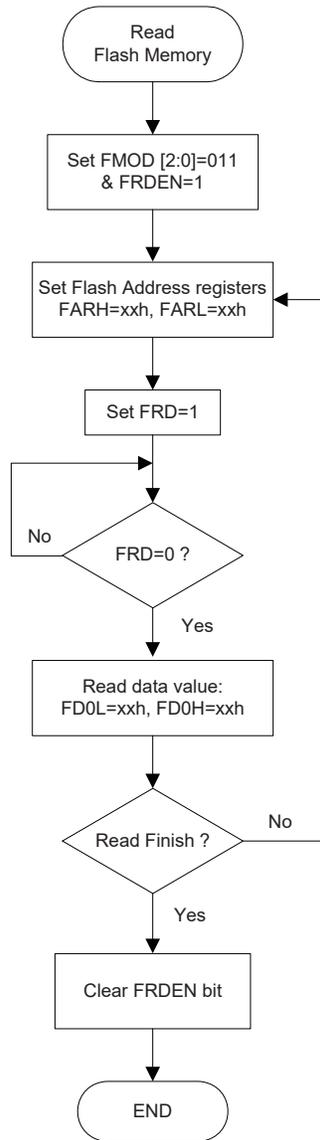
"x": don't care

**HT67F5650 Erase Page Number and Selection**

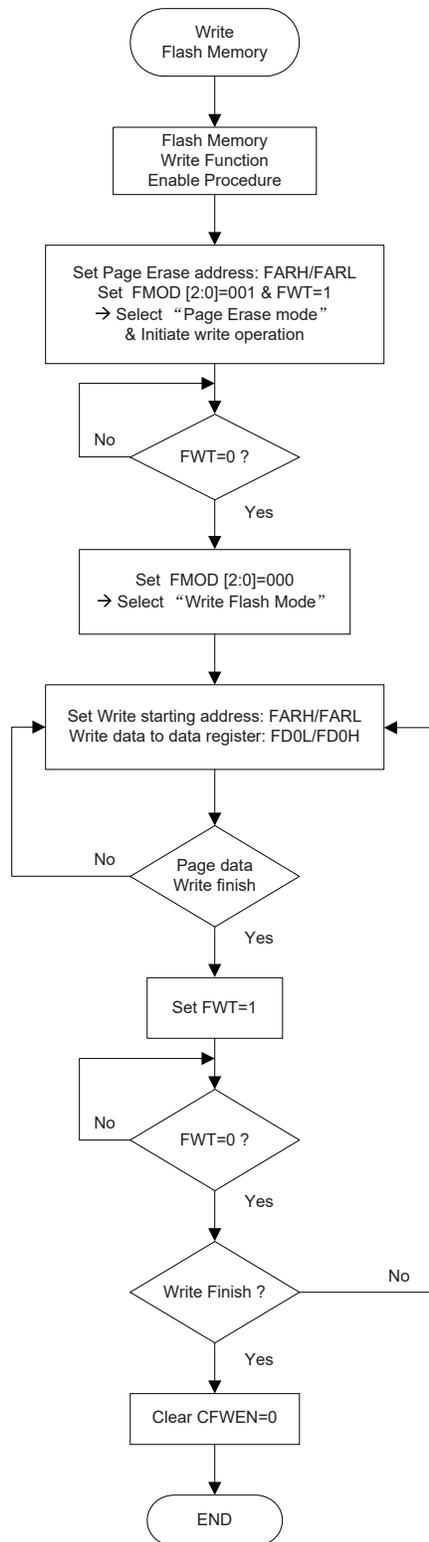
Eraser Page	FARH	FARL[7:6]	FARL[5:0]
0	0000 0000	00	xx xxxx
1	0000 0000	01	xx xxxx
2	0000 0000	10	xx xxxx
3	0000 0000	11	xx xxxx
4	0000 0001	00	xx xxxx
5	0000 0001	01	xx xxxx
:	:	:	:
:	:	:	:
126	0001 1111	10	xx xxxx
127	0001 1111	11	xx xxxx
128	0010 0000	00	xx xxxx
129	0010 0000	01	xx xxxx
:	:	:	:
:	:	:	:
254	0011 1111	10	xx xxxx
255	0011 1111	11	xx xxxx

"x": don't care

**HT67F5660 Erase Page Number and Selection**



Read Flash Memory Procedure



**Write Flash Memory Procedure**

Note: When the FWT or FRD bit is set to 1, the MCU is stopped.

## RAM Data Memory

The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored.

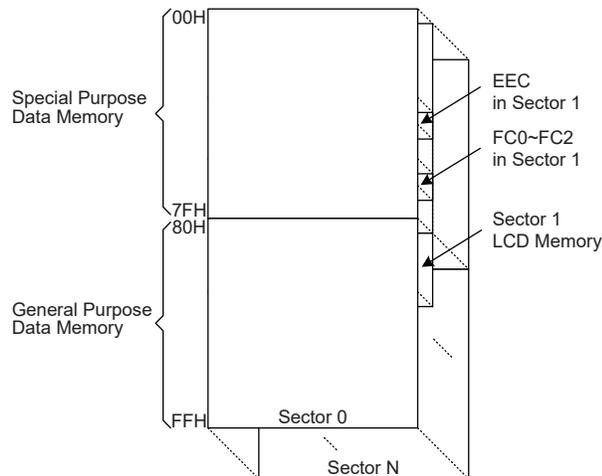
Divided into three types, the first of these is an area of RAM where special function registers are located. These registers have fixed locations and are necessary for correct operation of these devices. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation. The second area of Data Memory is reserved for general purpose use. All locations within this area are read and write accessible under program control. The third area is reserved for the LCD Memory. This special area of Data Memory is mapped directly to the LCD display so data written into this memory area will directly affect the displayed data.

### Structure

The Data Memory is subdivided into several sectors. The Special Purpose Data Memory registers are accessible in all sectors, with the exception of the EED register at address 40H, and the FC0, FC1 and FC2 registers at addresses 6DH~6FH, which are only accessible in Sector 1. Switching between the different Data Memory sectors is achieved by setting the Memory Pointers to the correct value. The start address of the Data Memory for all devices is the address 00H.

Device	Special Purpose Data Memory	LCD Data Memory		General Purpose Data Memory	
	Available Sectors	Capacity	Sectors	Capacity	Sectors
HT67F5650	0~4	40 × 8	1: 80H~A7H	512 × 8	0: 80H~FFH 2: 80H~FFH 3: 80H~FFH 4: 80H~FFH
HT67F5660	0~8	48 × 8	1: 80H~AFH	1024 × 8	0: 80H~FFH 2: 80H~FFH 3: 80H~FFH 4: 80H~FFH 5: 80H~FFH 6: 80H~FFH 7: 80H~FFH 8: 80H~FFH

**Data Memory Summary**



Note: 1. For HT67F5650, N=4 and the LCD Memory is from 80H~A7H;  
2. For HT67F5660, N=8 and the LCD Memory is from 80H~AFH.

**Data Memory Structure**

## **Data Memory Addressing**

For these devices that support the extended instructions, there is no Bank Pointer for Data Memory. The Bank Pointer, PBP, is only available for Program Memory. For Data Memory the desired Sector is pointed by the MP1H or MP2H register and the certain Data Memory address in the selected sector is specified by the MP1L or MP2L register when using indirect addressing access.

Direct Addressing can be used in all sectors using the corresponding instruction which can address all available data memory space. For the accessed data memory which is located in any data memory sectors except sector 0, the extended instructions can be used to access the data memory instead of using the indirect addressing access. The main difference between standard instructions and extended instructions is that the data memory address "m" in the extended instructions can be 10 bits or 11 bits depending upon which device is selected, the high byte indicates a sector and the low byte indicates a specific address.

## **General Purpose Data Memory**

All microcontroller programs require an area of read/write memory where temporary data can be stored and retrieved for use later. It is this area of RAM memory that is known as General Purpose Data Memory. This area of Data Memory is fully accessible by the user programming for both reading and writing operations. By using the bit operation instructions individual bits can be set or reset under program control giving the user a large range of flexibility for bit manipulation in the Data Memory.

## **Special Purpose Data Memory**

This area of Data Memory is where registers, necessary for the correct operation of the microcontroller, are stored. Most of the registers are both readable and writeable but some are protected and are readable only, the details of which are located under the relevant Special Function Register section. Note that for locations that are unused, any read instruction to these addresses will return the value "00H".

Sector 0~4		Sector 0,2,3,4   Sector 1	
00H	IAR0	40H	EEC
01H	MP0	41H	EEA
02H	IAR1	42H	EED
03H	MP1L	43H	PTM2C0
04H	MP1H	44H	PTM2C1
05H	ACC	45H	PTM2DL
06H	PCL	46H	PTM2DH
07H	TBLP	47H	PTM2AL
08H	TBLH	48H	PTM2AH
09H	TBHP	49H	CTRL0
0AH	STATUS	4AH	PTM1RPL
0BH		4BH	PTM1RPH
0CH	IAR2	4CH	PTM2RPL
0DH	MP2L	4DH	PTM2RPH
0EH	MP2H	4EH	CP1C
0FH		4FH	CPOC
10H	INTC0	50H	PWRC
11H	INTC1	51H	PGAC0
12H	INTC2	52H	PGAC1
13H	INTC3	53H	PGACS
14H	MFI0	54H	USR
15H	MFI1	55H	UCR1
16H	MFI2	56H	UCR2
17H	MFI3	57H	BRG
18H	PAWU	58H	TXR_RXR
19H	PAPU	59H	IRCTRL0
1AH	PA	5AH	IRCTRL1
1BH	PAC	5BH	LCDC
1CH	PBPU	5CH	LCD1
1DH	PB	5DH	LCD2
1EH	PBC	5EH	LCD3
1FH	PCPU	5FH	
20H	PC	60H	SIMC0
21H	PCC	61H	SIMC1
22H	PDPU	62H	SIMA/SIMC2
23H	PD	63H	SIMD
24H	PDC	64H	
25H		65H	SIMTOC
26H	SMOD	66H	STM3C0
27H	TBC	67H	STM3C1
28H	LVDC	68H	STM3DL
29H	INTEG	69H	STM3DH
2AH	WDTC	6AH	STM3AL
2BH	LVRC	6BH	STM3AH
2CH	CTRL	6CH	STM3RP
2DH		6DH	FC0
2EH	ADRL	6EH	FC1
2FH	ADRH	6FH	FC2
30H	ADCR0	70H	FARL
31H	ADCR1	71H	FARH
32H	ADCS	72H	FD0L
33H	ADRM	73H	FD0H
34H	PTM1C0	74H	FD1L
35H	PTM1C1	75H	FD1H
36H	PTM1DL	76H	FD2L
37H	PTM1DH	77H	FD2H
38H	PTM1AL	78H	FD3L
39H	PTM1AH	79H	FD3H
3AH	TM0C0	7AH	LCDCP
3BH	TM0C1	7BH	
3CH	TM0DL	7CH	
3DH	TM0DH	7DH	
3EH	TM0AL	7EH	
3FH	TM0AH	7FH	

■: unused, read as 00H

**Special Purpose Data Memory – HT67F5650**

Sector 0~8		Sector 0,2~8   Sector 1	
00H	IAR0	40H	EEC
01H	MP0	41H	EEA
02H	IAR1	42H	EED
03H	MP1L	43H	PTM2C0
04H	MP1H	44H	PTM2C1
05H	ACC	45H	PTM2DL
06H	PCL	46H	PTM2DH
07H	TBLP	47H	PTM2AL
08H	TBLH	48H	PTM2AH
09H	TBHP	49H	CTRL0
0AH	STATUS	4AH	PTM1RPL
0BH	PBP	4BH	PTM1RPH
0CH	IAR2	4CH	PTM2RPL
0DH	MP2L	4DH	PTM2RPH
0EH	MP2H	4EH	CP1C
0FH		4FH	CP0C
10H	INTC0	50H	PWRC
11H	INTC1	51H	PGAC0
12H	INTC2	52H	PGAC1
13H	INTC3	53H	PGACS
14H	MFI0	54H	USR
15H	MFI1	55H	UCR1
16H	MFI2	56H	UCR2
17H	MFI3	57H	BRG
18H	PAWU	58H	TXR_RXR
19H	PAPU	59H	IRCTRL0
1AH	PA	5AH	IRCTRL1
1BH	PAC	5BH	LCDC
1CH	PBPU	5CH	LCD1
1DH	PB	5DH	LCD2
1EH	PBC	5EH	LCD3
1FH	PCPU	5FH	LCD4
20H	PC	60H	SIMC0
21H	PCC	61H	SIMC1
22H	PDPU	62H	SIMA/SIMC2
23H	PD	63H	SIMD
24H	PDC	64H	
25H		65H	SIMTOC
26H	SMOD	66H	STM3C0
27H	TBC	67H	STM3C1
28H	LVDC	68H	STM3DL
29H	INTEG	69H	STM3DH
2AH	WDTC	6AH	STM3AL
2BH	LVRC	6BH	STM3AH
2CH	CTRL	6CH	STM3RP
2DH		6DH	FC0
2EH	ADRL	6EH	FC1
2FH	ADRH	6FH	FC2
30H	ADCR0	70H	FARL
31H	ADCR1	71H	FARH
32H	ADCS	72H	FD0L
33H	ADRM	73H	FD0H
34H	PTM1C0	74H	FD1L
35H	PTM1C1	75H	FD1H
36H	PTM1DL	76H	FD2L
37H	PTM1DH	77H	FD2H
38H	PTM1AL	78H	FD3L
39H	PTM1AH	79H	FD3H
3AH	TMOC0	7AH	LCDCP
3BH	TMOC1	7BH	
3CH	TMODL	7CH	
3DH	TMODH	7DH	
3EH	TMOAL	7EH	
3FH	TMOAH	7FH	

■: unused, read as 00H

**Special Purpose Data Memory – HT67F5660**

## Special Function Register Description

Most of the Special Function Register details will be described in the relevant functional section; however several registers require a separate description in this section.

### Indirect Addressing Registers – IAR0, IAR1, IAR2

The Indirect Addressing Registers, IAR0, IAR1 and IAR2, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0, IAR1 and IAR2 registers will result in no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointers, MP0, MP1L/MP1H or MP2L/MP2H. Acting as a pair, IAR0 and MP0 can together access data only from Sector 0 while the IAR1 register together with the MP1L/MP1H register pair and IAR2 register together with the MP2L/MP2H register pair can access data from any Data Memory Sector. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers will return a result of "00H" and writing to the registers will result in no operation.

### Memory Pointers – MP0, MP1L, MP1H, MP2L, MP2H

Five Memory Pointers, known as MP0, MP1L, MP1H, MP2L, MP2H, are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to is the address specified by the related Memory Pointer. MP0, together with Indirect Addressing Register, IAR0, are used to access data from Sector 0, while MP1L/MP1H together with IAR1 and MP2L/MP2H together with IAR2 are used to access data from all sectors according to the corresponding MP1H or MP2H register. Direct Addressing can be used in all sectors using the corresponding instruction which can address all available data memory space. The following example shows how to clear a section of four Data Memory locations already defined as locations `adres1` to `adres4`.

### Indirect Addressing Program Example

- **Example 1**

```
data .section 'data'
adres1 db ?
adres2 db ?
adres3 db ?
adres4 db ?
block db ?
code .section at 0 'code'
org 00h
start:
mov a,04h           ; setup size of block
mov block,a
mov a,offset adres1 ; Accumulator loaded with first RAM address
mov mp0,a          ; setup memory pointer with first RAM address
loop:
clr IAR0           ; clear the data at address defined by MP0
inc mp0            ; increment memory pointer
sdz block          ; check if last memory location has been cleared
jmp loop
continue:
:
```

• **Example 2**

```
data .section 'data'
adres1 db ?
adres2 db ?
adres3 db ?
adres4 db ?
block db ?
code .section at 0 'code'
org 00h
start:
mov a,04h           ; setup size of block
mov block,a
mov a,01h           ; setup the memory sector
mov mp1h,a
mov a,offset adres1 ; Accumulator loaded with first RAM address
mov mp1l,a          ; setup memory pointer with first RAM address
loop:
clr IAR1            ; clear the data at address defined by MP1L
inc mp1l            ; increment memory pointer MP1L
sdz block           ; check if last memory location has been cleared
jmp loop
continue:
:
```

The important point to note here is that in the example shown above, no reference is made to specific Data Memory addresses.

**Direct Addressing Program Example using extended instructions**

```
data .section 'data'
temp db ?
code .section at 0 'code'
org 00h
start:
lmov a,[m]          ; move [m] data to acc
lsub a, [m+1]        ; compare [m] and [m+1] data
snz c               ; [m]>[m+1]?
jmp continue        ; no
lmov a,[m]           ; yes, exchange [m] and [m+1] data
mov temp,a
lmov a,[m+1]
lmov [m],a
mov a,temp
lmov [m+1],a
continue:
:
```

Note: Here "m" is a data memory address located in any data memory sectors. For example, m=1F0H, it indicates address 0F0H in Sector 1.

### Program Memory Bank Pointer – PBP

For the HT67F5660 device the Program Memory is divided into several banks. Selecting the required Program Memory area is achieved using the Program Memory Bank Pointer, PBP. The PBP register should be properly configured before the device executes the "Branch" operation using the "JMP" or "CALL" instruction. After that a jump to a non-consecutive Program Memory address which is located in a certain bank selected by the program memory bank pointer bits will occur.

#### PBP Register – HT67F5660

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	PBP0
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1      Unimplemented, read as "0"  
 Bit 0      **PBP0**: Select Program Memory Banks  
             0: Program Memory Bank 0  
             1: Program Memory Bank 1

### Accumulator – ACC

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user-defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

### Program Counter Low Register – PCL

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location; however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

### Look-up Table Registers – TBLP, TBHP, TBLH

These three special function registers are used to control operation of the look-up table which is stored in the Program Memory. TBLP and TBHP are the table pointer registers and indicate the location where the table data is located. Their value must be setup before any table read commands are executed. Their value can be changed, for example using the "INC" or "DEC" instructions, allowing for easy table data pointing and reading. TBLH is the location where the high order byte of the table data is stored after a table read data instruction has been executed. Note that the lower order table data byte is transferred to a user defined location.

## **Status Register – STATUS**

This 8-bit register contains the SC flag, CZ flag, zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the "CLR WDT" or "HALT" instruction. The PDF flag is affected only by executing the "HALT" or "CLR WDT" instruction or during a system power-up.

The Z, OV, AC, C, SC and CZ flags generally reflect the status of the latest operations.

- SC is the result of the "XOR" operation which is performed by the OV flag and the MSB of the current instruction operation result.
- CZ is the operational result of different flags for different instructions. Refer to register definitions for more details.
- C is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.
- AC is set if an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
- Z is set if the result of an arithmetic or logical operation is zero; otherwise Z is cleared.
- OV is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
- PDF is cleared by a system power-up or executing the "CLR WDT" instruction. PDF is set by executing the "HALT" instruction.
- TO is cleared by a system power-up or executing the "CLR WDT" or "HALT" instruction. TO is set by a WDT time-out.

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status registers are important and if the subroutine can corrupt the status register, precautions must be taken to correctly save it.

**STATUS Register**

Bit	7	6	5	4	3	2	1	0
Name	SC	CZ	TO	PDF	OV	Z	AC	C
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	x	x	0	0	x	x	x	x

"x" unknown

- Bit 7      **SC:** The result of the "XOR" operation which is performed by the OV flag and the MSB of the instruction operation result.
- Bit 6      **CZ:** The operational result of different flags for different instructions.  
 For SUB/SUBM/LSUB/LSUBM instructions, the CZ flag is equal to the Z flag.  
 For SBC/ SBCM/ LSBC/ LSBCM instructions, the CZ flag is the "AND" operation result which is performed by the previous operation CZ flag and current operation zero flag.  
 For other instructions, the CZ flag will not be affected.
- Bit 5      **TO:** Watchdog Time-Out flag  
 0: After power up or executing the "CLR WDT" or "HALT" instruction  
 1: A watchdog time-out occurred.
- Bit 4      **PDF:** Power down flag  
 0: After power up or executing the "CLR WDT" instruction  
 1: By executing the "HALT" instruction
- Bit 3      **OV:** Overflow flag  
 0: no overflow  
 1: an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit or vice versa.
- Bit 2      **Z:** Zero flag  
 0: The result of an arithmetic or logical operation is not zero  
 1: The result of an arithmetic or logical operation is zero
- Bit 1      **AC:** Auxiliary flag  
 0: no auxiliary carry  
 1: an operation results in a carry out of the low nibbles, in addition, or no borrow from the high nibble into the low nibble in subtraction
- Bit 0      **C:** Carry flag  
 0: no carry-out  
 1: an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation  
 C is also affected by a rotate through carry instruction.

## EEPROM Data memory

These devices contain an area of internal EEPROM Data Memory. EEPROM, which stands for Electrically Erasable Programmable Read Only Memory, is by its nature a non-volatile form of re-programmable memory, with data retention even when its power supply is removed. By incorporating this kind of data memory, a whole new host of application possibilities are made available to the designer. The availability of EEPROM storage allows information such as product identification numbers, calibration values, specific user data, system setup data or other product information to be stored directly within the product microcontroller. The process of reading and writing data to the EEPROM memory has been reduced to a very trivial affair.

Device	Capacity	Address
HT67F5650	128×8	00H~7FH
HT67F5660	256×8	00H~FFH

### EEPROM Data Memory Structure

The EEPROM Data Memory capacity is 128×8 to 256×8 bits for these devices. Unlike the Program Memory and RAM Data Memory, the EEPROM Data Memory is not directly mapped into memory space and is therefore not directly addressable in the same way as the other types of memory. Read and Write operations to the EEPROM are carried out in single byte operations using an address and data register in Sector 0 and a single control register in Sector 1.

### EEPROM Registers

Three registers control the overall operation of the internal EEPROM Data Memory. These are the address register, EEA, the data register, EED and a single control register, EEC. As both the EEA and EED registers are located in all sectors, they can be directly accessed in the same way as any other Special Function Register. The EEC register, however, being located in Sector1, can be read from or written to indirectly using the MP1L/MP1H or MP2L/MP2H Memory Pointer pair and Indirect Addressing Register, IAR1/IAR2. Because the EEC control register is located at address 40H in Sector 1, the Memory Pointer low byte register, MP1L or MP2L, must first be set to the value 40H and the Memory Pointer high byte MP1H or MP2H register, set to the value, 01H, before any operations on the EEC register are executed.

Register Name	Bit							
	7	6	5	4	3	2	1	0
EEA (HT67F5650)	—	D6	D5	D4	D3	D2	D1	D0
EEA (HT67F5660)	D7	D6	D5	D4	D3	D2	D1	D0
EED	D7	D6	D5	D4	D3	D2	D1	D0
EEC	—	—	—	—	WREN	WR	RDEN	RD

EEPROM Register List

#### EEA Register – HT67F5650

Bit	7	6	5	4	3	2	1	0
Name	—	D6	D5	D4	D3	D2	D1	D0
R/W	—	R/W						
POR	—	x	x	x	x	x	x	x

"x" unknown

Bit 7 Unimplemented, read as "0"  
 Bit 6~0 **D6~D0**: Data EEPROM address  
 Data EEPROM address bit 6 ~ bit 0

**EEA Register – HT67F5660**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0     **D7~D0**: Data EEPROM address  
Data EEPROM address bit 7 ~ bit 0

**EED Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0     **D7~D0**: Data EEPROM data  
Data EEPROM data bit 7 ~ bit 0

**EEC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	WREN	WR	RDEN	RD
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4     Unimplemented, read as "0"

Bit 3     **WREN**: Data EEPROM Write Enable

0: Disable  
1: Enable

This is the Data EEPROM Write Enable Bit which must be set high before Data EEPROM write operations are carried out. Clearing this bit to zero will inhibit Data EEPROM write operations.

Bit 2     **WR**: EEPROM Write Control

0: Write cycle has finished  
1: Activate a write cycle

This is the Data EEPROM Write Control Bit and when set high by the application program will activate a write cycle. This bit will be automatically reset to zero by the hardware after the write cycle has finished. Setting this bit high will have no effect if the WREN has not first been set high.

Bit 1     **RDEN**: Data EEPROM Read Enable

0: Disable  
1: Enable

This is the Data EEPROM Read Enable Bit which must be set high before Data EEPROM read operations are carried out. Clearing this bit to zero will inhibit Data EEPROM read operations.

Bit 0     **RD**: EEPROM Read Control

0: Read cycle has finished  
1: Activate a read cycle

This is the Data EEPROM Read Control Bit and when set high by the application program will activate a read cycle. This bit will be automatically reset to zero by the hardware after the read cycle has finished. Setting this bit high will have no effect if the RDEN has not first been set high.

Note: The WREN, WR, RDEN and RD cannot be set high at the same time in one instruction. The WR and RD cannot be set high at the same time.

## **Reading Data from the EEPROM**

To read data from the EEPROM, the read enable bit, RDEN, in the EEC register must first be set high to enable the read function. The EEPROM address of the data to be read must then be placed in the EEA register. If the RD bit in the EEC register is now set high, a read cycle will be initiated. Setting the RD bit high will not initiate a read operation if the RDEN bit has not been set. When the read cycle terminates, the RD bit will be automatically cleared to zero, after which the data can be read from the EED register. The data will remain in the EED register until another read or write operation is executed. The application program can poll the RD bit to determine when the data is valid for reading.

## **Writing Data to the EEPROM**

The EEPROM address of the data to be written must first be placed in the EEA register and the data placed in the EED register. To write data to the EEPROM, the write enable bit, WREN, in the EEC register must first be set high to enable the write function. After this, the WR bit in the EEC register must be immediately set high to initiate a write cycle. These two instructions must be executed consecutively. The global interrupt bit EMI should also first be cleared before implementing any write operations, and then set again after the write cycle has started. Note that setting the WR bit high will not initiate a write cycle if the WREN bit has not been set. As the EEPROM write cycle is controlled using an internal timer whose operation is asynchronous to microcontroller system clock, a certain time will elapse before the data will have been written into the EEPROM. Detecting when the write cycle has finished can be implemented either by polling the WR bit in the EEC register or by using the EEPROM interrupt. When the write cycle terminates, the WR bit will be automatically cleared to zero by the microcontroller, informing the user that the data has been written to the EEPROM. The application program can therefore poll the WR bit to determine when the write cycle has ended.

## **Write Protection**

Protection against inadvertent write operation is provided in several ways. After these devices are powered-on the Write Enable bit in the control register will be cleared preventing any write operations. Also at power-on the Memory Pointer pairs, MP1L/MP1H and MP2L/MP2H, will be reset to zero, which means that Data Memory Sector 0 will be selected. As the EEPROM control register is located in Sector 1, this adds a further measure of protection against spurious write operations. During normal program operation, ensuring that the Write Enable bit in the control register is cleared will safeguard against incorrect write operations.

## **EEPROM Interrupt**

The EEPROM write interrupt is generated when an EEPROM write cycle has ended. The EEPROM interrupt must first be enabled by setting the DEE bit in the relevant interrupt register. However as the EEPROM is contained within a Multi-function Interrupt, the associated multi-function interrupt enable bit must also be set. When an EEPROM write cycle ends, the DEF request flag and its associated multi-function interrupt request flag will both be set. If the global, EEPROM and Multi-function interrupts are enabled and the stack is not full, a jump to the associated Multi-function Interrupt vector will take place. When the interrupt is serviced only the Multi-function interrupt flag will be automatically reset, the EEPROM interrupt flag must be manually reset by the application program. More details can be obtained in the Interrupt section.

## Programming Considerations

Care must be taken that data is not inadvertently written to the EEPROM. Protection can be enhanced by ensuring that the Write Enable bit is normally cleared to zero when not writing. Also the Memory Pointer high byte register, MP1H or MP2H, could be normally cleared to zero as this would inhibit access to Sector 1 where the EEPROM control register exist. Although certainly not necessary, consideration might be given in the application program to the checking of the validity of new write data by a simple read back process.

When writing data the WR bit must be set high immediately after the WREN bit has been set high, to ensure the write cycle executes correctly. The global interrupt bit EMI should also be cleared before a write cycle is executed and then re-enabled after the write cycle starts. Note that these devices should not enter the IDLE or SLEEP mode until the EEPROM read or write operation is totally complete. Otherwise, the EEPROM read or write operation will fail.

## Programming Examples

### • Reading data from the EEPROM – polling method

```
MOV A, EEPROM_ADRES      ; user defined address
MOV EEA, A
MOV A, 040H              ; setup memory pointer MP1L
MOV MP1L, A              ; MP1 points to EEC register
MOV A, 01H               ; setup memory pointer MP1H
MOV MP1H, A
SET IAR1.1               ; set RDEN bit, enable read operations
SET IAR1.0               ; start Read Cycle - set RD bit
BACK:
SZ IAR1.0                ; check for read cycle end
JMP BACK
CLR IAR1                  ; disable EEPROM read/write
CLR MP1H
MOV A, EED                ; move read data to register
MOV READ_DATA, A
```

### • Writing Data to the EEPROM – polling method

```
MOV A, EEPROM_ADRES      ; user defined address
MOV EEA, A
MOV A, EEPROM_DATA       ; user defined data
MOV EED, A
MOV A, 040H              ; setup memory pointer MP1L
MOV MP1L, A              ; MP1 points to EEC register
MOV A, 01H               ; setup memory pointer MP1H
MOV MP1H, A
CLR EMI
SET IAR1.3               ; set WREN bit, enable write operations
SET IAR1.2               ; start Write Cycle - set WR bit - executed immediately
                        ; after set WREN bit

SET EMI
BACK:
SZ IAR1.2                ; check for write cycle end
JMP BACK
CLR IAR1                  ; disable EEPROM read/write
CLR MP1H
```

## Oscillators

Various oscillator options offer the user a wide range of functions according to their various application requirements. The flexible features of the oscillator functions ensure that the best optimisation can be achieved in terms of speed and power saving. Oscillator selections and operation are selected through a combination of configuration options and registers.

### Oscillator Overview

In addition to being the source of the main system clock the oscillators also provide clock sources for the Watchdog Timer and Time Base Interrupts. External oscillators requiring some external components as well as fully integrated internal oscillators, requiring no external components, are provided to form a wide range of both fast and slow system oscillators. All oscillator options are selected through the configuration options. The higher frequency oscillators provide higher performance but carry with it the disadvantage of higher power requirements, while the opposite is of course true for the lower frequency oscillators. With the capability of dynamically switching between fast and slow system clock, these devices have the flexibility to optimize the performance/power ratio, a feature especially important in power sensitive portable applications.

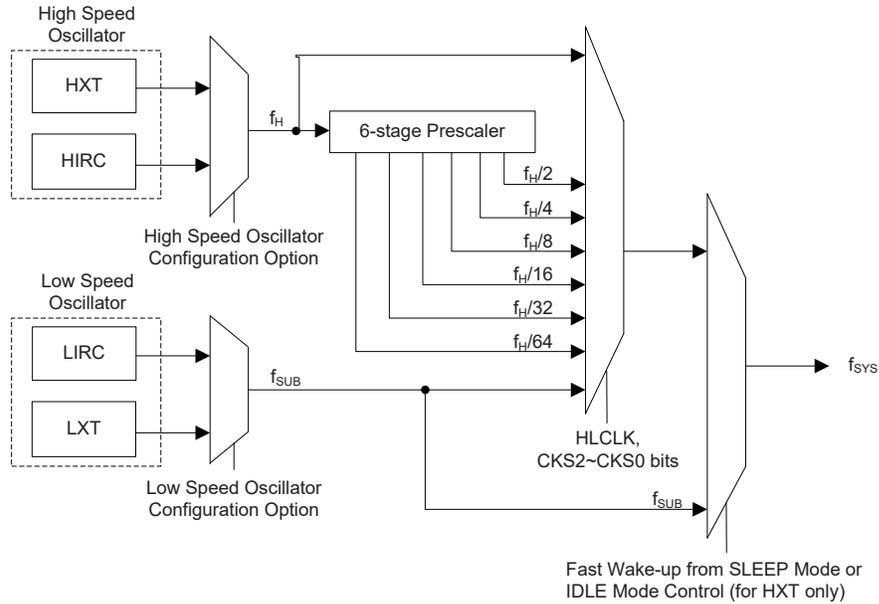
Type	Name	Frequency	Pins
External Crystal	HXT	400kHz~20MHz	OSC1/OSC2
Internal High Speed RC	HIRC	4.9152, 4.9152×2 or 4.9152×3MHz	—
External Low Speed Crystal	LXT	32.768kHz	XT1/XT2
Internal Low Speed RC	LIRC	32kHz	—

**Oscillator Types**

### System Clock Configurations

There are four methods of generating the system clock, two high speed oscillators and two low speed oscillators. The high speed oscillators are the external crystal oscillator and the internal 4.9152MHz, 4.9152×2MHz or 4.9152×3MHz RC oscillator. The two low speed oscillators are the internal 32kHz RC oscillator and the external 32.768kHz crystal oscillator. Selecting whether the low or high speed oscillator is used as the system oscillator is implemented using the HLCLK bit and CKS2~CKS0 bits in the SMOD register and as the system clock can be dynamically selected.

The actual source clock used for each of the high speed and low speed oscillators is chosen via configuration options. The frequency of the slow speed or high speed system clock is also determined using the HLCLK bit and CKS2~CKS0 bits in the SMOD register. Note that two oscillator selections must be made namely one high speed and one low speed system oscillators. It is not possible to choose a no-oscillator selection for either the high or low speed oscillator.

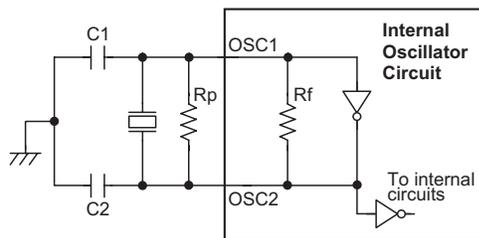


**System Clock Configurations**

### External Crystal/Ceramic Oscillator – HXT

The External Crystal/Ceramic System Oscillator is one of the high frequency oscillator choices, which is selected via configuration option. For most crystal oscillator configurations, the simple connection of a crystal across OSC1 and OSC2 will create the necessary phase shift and feedback for oscillation, without requiring external capacitors. However, for some crystal types and frequencies, to ensure oscillation, it may be necessary to add two small value capacitors, C1 and C2. Using a ceramic resonator will usually require two small value capacitors, C1 and C2, to be connected as shown for oscillation to occur. The values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer’s specification.

For oscillator stability and to minimise the effects of noise and crosstalk, it is important to ensure that the crystal and any associated resistors and capacitors along with interconnecting lines are all located as close to the MCU as possible.



- Note: 1.  $R_p$  is normally not required. C1 and C2 are required.  
 2. Although not shown OSC1/OSC2 pins have a parasitic capacitance of around 7pF.

### Crystal/Resonator Oscillator – HXT

Crystal Oscillator C1 and C2 Values		
Crystal Frequency	C1	C2
20MHz	0pF	0pF
12MHz	0pF	0pF
8MHz	0pF	0pF
4MHz	0pF	0pF
1MHz	100pF	100pF

Note: C1 and C2 values are for guidance only.

**Crystal Recommended Capacitor Values**

**Internal RC Oscillator – HIRC**

The internal RC oscillator is a fully integrated system oscillator requiring no external components. The internal RC oscillator has three fixed frequencies of either 4.9152MHz, 4.9152×2MHz or 4.9152×3MHz. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised. Note that if this internal system clock option is selected, as it requires no external pins for its operation, I/O pins PB1 and PB2 are free for use as normal I/O pins.

**Internal 32kHz Oscillator – LIRC**

The Internal 32kHz System Oscillator is one of the low frequency oscillator choices, which is selected via configuration option. It is a fully integrated RC oscillator with a typical frequency of 32kHz at 5V, requiring no external components for its implementation. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised.

**External 32.768kHz Crystal Oscillator – LXT**

The External 32.768kHz Crystal System Oscillator is one of the low frequency oscillator choices, which is selected via configuration option. This clock source has a fixed frequency of 32.768kHz and requires a 32.768kHz crystal to be connected between pins XT1 and XT2. The external resistor and capacitor components connected to the 32.768kHz crystal are necessary to provide oscillation. For applications where precise frequencies are essential, these components may be required to provide frequency compensation due to different crystal manufacturing tolerances. During power-up there is a time delay associated with the LXT oscillator waiting for it to start-up.

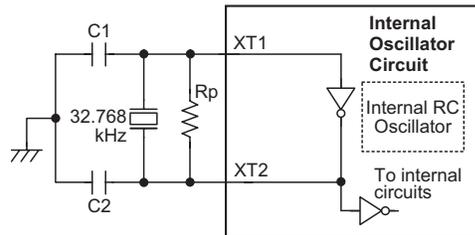
When the microcontroller enters the SLEEP or IDLE Mode, the system clock is switched off to stop microcontroller activity and to conserve power. However, in many microcontroller applications it may be necessary to keep the internal timers operational even when the microcontroller is in the SLEEP or IDLE Mode. To do this, another clock, independent of the system clock, must be provided.

However, for some crystals, to ensure oscillation and accurate frequency generation, it is necessary to add two small value external capacitors, C1 and C2. The exact values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer specification. The external parallel feedback resistor, R<sub>F</sub>, is required.

Some configuration options determine if the XT1/XT2 pins are used for the LXT oscillator or as I/O pins.

- If the LXT oscillator is not used for any clock source, the XT1/XT2 pins can be used as normal I/O pins.
- If the LXT oscillator is used for any clock source, the 32.768kHz crystal should be connected to the XT1/XT2 pins.

For oscillator stability and to minimise the effects of noise and crosstalk, it is important to ensure that the crystal and any associated resistors and capacitors along with interconnecting lines are all located as close to the MCU as possible.



- Note: 1. Rp, C1 and C2 are required.  
2. Although not shown pins have a parasitic capacitance of around 7pF.

**External LXT Oscillator**

LXT Oscillator C1 and C2 Values		
Crystal Frequency	C1	C2
32.768kHz	10pF	10pF
Note: 1. C1 and C2 values are for guidance only. 2. Rp=5M~10MΩ is recommended.		

**32.768kHz Crystal Recommended Capacitor Values**

**LXT Oscillator Low Power Function**

The LXT oscillator can function in one of two modes, the Quick Start Mode and the Low Power Mode. The mode selection is executed using the LXTLP bit in the TBC register.

LXTLP Bit	LXT Mode
0	Quick Start
1	Low-power

After power on, the LXTLP bit will be automatically cleared to zero ensuring that the LXT oscillator is in the Quick Start operating mode. In the Quick Start Mode the LXT oscillator will power up and stabilise quickly. However, after the LXT oscillator has fully powered up it can be placed into the Low-power mode by setting the LXTLP bit high. The oscillator will continue to run but with reduced current consumption, as the higher current consumption is only required during the LXT oscillator start-up. In power sensitive applications, such as battery applications, where power consumption must be kept to a minimum, it is therefore recommended that the application program sets the LXTLP bit high about 2 seconds after power-on.

It should be noted that, no matter what condition the LXTLP bit is set to, the LXT oscillator will always be function normally, the only difference is that it will take more time to start up if in the Low-power mode.

**Supplementary Oscillators**

The low speed oscillators, in addition to providing a system clock source are also used to provide a clock source to four other device functions. These are the Watchdog Timer, the Time Base Interrupts function, the LCD driver, and the SIM.

## Operating Modes and System Clocks

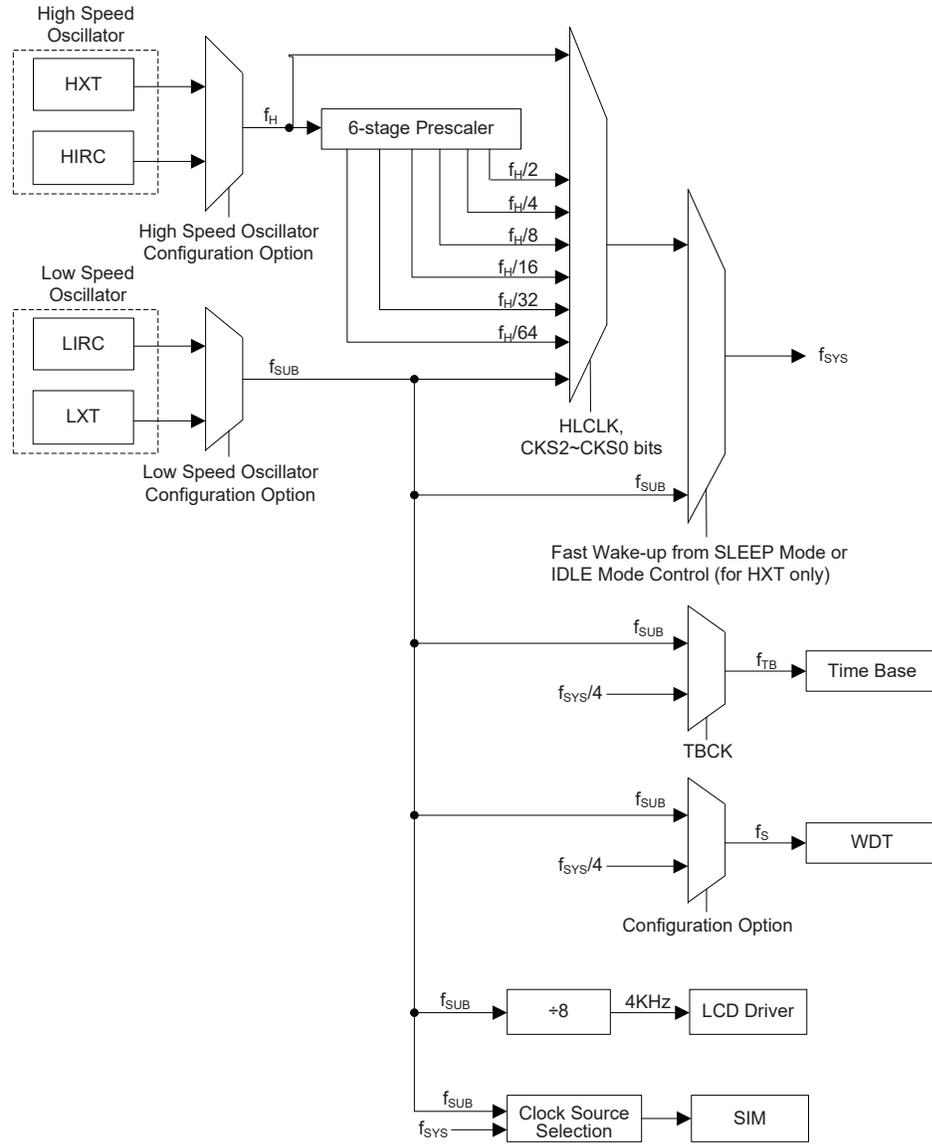
Present day applications require that their microcontrollers have high performance but often still demand that they consume as little power as possible, conflicting requirements that are especially true in battery powered portable applications. The fast clocks required for high performance will by their nature increase current consumption and of course vice-versa, lower speed clocks reduce current consumption. As Holtek has provided these devices with both high and low speed clock sources and the means to switch between them dynamically, the user can optimise the operation of their microcontroller to achieve the best performance/power ratio.

### System Clocks

These devices have many different clock sources for both the CPU and peripheral function operation. By providing the user with a wide range of clock options using configuration options and register programming, a clock system can be configured to obtain maximum application performance.

The main system clock, can come from either a high frequency  $f_H$  or low frequency  $f_{SUB}$  source, and is selected using the HLCLK bit and CKS2~CKS0 bits in the SMOD register. The high speed system clock can be sourced from either an HXT or HIRC oscillator, selected via a configuration option. The low speed system clock source can be sourced from internal clock  $f_{SUB}$ . If  $f_{SUB}$  is selected then it can be sourced by either the LXT or LIRC oscillator, selected via a configuration option. The other choice, which is a divided version of the high speed system oscillator has a range of  $f_H/2 \sim f_H/64$ .

The  $f_{SUB}$  clock is used to provide a substitute clock for the microcontroller just after a wake-up has occurred to enable faster wake-up times. The  $f_{SUB}$  is used as a clock source for the Watchdog timer, the Time Base interrupt, the TMs, the LCD and the SIM functions.



**System Clock Configurations**

Note: When the system clock source  $f_{SYS}$  is switched to  $f_{SUB}$  from  $f_H$ , the high speed oscillation will stop to conserve the power. Thus there is no  $f_H \sim f_H/64$  for peripheral circuit to use.

## System Operation Modes

There are six different modes of operation for the microcontroller, each one with its own special characteristics and which can be chosen according to the specific performance and power requirements of the application. There are two modes allowing normal operation of the microcontroller, the NORMAL Mode and SLOW Mode. The remaining four modes, the SLEEP0, SLEEP1, IDLE0 and IDLE1 Mode are used when the microcontroller CPU is switched off to conserve power.

Operating Mode	Description			
	CPU	f <sub>sys</sub>	f <sub>sub</sub>	f <sub>s</sub>
NORMAL Mode	on	f <sub>H</sub> ~f <sub>H</sub> /64	on	on
SLOW Mode	on	f <sub>sub</sub>	on	on
IDLE0 Mode	off	off	on	on/off
IDLE1 Mode	off	on	on	on
SLEEP0 Mode	off	off	off	off
SLEEP1 Mode	off	off	on	on

### NORMAL Mode

As the name suggests this is one of the main operating modes where the microcontroller has all of its functions operational and where the system clock is provided by one of the high speed oscillators. This mode operates allowing the microcontroller to operate normally with a clock source will come from one of the high speed oscillators, either the HXT or HIRC oscillators. The high speed oscillator will however first be divided by a ratio ranging from 1 to 64, the actual ratio being selected by the CKS2~CKS0 and HLCLK bits in the SMOD register. Although a high speed oscillator is used, running the microcontroller at a divided clock ratio reduces the operating current.

### SLOW Mode

This is also a mode where the microcontroller operates normally although now with a slower speed clock source. The clock source used will be from one of the low speed oscillators, either the LXT or the LIRC. Running the microcontroller in this mode allows it to run with much lower operating currents. In the SLOW Mode, the f<sub>H</sub> is off.

### SLEEP0 Mode

The SLEEP Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is low. In the SLEEP0 mode the CPU will be stopped, and the f<sub>sub</sub> and f<sub>s</sub> clocks will be stopped too, and the Watchdog Timer function is disabled. In this mode, the LVDEN is must cleared to zero. If the LVDEN is set high, it won't enter the SLEEP0 Mode. In this mode, the ENLCD is must cleared to zero. If the ENLCD is set high, it won't enter the SLEEP0 Mode.

### SLEEP1 Mode

The SLEEP Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is low. In the SLEEP1 mode the CPU will be stopped. However the f<sub>sub</sub> and f<sub>s</sub> clocks will continue to operate if the LVDEN is "1" or the ENLCD is "1" or the Watchdog Timer function is enabled and if its clock source is chosen via configuration option to come from the f<sub>sub</sub>.

### IDLE0 Mode

The IDLE0 Mode is entered when a HALT instruction is executed and when the IDLEN bit in the SMOD register is high and the FSYSON bit in the CTRL register is low. In the IDLE0 Mode the system oscillator will be inhibited from driving the CPU but some peripheral functions will remain operational such as the Watchdog Timer, TMs, LCD driver and SIM. In the IDLE0 Mode, the system oscillator will be stopped. In the IDLE0 Mode the Watchdog Timer clock,  $f_s$ , will either be on or off depending upon the  $f_s$  clock source. If the WDT clock source selects  $f_{SYS}/4$  then the  $f_s$  clock will be off, and if the source comes from  $f_{SUB}$  then  $f_s$  will be on.

### IDLE1 Mode

The IDLE1 Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is high and the FSYSON bit in the CTRL register is high. In the IDLE1 Mode the system oscillator will be inhibited from driving the CPU but may continue to provide a clock source to keep some peripheral functions operational such as the Watchdog Timer, TMs, LCD driver and SIM. In the IDLE1 Mode, the system oscillator will continue to run, and this system oscillator may be high speed or low speed system oscillator. In the IDLE1 Mode the Watchdog Timer clock,  $f_s$ , will be on.

## Control Register

The registers, SMOD and CTRL, are used for overall control of the internal clocks within these devices.

### SMOD Register

Bit	7	6	5	4	3	2	1	0
Name	CKS2	CKS1	CKS0	FSTEN	LTO	HTO	IDLEN	HLCLK
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	0	0	0	1	1

Bit 7~5 **CKS2~CKS0:** The system clock selection when HLCLK is "0"

000:  $f_{SUB}$  ( $f_{LXT}$  or  $f_{LIRC}$ )

001:  $f_{SUB}$  ( $f_{LXT}$  or  $f_{LIRC}$ )

010:  $f_H/64$

011:  $f_H/32$

100:  $f_H/16$

101:  $f_H/8$

110:  $f_H/4$

111:  $f_H/2$

These three bits are used to select which clock is used as the system clock source. In addition to the system clock source, which can be either the LXT or LIRC, a divided version of the high speed system oscillator can also be chosen as the system clock source.

Bit 4 **FSTEN:** Fast Wake-up Control (only for HXT)

0: Disable

1: Enable

This is the Fast Wake-up Control bit which determines if the  $f_{SUB}$  clock source is initially used after the device wakes up. When the bit is high, the  $f_{SUB}$  clock source can be used as a temporary system clock to provide a faster wake up time as the  $f_{SUB}$  clock is available.

- Bit 3     **LTO**: Low speed system oscillator ready flag  
           0: Not ready  
           1: Ready  
 This is the low speed system oscillator ready flag which indicates when the low speed system oscillator is stable after power on reset or a wake-up has occurred. The flag will be low when in the SLEEP0 Mode but after a wake-up has occurred, the flag will change to a high level after 1024 clock cycles if the LXT oscillator is used and 1~2 clock cycles if the LIRC oscillator is used.
- Bit 2     **HTO**: High speed system oscillator ready flag  
           0: Not ready  
           1: Ready  
 This is the high speed system oscillator ready flag which indicates when the high speed system oscillator is stable. This flag is cleared to zero by hardware when the device is powered on and then changes to a high level after the high speed system oscillator is stable.  
 Therefore this flag will always be read as "1" by the application program after device power-on. The flag will be low when in the SLEEP or IDLE0 Mode but after a wake-up has occurred, the flag will change to a high level after 1024 clock cycles if the HXT oscillator is used and after 15~16 clock cycles if the HIRC oscillator is used.
- Bit 1     **IDLEN**: IDLE Mode control  
           0: Disable  
           1: Enable  
 This is the IDLE Mode Control bit and determines what happens when the HALT instruction is executed. If this bit is high, when a HALT instruction is executed the device will enter the IDLE Mode. In the IDLE1 Mode the CPU will stop running but the system clock will continue to keep the peripheral functions operational, if FSYSON bit is high. If FSYSON bit is low, the CPU and the system clock will all stop in IDLE0 mode. If the bit is low the device will enter the SLEEP Mode when a HALT instruction is executed.
- Bit 0     **HLCLK**: system clock selection  
           0:  $f_H/2 \sim f_H/64$  or  $f_{SUB}$   
           1:  $f_H$   
 This bit is used to select if the  $f_H$  clock or the  $f_H/2 \sim f_H/64$  or  $f_{SUB}$  clock is used as the system clock. When the bit is high the  $f_H$  clock will be selected and if low the  $f_H/2 \sim f_H/64$  or  $f_{SUB}$  clock will be selected. When system clock switches from the  $f_H$  clock to the  $f_{SUB}$  clock and the  $f_H$  clock will be automatically switched off to conserve power.

**CTRL Register**

Bit	7	6	5	4	3	2	1	0
Name	FSYSON	—	—	—	—	LVRF	LRF	WRF
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	x	0	0

"x" unknown

- Bit 7     **FSYSON**:  $f_{SYS}$  Control in IDLE Mode  
           0: Disable  
           1: Enable
- Bit 6~3   Unimplemented, read as "0"
- Bit 2     **LVRF**: LVR function reset flag  
 Described elsewhere.
- Bit 1     **LRF**: LVR Control register software reset flag  
 Described elsewhere.
- Bit 0     **WRF**: WDT Control register software reset flag  
 Described elsewhere.

### Fast Wake-up

To minimise power consumption these devices can enter the SLEEP or IDLE0 Mode, where the system clock source to these devices will be stopped. However when these devices are woken up again, they can take a considerable time for the original system oscillator to restart, stabilise and allow normal operation to resume. To ensure these devices are up and running as fast as possible a Fast Wake-up function is provided, which allows  $f_{SUB}$ , namely either the LXT or LIRC oscillator, to act as a temporary clock to first drive the system until the original system oscillator has stabilised. As the clock source for the Fast Wake-up function is  $f_{SUB}$ , the Fast Wake-up function is only available in the SLEEP1 and IDLE0 modes. When these devices are woken up from the SLEEP0 mode, the Fast Wake-up function has no effect because the  $f_{SUB}$  clock is stopped. The Fast Wake-up enable/disable function is controlled using the FSTEN bit in the SMOD register.

If the HXT oscillator is selected as the NORMAL Mode system clock, and if the Fast Wake-up function is enabled, then it will take one to two  $t_{SUB}$  clock cycles of the LIRC or LXT oscillator for the system to wake-up. The system will then initially run under the  $f_{SUB}$  clock source until 1024 HXT clock cycles have elapsed, at which point the HTO flag will switch high and the system will switch over to operating from the HXT oscillator.

If the HIRC oscillator or LIRC oscillator is used as the system oscillator then it will take 15~16 clock cycles of the HIRC or 1~2 cycles of the LIRC to wake up the system from the SLEEP or IDLE0 Mode. The Fast Wake-up bit, FSTEN will have no effect in these cases.

System Oscillator	FSTEN Bit	Wake-up Time (SLEEP0 Mode)	Wake-up Time (SLEEP1 Mode)	Wake-up Time (IDLE0 Mode)	Wake-up Time (IDLE1 Mode)
HXT	0	1024 HXT cycles	1024 HXT cycles		1~2 HXT cycles
	1	1024 HXT cycles	1~2 $f_{SUB}$ cycles (System runs with $f_{SUB}$ first for 1024 HXT cycles and then switches over to run with the HXT clock)		1~2 HXT cycles
HIRC	x	15~16 HIRC cycles	15~16 HIRC cycles		1~2 HIRC cycles
LIRC	x	1~2 LIRC cycles	1~2 LIRC cycles		1~2 LIRC cycles
LXT	x	1024 LXT cycles	1024 LXT cycles		1~2 LXT cycles

"x": don't care

#### Wake-Up Times

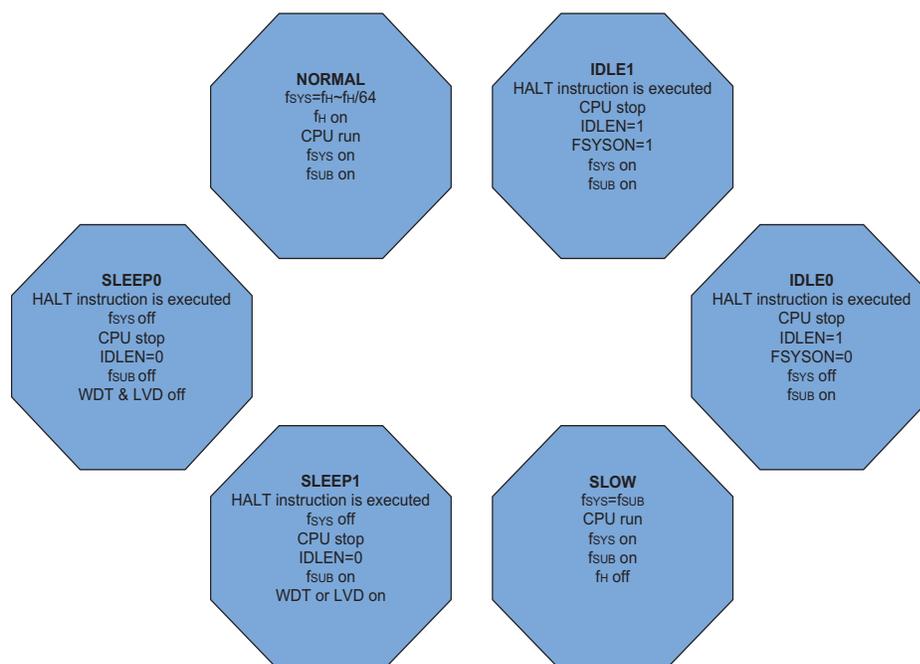
Note that if the Watchdog Timer is disabled, which means that the LXT and LIRC are all both off, then there will be no Fast Wake-up function available when these devices wake-up from the SLEEP0 Mode.

## Operating Mode Switching

These devices can switch between operating modes dynamically allowing the user to select the best performance/power ratio for the present task in hand. In this way microcontroller operations that do not require high performance can be executed using slower clocks thus requiring less operating current and prolonging battery life in portable applications.

In simple terms, Mode Switching between the NORMAL Mode and SLOW Mode is executed using the HLCLK bit and CKS2~CKS0 bits in the SMOD register while Mode Switching from the NORMAL/SLOW Modes to the SLEEP/IDLE Modes is executed via the HALT instruction. When a HALT instruction is executed, whether these devices enter the IDLE Mode or the SLEEP Mode is determined by the condition of the IDLEN bit in the SMOD register and FSYSON in the CTRL register.

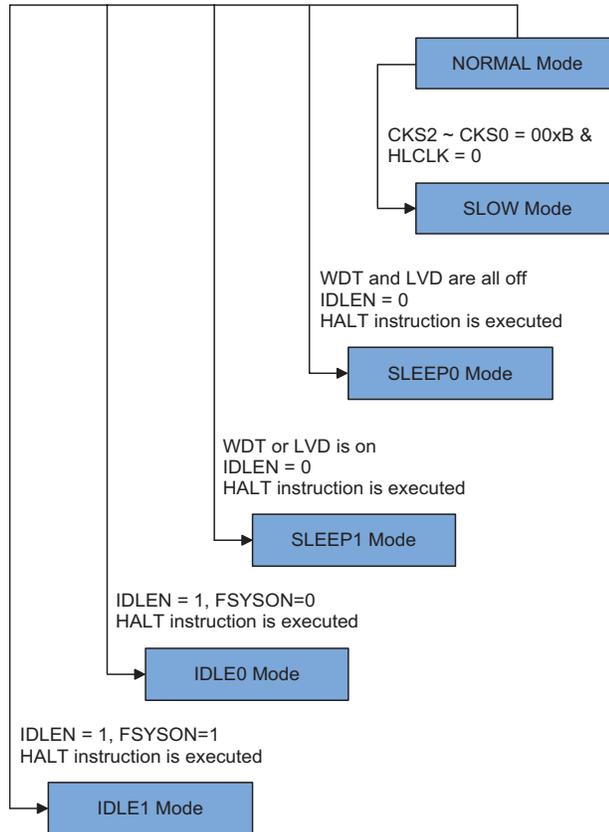
When the HLCLK bit switches to a low level, which implies that clock source is switched from the high speed clock source,  $f_H$ , to the clock source,  $f_H/2 \sim f_H/64$  or  $f_{SUB}$ . If the clock is from the  $f_{SUB}$ , the high speed clock source will stop running to conserve power. When this happens it must be noted that the  $f_H/16$  and  $f_H/64$  internal clock sources will also stop running, which may affect the operation of other internal functions such as the TMs and the SIM. The accompanying flowchart shows what happens when these devices move between the various operating modes.



**NORMAL Mode to SLOW Mode Switching**

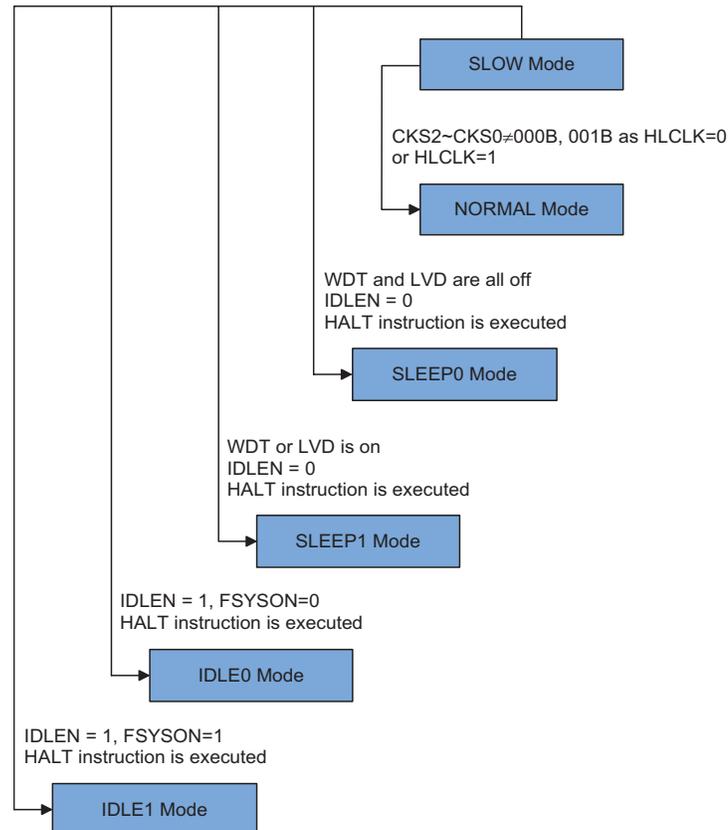
When running in the NORMAL Mode, which uses the high speed system oscillator, and therefore consumes more power, the system clock can switch to run in the SLOW Mode by set the HLCLK bit to "0" and set the CKS2~CKS0 bits to "000" or "001" in the SMOD register. This will then use the low speed system oscillator which will consume less power. Users may decide to do this for certain operations which do not require high performance and can subsequently reduce power consumption.

The SLOW Mode is sourced from the LXT or the LIRC oscillators and therefore requires these oscillators to be stable before full mode switching occurs. This is monitored using the LTO bit in the SMOD register.



### SLOW Mode to NORMAL Mode Switching

In SLOW Mode the system uses either the LXT or LIRC low speed system oscillator. To switch back to the NORMAL Mode, where the high speed system oscillator is used, the HLCLK bit should be set high or HLCLK bit is "0", but CKS2~CKS0 is set to "010", "011", "100", "101", "110" or "111". As a certain amount of time will be required for the high frequency clock to stabilise, the status of the HTO bit is checked. The amount of time required for high speed system oscillator stabilization depends upon which high speed system oscillator type is used.



### Entering the SLEEP0 Mode

There is only one way for these devices to enter the SLEEP0 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "0" and the WDT, LVD and LCD all off. When this instruction is executed under the conditions described above, the following will occur:

- The system clock and the  $f_{SUB}$  clock will be stopped and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and stopped no matter if the WDT clock source originates from the  $f_{SUB}$  clock or from the system clock.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

### Entering the SLEEP1 Mode

There is only one way for these devices to enter the SLEEP1 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "0" and the WDT or LVD on. When this instruction is executed under the conditions described above, the following will occur:

- The system clock will be stopped and the application program will stop at the "HALT" instruction, but the WDT or LVD will remain with the clock source coming from the  $f_{SUB}$  clock.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT clock source is selected to come from the  $f_{SUB}$  clock as the WDT is enabled.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

### Entering the IDLE0 Mode

There is only one way for these devices to enter the IDLE0 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "1" and the FSYSON bit in CTRL register equal to "0". When this instruction is executed under the conditions described above, the following will occur:

- The system clock will be stopped and the application program will stop at the "HALT" instruction, but the  $f_{SUB}$  clock will be on.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT clock source is selected to come from the  $f_{SUB}$  clock and the WDT is enabled. The WDT will stop if its clock source originates from the system clock.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

### Entering the IDLE1 Mode

There is only one way for these devices to enter the IDLE1 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "1" and the FSYSON bit in CTRL register equal to "1". When this instruction is executed under the conditions described above, the following will occur:

- The system clock and the  $f_{SUB}$  clock will be on and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT is enabled regardless of the WDT clock source which originates from the  $f_{SUB}$  clock or from the system clock.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

## Standby Current Considerations

As the main reason for entering the SLEEP or IDLE Mode is to keep the current consumption of these devices to as low a value as possible, perhaps only in the order of several micro-amps except in the IDLE1 Mode, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised. Special attention must be made to the I/O pins on these devices. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. This also applies to these devices which have different package types, as there may be unbonded pins. These must either be setup as outputs or if setup as inputs must have pull-high resistors connected.

Care must also be taken with the loads, which are connected to I/O pins, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs. Also note that additional standby current will also be required if the configuration options have enabled the LXT or LIRC oscillator.

In the IDLE1 Mode the system oscillator is on, if the system oscillator is from the high speed system oscillator, the additional standby current will also be perhaps in the order of several hundred micro-amps.

## Wake-up

After the system enters the SLEEP or IDLE Mode, it can be woken up from one of various sources listed as follows:

- An external falling edge on Port A
- A system interrupt
- A WDT overflow

If these devices are woken up by a WDT overflow, a Watchdog Timer reset will be initiated. The PDF flag is cleared by a system power-up or executing the clear Watchdog Timer instructions and is set when executing the "HALT" instruction. The TO flag is set if a WDT time-out occurs, and causes a wake-up that only resets the Program Counter and Stack Pointer, the other flags remain in their original status.

Each pin on Port A can be setup using the PAWU register to permit a negative transition on the pin to wake-up the system. When a Port A pin wake-up occurs, the program will resume execution at the instruction following the "HALT" instruction. If the system is woken up by an interrupt, then two possible situations may occur. The first is where the related interrupt is disabled or the interrupt is enabled but the stack is full, in which case the program will resume execution at the instruction following the "HALT" instruction. In this situation, the interrupt which woke-up these devices will not be immediately serviced, but will rather be serviced later when the related interrupt is finally enabled or when a stack level becomes free. The other situation is where the related interrupt is enabled and the stack is not full, in which case the regular interrupt response takes place. If an interrupt request flag is set high before entering the SLEEP or IDLE Mode, the wake-up function of the related interrupt will be disabled.

### Programming Considerations

The HXT and LXT oscillators both use the same SST counter. For example, if the system is woken up from the SLEEP0 Mode and both the HXT and LXT oscillators need to start-up from an off state. The LXT oscillator uses the SST counter after HXT oscillator has finished its SST period.

- If these devices are woken up from the SLEEP0 Mode to the NORMAL Mode, the high speed system oscillator needs an SST period. The devices will execute first instruction after HTO is "1". At this time, the LXT oscillator may not be stability if  $f_{SUB}$  is from LXT oscillator. The same situation occurs in the power-on state. The LXT oscillator is not ready yet when the first instruction is executed.
- If these devices are woken up from the SLEEP1 Mode to NORMAL Mode, and the system clock source is from HXT oscillator and FSTEN is "1", the system clock can be switched to the LXT or LIRC oscillator after wake up.
- There are peripheral functions, such as WDT, TMs, LCD driver and SIM, for which the  $f_{SYS}$  is used. If the system clock source is switched from  $f_H$  to  $f_{SUB}$ , the clock source to the peripheral functions mentioned above will change accordingly.

## Watchdog Timer

The Watchdog Timer is provided to prevent program malfunctions or sequences from jumping to unknown locations, due to certain uncontrollable external events such as electrical noise.

### Watchdog Timer Clock Source

The Watchdog Timer clock source is provided by the internal clock,  $f_s$ , which is in turn supplied by one of two sources selected by configuration option:  $f_{SUB}$  or  $f_{SYS}/4$ . The  $f_{SUB}$  clock can be sourced from either the LXT or LIRC oscillators, again chosen via a configuration option. The Watchdog Timer source clock is then subdivided by a ratio of  $2^8$  to  $2^{18}$  to give longer timeouts, the actual value being chosen using the WS2~WS0 bits in the WDTC register. The LIRC internal oscillator has an approximate period of 32kHz at a supply voltage of 5V. However, it should be noted that this specified internal clock period can vary with  $V_{DD}$ , temperature and process variations. The LXT oscillator is supplied by an external 32.768kHz crystal. The other Watchdog Timer clock source option is the  $f_{SYS}/4$  clock.

### Watchdog Timer Control Register

A single register, WDTC, controls the required timeout period as well as the enable/disable operation. This register together with several configuration options control the overall operation of the Watchdog Timer.

#### WDTC Register

Bit	7	6	5	4	3	2	1	0
Name	WE4	WE3	WE2	WE1	WE0	WS2	WS1	WS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	0	1	1

Bit 7~3 **WE4~WE0**: WDT function software control

If the WDT configuration option is "always enable":

10101 or 01010: Enable

Others: Reset MCU

If the WDT configuration option is "controlled by the WDT control register":

10101: Disable

01010: Enable

Others: Reset MCU

When these bits are changed by the environmental noise or software setting to reset the microcontroller, the reset operation will be activated after 2~3 LIRC clock cycles and the WRF bit in the CTRL register will be set high.

Bit 2~0 **WS2~WS0**: WDT time-out period selection

000:  $2^8/f_s$

001:  $2^{10}/f_s$

010:  $2^{12}/f_s$

011:  $2^{14}/f_s$

100:  $2^{15}/f_s$

101:  $2^{16}/f_s$

110:  $2^{17}/f_s$

111:  $2^{18}/f_s$

### CTRL Register

Bit	7	6	5	4	3	2	1	0
Name	FSYSON	—	—	—	—	LVRF	LRF	WRF
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	x	0	0

"x" unknown

Bit 7      **FSYSON**:  $f_{SYS}$  Control in IDLE Mode  
Described elsewhere.

Bit 6~3    Unimplemented, read as "0"

Bit 2      **LVRF**: LVR function reset flag  
Described elsewhere.

Bit 1      **LRF**: LVR Control register software reset flag  
Described elsewhere.

Bit 0      **WRF**: WDT Control register software reset flag  
0: Not occur  
1: Occurred

This bit is set high by the WDT Control register software reset and cleared by the application program. Note that this bit can only be cleared to zero by the application program.

### Watchdog Timer Operation

The Watchdog Timer operates by providing a device reset when its timer overflows. This means that in the application program and during normal operation the user has to strategically clear the Watchdog Timer before it overflows to prevent the Watchdog Timer from executing a reset. This is done using the clear watchdog instructions. If the program malfunctions for whatever reason, jumps to an unknown location, or enters an endless loop, these clear instructions will not be executed in the correct manner, in which case the Watchdog Timer will overflow and reset the device. Some of the Watchdog Timer options, such as always on select and clock source are selected using configuration options. With regard to the Watchdog Timer enable/disable function, there are also five bits, WE4~WE0, in the WDTC register to offer additional enable/disable and reset control of the Watchdog Timer. If the WDT configuration option is determined that the WDT function is always enabled, the WE4~WE0 bits still have effects on the WDT function. When the WE4~WE0 bits value is equal to 01010B or 10101B, the WDT function is enabled. However, if the WE4~WE0 bits are changed to any other values except 01010B and 10101B, which is caused by the environmental noise or software setting, it will reset the microcontroller after 2~3 LIRC clock cycles. If the WDT configuration option is determined that the WDT function is controlled by the WDT control register, the WE4~WE0 values can determine which mode the WDT operates in. The WDT function will be disabled when the WE4~WE0 bits are set to a value of 10101B. The WDT function will be enabled if the WE4~WE0 bits value is equal to 01010B. If the WE4~WE0 bits are set to any other values by the environmental noise or software setting, except 01010B and 10101B, it will reset the device after 2~3 LIRC clock cycles. After power on these bits will have the value of 01010B.

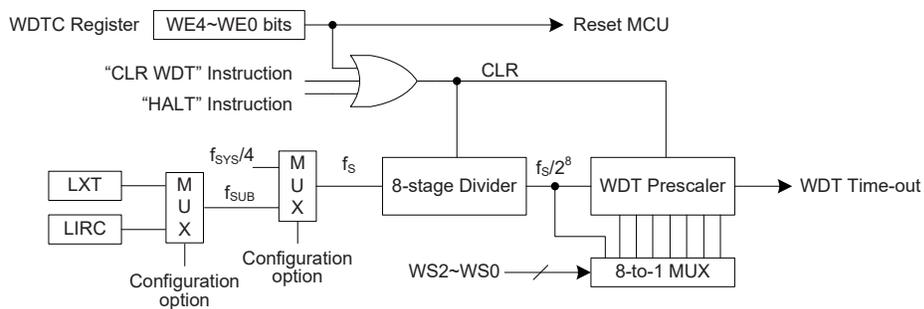
WDT Configuration Option	WE4 ~ WE0 Bits	WDT Function
Always Enable	01010B or 10101B	Enable
	Any other values	Reset MCU
Controlled by WDT Control Register	10101B	Disable
	01010B	Enable
	Any other values	Reset MCU

**Watchdog Timer Enable/Disable Control**

Under normal program operation, a Watchdog Timer time-out will initialise a device reset and set the status bit TO. However, if the system is in the SLEEP or IDLE Mode, when a Watchdog Timer time-out occurs, the TO bit in the status register will be set and only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the contents of the Watchdog Timer. The first is a WDT reset, which means a certain value except 01010B and 10101B written into the WE4~WE0 bit filed, the second is using the Watchdog Timer software clear instructions and the third is via a HALT instruction.

There is only one method of using software instruction to clear the Watchdog Timer. That is to use the single "CLR WDT" instruction to clear the WDT.

The maximum time out period is when the  $2^{18}$  division ratio is selected. As an example, with a 32kHz LIRC oscillator as its source clock, this will give a maximum watchdog period of around 8 second for the  $2^{18}$  division ratio, and a minimum timeout of 7.8ms for the  $2^8$  division ratio.



**Watchdog Timer**

## Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that the device can be set to some predetermined condition irrespective of outside parameters. The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well-defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program commences. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

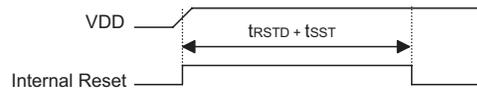
Another type of reset is when the Watchdog Timer overflows and resets. All types of reset operations result in different register conditions being setup. Another reset exists in the form of a Low Voltage Reset, LVR, where a full reset, is implemented in situations where the power supply voltage falls below a certain threshold.

### Reset Functions

There are four ways in which a reset can occur, through events occurring internally:

#### Power-on Reset

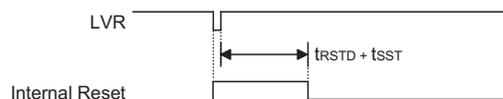
The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all I/O ports will be first set to inputs.



**Power-On Reset Timing Chart**

#### Low Voltage Reset – LVR

The microcontrollers contain a low voltage reset circuit in order to monitor the supply voltage of the devices. The LVR function is always enabled with a specific LVR voltage  $V_{LVR}$ . If the supply voltage of the devices drops to within a range of  $0.9V \sim V_{LVR}$  such as might occur when changing the battery, the LVR will automatically reset the devices internally and the LVRF bit in the CTRL register will also be set high. For a valid LVR signal, a low supply voltage, i.e., a voltage in the range between  $0.9V \sim V_{LVR}$  must exist for a time greater than that specified by  $t_{LVR}$  in the A.C. characteristics. If the low supply voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function. The actual  $V_{LVR}$  value can be selected by the LVS bits in the LVRC register. If the LVS7~LVS0 bits are changed to some certain values by the environmental noise or software setting, the LVR will reset the devices after 2~3 LIRC clock cycles. When this happens, the LRF bit in the CTRL register will be set high. After power on the register will have the value of 01010101B. Note that the LVR function will be automatically disabled when the devices enter the power down mode.



**Low Voltage Reset Timing Chart**

• **LVRC Register**

Bit	7	6	5	4	3	2	1	0
Name	LVS7	LVS6	LVS5	LVS4	LVS3	LVS2	LVS1	LVS0
R/W								
POR	0	1	0	1	0	1	0	1

Bit 7~0 **LVS7~LVS0**: LVR voltage select

01010101: 2.1V

00110011: 2.55V

10011001: 3.15V

10101010: 3.8V

Other values: Reset MCU (register is reset to POR value).

When an actual low voltage condition occurs, as specified by one of the four defined LVR voltage values above, an MCU reset will be generated. The reset operation will be activated after 2~3 LIRC clock cycles. In this situation the register contents will remain the same after such a reset occurs.

Any register value, other than the four defined LVR values above, will also result in the generation of an MCU reset. The reset operation will be activated after 2~3 LIRC clock cycles. However in this situation the register contents will be reset to the POR value.

• **CTRL Register**

Bit	7	6	5	4	3	2	1	0
Name	FSYSON	—	—	—	—	LVRF	LRF	WRF
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	x	0	0

"x" unknown

Bit 7 **FSYSON**:  $f_{SYS}$  Control in IDLE Mode

Described elsewhere.

Bit 6~3 Unimplemented, read as "0"

Bit 2 **LVRF**: LVR function reset flag

0: not occur

1: occurred

This bit is set high when a specific Low Voltage Reset situation condition occurs. This bit can only be cleared to zero by the application program.

Bit 1 **LRF**: LVR Control register software reset flag

0: not occur

1: occurred

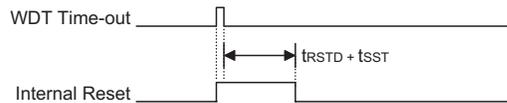
This bit is set high if the LVRC register contains any non-defined LVR voltage register values. This in effect acts like a software-reset function. This bit can only be cleared to zero by the application program.

Bit 0 **WRF**: WDT Control register software reset flag

Described elsewhere.

### Watchdog Time-out Reset during Normal Operation

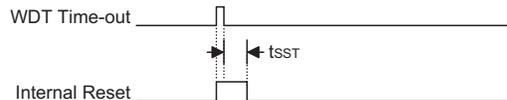
The Watchdog time-out Reset during normal operation is the same as LVR reset except that the Watchdog time-out flag TO will be set high.



**WDT Time-out Reset during Normal Operation Timing Chart**

### Watchdog Time-out Reset during SLEEP or IDLE Mode

The Watchdog time-out Reset during SLEEP or IDLE Mode is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to zero and the TO flag will be set high. Refer to the A.C. Characteristics for  $t_{SST}$  details.



**WDT Time-out Reset during Sleep or IDLE Timing Chart**

### Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the SLEEP or IDLE Mode function or Watchdog Timer. The reset flags are shown in the table:

TO	PDF	Reset Conditions
0	0	Power-on reset
u	u	LVR reset during Normal or SLOW Mode operation
1	u	WDT time-out reset during Normal or SLOW Mode operation
1	1	WDT time-out reset during IDLE or SLEEP Mode operation

Note: "u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

Item	Condition after Reset
Program Counter	Reset to zero
Interrupts	All interrupts will be disabled
WDT	Clear after reset, WDT begins counting
Timer Modules	Timer Modules will be turned off
Input/Output Ports	I/O ports will be setup as inputs, and AN0~AN7 as A/D input pin.
Stack Pointer	Stack Pointer will point to the top of the stack

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects each of the microcontroller internal registers.

Register Name	HT67F5650	HT67F5660	Power On Reset	WDT Time-out (Normal Operation)	WDT Time-out (HALT)
MP0	•	•	0000 0000	0000 0000	uuuu uuuu
MP1L	•	•	0000 0000	0000 0000	uuuu uuuu
MP1H	•	•	0000 0000	0000 0000	uuuu uuuu
MP2L	•	•	0000 0000	0000 0000	uuuu uuuu
MP2H	•	•	0000 0000	0000 0000	uuuu uuuu
IAR0	•	•	0000 0000	0000 0000	uuuu uuuu
IAR1	•	•	0000 0000	0000 0000	uuuu uuuu
IAR2	•	•	0000 0000	0000 0000	uuuu uuuu
ACC	•	•	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	•	•	0000 0000	0000 0000	0000 0000
TBLP	•	•	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLH	•	•	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBHP	•		---x xxxx	---u uuuu	---u uuuu
TBHP		•	--xx xxxx	--uu uuuu	--uu uuuu
STATUS	•	•	xx00 xxxx	uu1u uuuu	uu11 uuuu
SMOD	•	•	0000 0011	0000 0011	uuuu uuuu
PBP		•	---- ---0	---- ---0	---- ---u
INTEG	•	•	0000 0000	0000 0000	uuuu uuuu
LVDC	•	•	--00 -000	--00 -000	--uu -uuu
INTC0	•	•	-000 0000	-000 0000	-uuu uuuu
INTC1	•	•	0000 0000	0000 0000	uuuu uuuu
INTC2	•	•	0000 0000	0000 0000	uuuu uuuu
INTC3	•	•	--00 --00	--00 --00	--uu --uu
MFI0	•	•	--00 --00	--00 --00	--uu --uu
MFI1	•	•	0000 0000	0000 0000	uuuu uuuu
MFI2	•	•	0-00 0-00	0-00 0-00	u-uu u-uu
MFI3	•	•	0000 0000	0000 0000	uuuu uuuu
PA	•	•	1111 1111	1111 1111	uuuu uuuu
PAC	•	•	1111 1111	1111 1111	uuuu uuuu
PB	•	•	1111 1111	1111 1111	uuuu uuuu
PBC	•	•	1111 1111	1111 1111	uuuu uuuu
PC	•	•	1111 1111	1111 1111	uuuu uuuu
PCC	•	•	1111 1111	1111 1111	uuuu uuuu
PD	•	•	1111 1111	1111 1111	uuuu uuuu
PDC	•	•	1111 1111	1111 1111	uuuu uuuu
WDTC	•	•	0101 0011	0101 0011	uuuu uuuu
TBC	•	•	0011 0111	0011 0111	uuuu uuuu
PAWU	•	•	0000 0000	0000 0000	uuuu uuuu
PAPU	•	•	0000 0000	0000 0000	uuuu uuuu
PBPU	•	•	0000 0000	0000 0000	uuuu uuuu
PCPU	•	•	0000 0000	0000 0000	uuuu uuuu

Register Name	HT67F5650	HT67F5660	Power On Reset	WDT Time-out (Normal Operation)	WDT Time-out (HALT)
PDPU	•	•	0000 0000	0000 0000	uuuu uuuu
TM0C0	•	•	0000 0000	0000 0000	uuuu uuuu
TM0C1	•	•	0000 0000	0000 0000	uuuu uuuu
TM0DL	•	•	0000 0000	0000 0000	uuuu uuuu
TM0DH	•	•	---- --00	---- --00	---- --uu
TM0AL	•	•	0000 0000	0000 0000	uuuu uuuu
TM0AH	•	•	---- --00	---- --00	---- --uu
LCDC	•	•	0000 -000	0000 -000	uuuu -uuu
LCD1	•	•	0000 0000	0000 0000	uuuu uuuu
LCD2	•	•	0000 0000	0000 0000	uuuu uuuu
LCD3	•	•	---- --00	---- --00	---- --uu
LCD4		•	0000 0000	0000 0000	uuuu uuuu
CP1C	•	•	1000 0--1	1000 0--1	uuuu u--u
CP0C	•	•	1000 0--1	1000 0--1	uuuu u--u
PWRC	•	•	00-- -000	00-- -000	uu-- -uuu
PGAC0	•	•	-000 0000	-000 0000	-uuu uuuu
PGAC1	•	•	10--000-	10--000-	uu--uuu-
PGACS	•	•	--00 0000	--00 0000	--uu uuuu
USR	•	•	0000 1011	0000 1011	uuuu uuuu
UCR1	•	•	0000 00x0	0000 00x0	uuuu uuuu
UCR2	•	•	0000 0000	0000 0000	uuuu uuuu
BRG	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
TXR_RXR	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
IRCTRL0	•	•	0000 0000	0000 0000	uuuu uuuu
IRCTRL1	•	•	---- --0	---- --0	---- --u
ADCR0	•	•	0010 00-0	0010 00-0	uuuu uu-u
ADCR1	•	•	0000 000-	0000 000-	uuuu uu-u
ADRL	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
ADRH	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
ADCS	•	•	---0 0000	---0 0000	---u uuuu
ADRM	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
SPIC0	•	•	111- --0-	111- --0-	uuu- --u-
SPIC1	•	•	--00 0000	--00 0000	--uu uuuu
SPID	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
LVRC	•	•	0101 0101	0101 0101	uuuu uuuu
CTRL	•	•	0--- -x00	0--- -x00	u--- -uuu
PTM1C0	•	•	0000 0---	0000 0---	uuuu u---
PTM1C1	•	•	0000 0000	0000 0000	uuuu uuuu
PTM1DL	•	•	0000 0000	0000 0000	uuuu uuuu
PTM1DH	•	•	---- --00	---- --00	---- --uu
PTM1AL	•	•	0000 0000	0000 0000	uuuu uuuu
PTM1AH	•	•	---- --00	---- --00	---- --uu
PTM2C0	•	•	0000 0---	0000 0---	uuuu u---
PTM2C1	•	•	0000 0000	0000 0000	uuuu uuuu
PTM2DL	•	•	0000 0000	0000 0000	uuuu uuuu

Register Name	HT67F5650	HT67F5660	Power On Reset	WDT Time-out (Normal Operation)	WDT Time-out (HALT)
PTM2DH	•	•	---- --00	---- --00	---- --uu
PTM2AL	•	•	0000 0000	0000 0000	uuuu uuuu
PTM2AH	•	•	---- --00	---- --00	---- --uu
CTRL0	•	•	---- 0000	---- 0000	---- uuuu
PTM1RPL	•	•	0000 0000	0000 0000	uuuu uuuu
PTM1RPH	•	•	---- --00	---- --00	---- --uu
PTM2RPL	•	•	0000 0000	0000 0000	uuuu uuuu
PTM2RPH	•	•	---- --00	---- --00	---- --uu
SIMC0	•	•	1110 0000	1110 0000	uuuu uuuu
SIMC1	•	•	1000 0001	1000 0001	uuuu uuuu
SIMA/SIMC2	•	•	0000 0000	0000 0000	uuuu uuuu
SIMD	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
SIMTOC	•	•	0000 0000	0000 0000	uuuu uuuu
STM3C0	•	•	0000 0000	0000 0000	uuuu uuuu
STM3C1	•	•	0000 0000	0000 0000	uuuu uuuu
STM3DL	•	•	0000 0000	0000 0000	uuuu uuuu
STM3DH	•	•	0000 0000	0000 0000	uuuu uuuu
STM3AL	•	•	0000 0000	0000 0000	uuuu uuuu
STM3AH	•	•	0000 0000	0000 0000	uuuu uuuu
STM3RP	•	•	0000 0000	0000 0000	uuuu uuuu
FARL	•	•	0000 0000	0000 0000	uuuu uuuu
FARH	•		---0 0000	--00 0000	--uu uuuu
FARH		•	--00 0000	--00 0000	--uu uuuu
FD0L	•	•	0000 0000	0000 0000	uuuu uuuu
FD0H	•	•	0000 0000	0000 0000	uuuu uuuu
FD1L	•	•	0000 0000	0000 0000	uuuu uuuu
FD1H	•	•	0000 0000	0000 0000	uuuu uuuu
FD2L	•	•	0000 0000	0000 0000	uuuu uuuu
FD2H	•	•	0000 0000	0000 0000	uuuu uuuu
FD3L	•	•	0000 0000	0000 0000	uuuu uuuu
FD3H	•	•	0000 0000	0000 0000	uuuu uuuu
LCDCP	•	•	---- 0-00	---- 0-00	---- u-uu
EEA	•		-xxx xxxx	-xxx xxxx	-uuu uuuu
EEA		•	xxxx xxxx	xxxx xxxx	uuuu uuuu
EED	•	•	xxxx xxxx	xxxx xxxx	uuuu uuuu
EEC	•	•	---- 0000	---- 0000	---- uuuu
FC0	•	•	0000 0000	0000 0000	uuuu uuuu
FC1	•	•	0000 0000	0000 0000	uuuu uuuu
FC2	•	•	---- ---0	---- ---0	---- ---u

Note: "u" stands for unchanged  
"x" stands for unknown  
"-" stands for unimplemented

## Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. With the input or output designation of every pin fully under user program control, pull-high selections for all ports and wake-up selections on certain pins, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities.

These devices provide bidirectional input/output lines labeled with port names PA~PD. These I/O ports are mapped to the RAM Data Memory with specific addresses as shown in the Special Purpose Data Memory table. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A, [m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PAWU	D7	D6	D5	D4	D3	D2	D1	D0
PAPU	D7	D6	D5	D4	D3	D2	D1	D0
PA	D7	D6	D5	D4	D3	D2	D1	D0
PAC	D7	D6	D5	D4	D3	D2	D1	D0
PBPU	D7	D6	D5	D4	D3	D2	D1	D0
PB	D7	D6	D5	D4	D3	D2	D1	D0
PBC	D7	D6	D5	D4	D3	D2	D1	D0
PCPU	D7	D6	D5	D4	D3	D2	D1	D0
PC	D7	D6	D5	D4	D3	D2	D1	D0
PCC	D7	D6	D5	D4	D3	D2	D1	D0
PDPU	D7	D6	D5	D4	D3	D2	D1	D0
PD	D7	D6	D5	D4	D3	D2	D1	D0
PDC	D7	D6	D5	D4	D3	D2	D1	D0

I/O Register List

### Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, all I/O pins, when configured as an input have the capability of being connected to an internal pull-high resistor. These pull-high resistors are selected using registers PAPU~PDPU, and are implemented using weak PMOS transistors.

#### PAPU Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 Port A bit 7 ~ bit 0 Pull-high Control  
0: Disable  
1: Enable

**PBPU Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 Port B bit 7 ~ bit 0 Pull-high Control  
 0: Disable  
 1: Enable

**PCPU Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 Port C bit 7 ~ bit 0 Pull-high Control  
 0: Disable  
 1: Enable

**PDPU Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 Port D bit 7 ~ bit 0 Pull-high Control  
 0: Disable  
 1: Enable

**Port A Wake-up**

The HALT instruction forces the microcontroller into the SLEEP or IDLE Mode which preserves power, a feature that is important for battery and other low-power applications. Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the Port A pins from high to low. This function is especially suitable for applications that can be woken up via external switches. Each pin on Port A can be selected individually to have this wake-up feature using the PAWU register.

**PAWU Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 Port A bit 7~bit 0 Wake-up Control  
 0: Disable  
 1: Enable

## I/O Port Control Registers

Each I/O port has its own control register known as PAC~PDC, to control the input/output configuration. With this control register, each CMOS output or input can be reconfigured dynamically under software control. Each pin of the I/O ports is directly mapped to a bit in its associated port control register. For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as a CMOS output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin.

### PAC Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 Port A bit 7 ~ bit 0 Input/Output Control  
0: Output  
1: Input

### PBC Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 Port B bit 7 ~ bit 0 Input/Output Control  
0: Output  
1: Input

### PCC Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 Port C bit 7 ~ bit 0 Input/Output Control  
0: Output  
1: Input

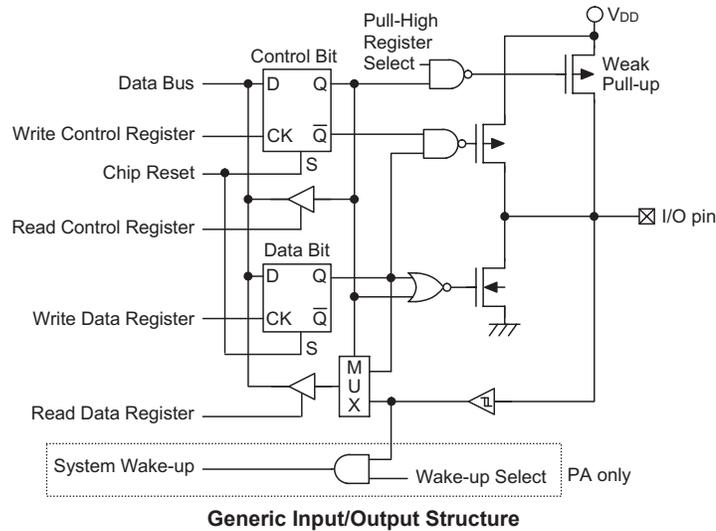
### PDC Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 Port D bit 7 ~ bit 0 Input/Output Control  
0: Output  
1: Input

## I/O Pin Structures

The accompanying diagrams illustrate the internal structures of some generic I/O pin types. As the exact logical construction of the I/O pin will differ from these drawings, they are supplied as a guide only to assist with the functional understanding of the I/O pins. The wide range of pin-shared structures does not permit all types to be shown.



## Programming Considerations

Within the user program, one of the first things to consider is port initialisation. After a reset, all of the I/O data and port control registers will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high selections have been chosen. If the port control registers, PAC~PDC, are then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated port data registers, PA~PD, are first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct values into the appropriate port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire port, modify it to the required new bit values and then rewrite this data back to the output ports.

Port A has the additional capability of providing wake-up functions. When these devices are in the SLEEP or IDLE Mode, various methods are available to wake the devices up. One of these is a high to low transition of any of the Port A pins. Single or multiple pins on Port A can be setup to have this function.

## Timer Modules – TM

One of the most fundamental functions in any microcontroller devices is the ability to control and measure time. To implement time related functions each device includes several Timer Modules, abbreviated to the name TM. The TMs are multi-purpose timing units and serve to provide operations such as Timer/Counter, Input Capture, Compare Match Output and Single Pulse Output as well as being the functional unit for the generation of PWM signals. Each of the TMs has two individual interrupts. The addition of input and output pins for each TM ensures that users are provided with timing units with a wide and flexible range of features.

The common features of the different TM types are described here with more detailed information provided in the individual Compact, Periodic and Standard TM sections.

### Introduction

Each device contains four TMs having a reference name of TM0, TM1, TM2 and TM3. Each individual TM can be categorised as a certain type, namely Compact Type TM, Periodic Type TM or Standard Type TM. Although similar in nature, the different TM types vary in their feature complexity. The common features to all of the Compact, Periodic and Standard TMs will be described in this section; the detailed operation regarding each of the TM types will be described in separate sections. The main features and differences between the three types of TMs are summarised in the accompanying table.

Function	CTM	PTM	STM
Timer/Counter	√	√	√
I/P Capture	—	√	√
Compare Match Output	√	√	√
PWM Channels	1	1	1
Single Pulse Output	—	1	1
PWM Alignment	Edge	Edge	Edge
PWM Adjustment Period & Duty	Duty or Period	Duty or Period	Duty or Period

**TM Function Summary**

Device	TM0	TM1	TM2	TM3
HT67F5650	10-bit CTM	10-bit PTM	10-bit PTM	16-bit STM
HT67F5660				

**TM Name/Type Reference**

### TM Operation

The three different types of TM offer a diverse range of functions, from simple timing operations to PWM signal generation. The key to understanding how the TM operates is to see it in terms of a free running counter whose value is then compared with the value of pre-programmed internal comparators. When the free running counter has the same value as the pre-programmed comparator, known as a compare match situation, a TM interrupt signal will be generated which can clear the counter and perhaps also change the condition of the TM output pin. The internal TM counter is driven by a user selectable clock source, which can be an internal clock or an external pin.

### TM Clock Source

The clock source which drives the main counter in each TM can originate from various sources. The selection of the required clock source is implemented using the TnCK2~TnCK0 bits in the TM control registers. The clock source can be a ratio of the system clock  $f_{SYS}$  or the internal high clock  $f_H$ , the  $f_{SUB}$  clock source or the external TCKn pin. The TCKn pin clock source is used to allow an external signal to drive the TM as an external clock source or for event counting.

### TM Interrupts

The Compact Type, Periodic Type and Standard Type TMs each have two internal interrupts, one for each of the internal comparator A or comparator P, which generate a TM interrupt when a compare match condition occurs. When a TM interrupt is generated it can be used to clear the counter and also to change the state of the TM output pin.

### TM External Pins

Each of the TMs, irrespective of what type, has one TM input pin, with the label TCKn. The TM input pin is essentially a clock source for the TM and is selected using the TnCK2~TnCK0 bits in the TMnC0/PTMnC0/STMnC0 register. This external TM input pin allows an external clock source to drive the internal TM. This external TM input pin is shared with other functions but will be connected to the internal TM if selected using the TnCK2~TnCK0 bits. The TM input pin can be chosen to have either a rising or falling active edge.

The TMs each have two output pins with the label TPn\_0 and TPn\_1. When the TM is in the Compare Match Output Mode, these pins can be controlled by the TM to switch to a high or low level or to toggle when a compare match situation occurs. The external TPn\_0 and TPn\_1 output pins are also the pin where the TM generates the PWM output waveform. As the TM output pins are pin-shared with other function, the TM output function must first be setup using the CTRL0 register. A single bit in one of the registers determines if its associated pin is to be used as an external TM output pin or if it is to have another function. The details of the TM output pins for each TM type are provided in the accompanying table.

All TM output pin names have a "\_n" suffix. Pin names that include a "\_0" or "\_1" suffix indicate that they are from a TM with multiple output pins.

Device	TM0	TM1	TM2	TM3	Register
HT67F5650	TP0_0, TP0_1	TP1_0, TP1_1	TP2_0, TP2_1	TP3_0, TP3_1	CTRL0
HT67F5660					

**TM Output Pins**

### TM Input/Output Pin Control Registers

Selecting to have a TM input/output or whether to retain its other shared functions is implemented using one register with a single bit in each register corresponding to a TM input/output pin. When the TM<sub>n</sub> is enabled, if the corresponding pin is setup as a TM input/output, and the complimentary output will be as a normal I/O pin.

#### CTRL0 Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	TP3CPS	TP2CPS	TP1CPS	TP0CPS
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3 **TP3CPS**: TP3\_0, TP3\_1 pin selection

0: TP3\_0

1: TP3\_1

When TM3 is enabled, the output function of TP3\_0 is timer, then the TP3\_1 is I/O, and vice versa.

Bit 2 **TP2CPS**: TP2\_0, TP2\_1 pin selection

0: TP2\_0

1: TP2\_1

When TM2 is enabled, the output function of TP2\_0 is timer, then the TP2\_1 is I/O, and vice versa.

Bit 1 **TP1CPS**: TP1\_0, TP1\_1 pin selection

0: TP1\_0

1: TP1\_1

When TM1 is enabled, the output function of TP1\_0 is timer, then the TP1\_1 is I/O, and vice versa.

Bit 0 **TP0CPS**: TP0\_0, TP0\_1 pin selection

0: TP0\_0

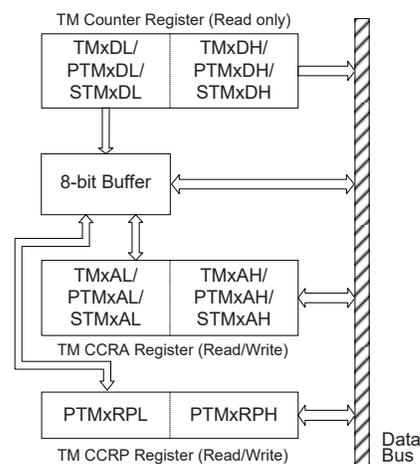
1: TP0\_1

When TM0 is enabled, the output function of TP0\_0 is timer, then the TP0\_1 is I/O, and vice versa.

## Programming Considerations

The TM Counter Registers and the Capture/Compare CCRA registers, being either 10-bit or 16-bit, and CCRP register pair for Periodic Timer Module, being 10-bit, all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to note is that data transfer to and from the 8-bit buffer and its related low byte only takes place when a write or read operation to its corresponding high byte is executed.

As the CCRA and PTM CCRP registers are implemented in the way shown in the following diagram and accessing the register is carried out in a specific way described above, it is recommended to use the "MOV" instruction to access the CCRA and PTM CCRP low byte registers, named TMxAL/PTMxAL/STMxAL and PTMxRPL, using the following access procedures. Accessing the CCRA or PTM CCRP low byte register without following these access procedures will result in unpredictable values.



The following steps show the read and write procedures:

- Writing Data to CCRA or PTM CCRP
  - ♦ Step 1. Write data to Low Byte TMxAL/PTMxAL/STMxAL or PTMxRPL
    - Note that here data is only written to the 8-bit buffer.
  - ♦ Step 2. Write data to High Byte TMxAH/PTMxAH/STMxAH or PTMxRPH
    - Here data is written directly to the high byte registers and simultaneously data is latched from the 8-bit buffer to the Low Byte registers.
- Reading Data from the Counter Registers and CCRA or PTM CCRP
  - ♦ Step 1. Read data from the High Byte TMxDH/PTMxDH/STMxDH, TMxAH/PTMxAH/STMxAH or PTMxRPH
    - Here data is read directly from the High Byte registers and simultaneously data is latched from the Low Byte register into the 8-bit buffer.
  - ♦ Step 2. Read data from the Low Byte TMxDL/PTMxDL/STMxDL, TMxAL/PTMxAL/STMxAL or PTMxRPL
    - This step reads data from the 8-bit buffer.

## Compact Type TM – CTM (TM0)

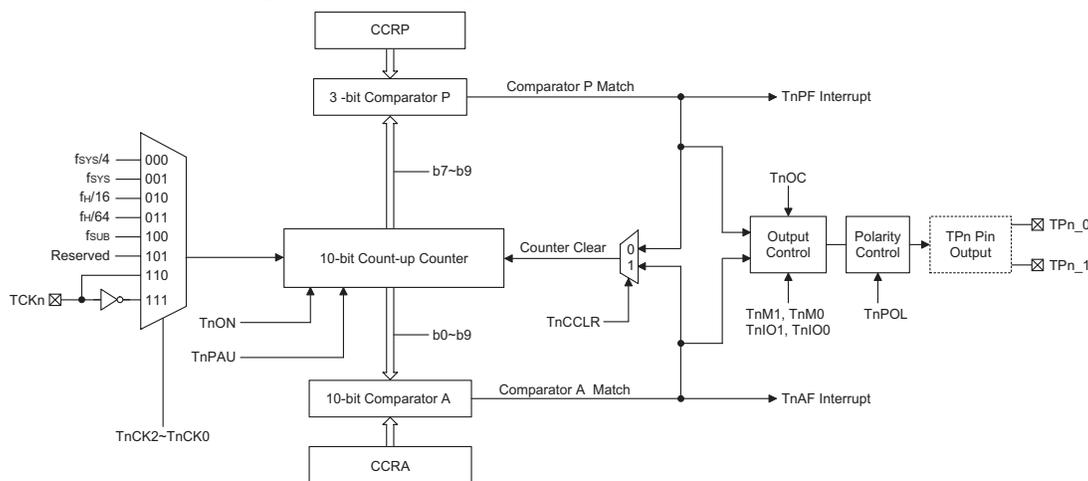
Although the simplest form of the two TM types, the Compact TM type still contains three operating modes, which are Compare Match Output, Timer/Event Counter and PWM Output modes. The Compact TM can be controlled with an external input pin and can drive two external output pins.

Device	Name	TM No.	TM Input Pin	TM Output Pin
HT67F5650	10-bit CTM	0	TCK0	TP0_0, TP0_1
HT67F5660				

### Compact TM Operation

At its core is a 10-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP is three bits wide whose value is compared with the highest three bits in the counter while the CCRA is the ten bits and therefore compares with all counter bits.

The only way of changing the value of the 10-bit counter using the application program, is to clear the counter by changing the TnON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a TM interrupt signal will also usually be generated. The Compact Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control the output pin. All operating setup conditions are selected using relevant internal registers.



**Compact Type TM Block Diagram (n=0)**

## Compact Type TM Register Description

Overall operation of the Compact TM is controlled using a series of registers. A read only register pair exists to store the internal counter 10-bit value, while a read/write register pair exists to store the internal 10-bit CCRA value. The remaining two registers are control registers which setup the different operating and control modes as well as the three CCRP bits.

Register Name	Bit							
	7	6	5	4	3	2	1	0
TMnC0	TnPAU	TnCK2	TnCK1	TnCK0	TnON	TnRP2	TnRP1	TnRP0
TMnC1	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
TMnDL	D7	D6	D5	D4	D3	D2	D1	D0
TMnDH	—	—	—	—	—	—	D9	D8
TMnAL	D7	D6	D5	D4	D3	D2	D1	D0
TMnAH	—	—	—	—	—	—	D9	D8

Compact TM Register List (n=0)

### TMnC0 Register (n=0)

Bit	7	6	5	4	3	2	1	0
Name	TnPAU	TnCK2	TnCK1	TnCK0	TnON	TnRP2	TnRP1	TnRP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **TnPAU**: TMn Counter Pause Control

0: Run  
1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4 **TnCK2~TnCK0**: Select TMn Counter clock

000:  $f_{SYS}/4$   
001:  $f_{SYS}$   
010:  $f_H/16$   
011:  $f_H/64$   
100:  $f_{SUB}$   
101: Reserved  
110: TCKn rising edge clock  
111: TCKn falling edge clock

These three bits are used to select the clock source for the TM. Selecting the Reserved clock input will effectively disable the internal counter. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source  $f_{SYS}$  is the system clock, while  $f_H$  and  $f_{SUB}$  are other internal clocks, the details of which can be found in the oscillator section.

- Bit 3     **TnON**: TMn Counter On/Off Control  
           0: Off  
           1: On
- This bit controls the overall on/off function of the TM. Setting the bit high enables the counter to run, clearing the bit disables the TM. Clearing this bit to zero will stop the counter from counting and turn off the TM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value. If the TM is in the Compare Match Output Mode then the TM output pin will be reset to its initial condition, as specified by the TnOC bit, when the TnON bit changes from low to high.
- Bit 2~0   **TnRP2~TnRP0**: TMn CCRP 3-bit register, compared with the TMn Counter bit 9~bit 7 Comparator P Match Period  
           000: 1024 TMn clocks  
           001: 128 TMn clocks  
           010: 256 TMn clocks  
           011: 384 TMn clocks  
           100: 512 TMn clocks  
           101: 640 TMn clocks  
           110: 768 TMn clocks  
           111: 896 TMn clocks
- These three bits are used to setup the value on the internal CCRP 3-bit register, which are then compared with the internal counter's highest three bits. The result of this comparison can be selected to clear the internal counter if the TnCCLR bit is set to zero. Setting the TnCCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest three counter bits, the compare values exist in 128 clock cycle multiples. Clearing all three bits to zero is in effect allowing the counter to overflow at its maximum value.

**TMnC1 Register (n=0)**

Bit	7	6	5	4	3	2	1	0
Name	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7~6   **TnM1~TnM0**: Select TMn Operating Mode  
           00: Compare Match Output Mode  
           01: Undefined  
           10: PWM Mode  
           11: Timer/Counter Mode
- These bits setup the required operating mode for the TM. To ensure reliable operation the TM should be switched off before any changes are made to the TnM1 and TnM0 bits. In the Timer/Counter Mode, the TM output pin control must be disabled.
- Bit 5~4   **TnIO1~TnIO0**: Select TPn\_0, TPn\_1 output function  
           Compare Match Output Mode  
           00: No change  
           01: Output low  
           10: Output high  
           11: Toggle output  
           PWM Mode  
           00: PWM Output inactive state  
           01: PWM Output active state  
           10: PWM output  
           11: Undefined

Timer/Counter Mode

Unused

These two bits are used to determine how the TM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the TM is running.

In the Compare Match Output Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the TM output pin should be setup using the TnOC bit in the TMnC1 register. Note that the output level requested by the TnIO1 and TnIO0 bits must be different from the initial value setup using the TnOC bit otherwise no change will occur on the TM output pin when a compare match occurs. After the TM output pin changes state, it can be reset to its initial level by changing the level of the TnON bit from low to high.

In the PWM Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the TnIO1 and TnIO0 bits only after the TMn has been switched off. Unpredictable PWM outputs will occur if the TnIO1 and TnIO0 bits are changed when the TM is running.

Bit 3 **TnOC**: TPn\_0, TPn\_1 Output control bit

Compare Match Output Mode

0: Initial low

1: Initial high

PWM Mode

0: Active low

1: Active high

This is the output control bit for the TM output pin. Its operation depends upon whether TM is being used in the Compare Match Output Mode or in the PWM Mode. It has no effect if the TM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the TM output pin before a compare match occurs. In the PWM Mode it determines if the PWM signal is active high or active low.

Bit 2 **TnPOL**: TPn\_0, TPn\_1 Output polarity Control

0: Non-invert

1: Invert

This bit controls the polarity of the TPn\_0 or TPn\_1 output pin. When the bit is set high the TM output pin will be inverted and not inverted when the bit is zero. It has no effect if the TM is in the Timer/Counter Mode.

Bit 1 **TnDPX**: TMn PWM period/duty Control

0: CCRP - period; CCRA - duty

1: CCRP - duty; CCRA - period

This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0 **TnCCLR**: Select TMn Counter clear condition

0: TMn Comparator P match

1: TMn Comparator A match

This bit is used to select the method which clears the counter. Remember that the Compact TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the TnCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The TnCCLR bit is not used in the PWM Mode.

**TMnDL Register (n=0)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0     **D7~D0**: TMn Counter Low Byte Register bit 7 ~ bit 0  
 TMn 10-bit Counter bit 7 ~ bit 0

**TMnDH Register (n=0)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R	R
POR	—	—	—	—	—	—	0	0

Bit 7~2     Unimplemented, read as "0"  
 Bit 1~0     **D9~D8**: TMn Counter High Byte Register bit 1 ~ bit 0  
 TMn 10-bit Counter bit 9 ~ bit 8

**TMnAL Register (n=0)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0     **D7~D0**: TMn CCRA Low Byte Register bit 7 ~ bit 0  
 TMn 10-bit CCRA bit 7 ~ bit 0

**TMnAH Register (n=0)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2     Unimplemented, read as "0"  
 Bit 1~0     **D9~D8**: TMn CCRA High Byte Register bit 1 ~ bit 0  
 TMn 10-bit CCRA bit 9 ~ bit 8

## **Compact Type TM Operating Modes**

The Compact Type TM can operate in one of three operating modes, Compare Match Output Mode, PWM Mode or Timer/Counter Mode. The operating mode is selected using the TnM1 and TnM0 bits in the TMnC1 register.

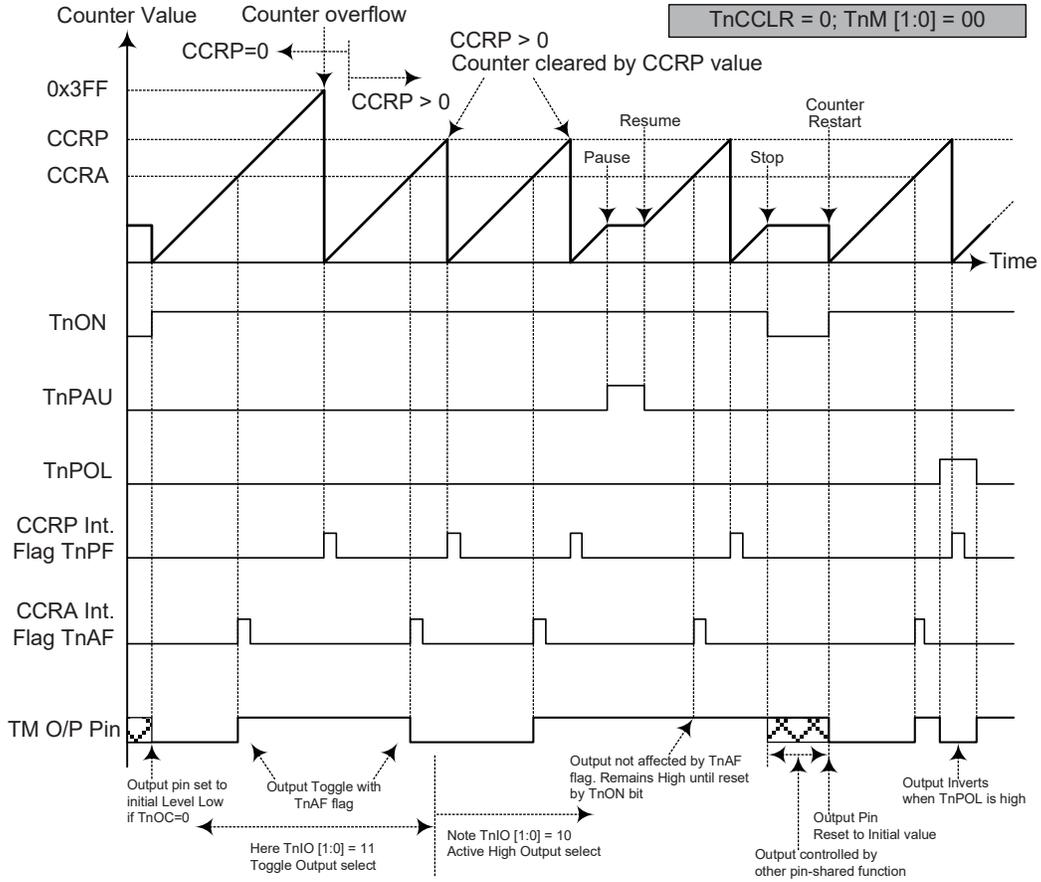
### **Compare Match Output Mode**

To select this mode, bits TnM1 and TnM0 in the TMnC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the TnCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match occurs from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both TnAF and TnPF interrupt request flags for the Comparator A and Comparator P respectively, will both be generated.

If the TnCCLR bit in the TMnC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the TnAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when TnCCLR is high no TnPF interrupt request flag will be generated.

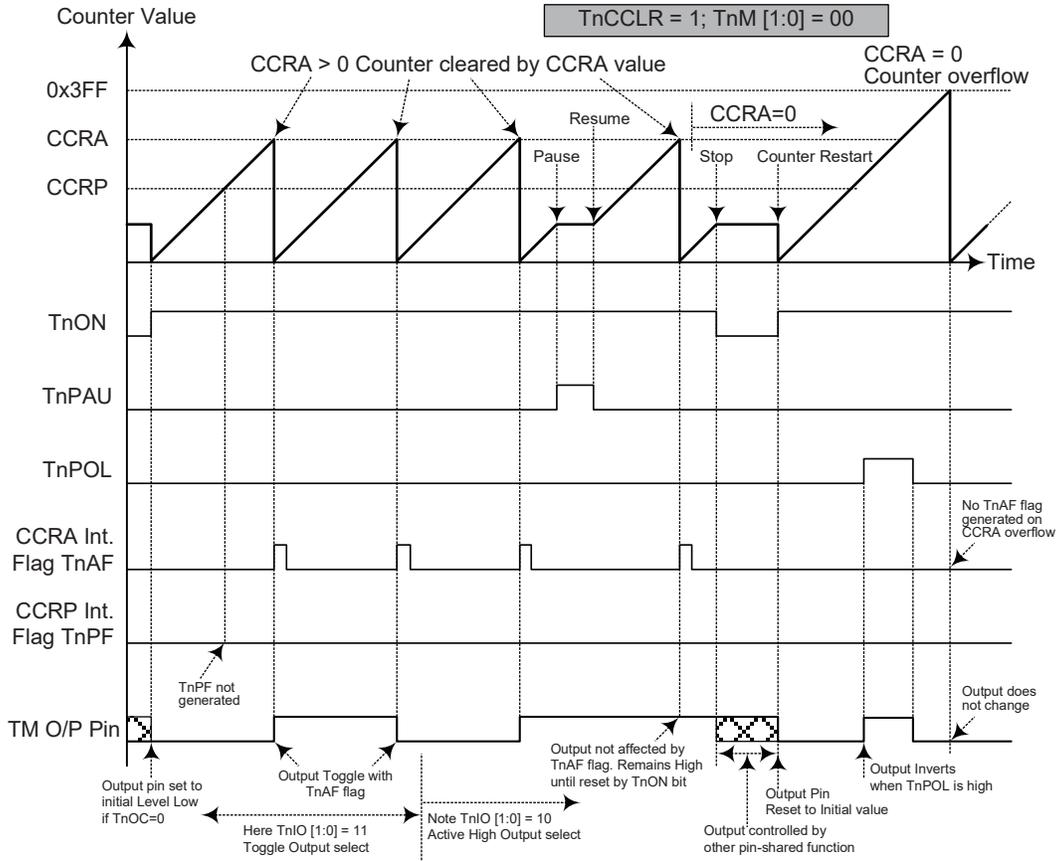
If the CCRA bits are all zero, the counter will overflow when it reaches its maximum 10-bit, 3FF Hex, value, however here the TnAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the TM output pin will change state. The TM output pin condition however only changes state when a TnAF interrupt request flag is generated after a compare match occurs from Comparator A. The TnPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the TM output pin. The way in which the TM output pin changes state are determined by the condition of the TnIO1 and TnIO0 bits in the TMnC1 register. The TM output pin can be selected using the TnIO1 and TnIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the TM output pin, which is setup after the TnON bit changes from low to high, is setup using the TnOC bit. Note that if the TnIO1 and TnIO0 bits are zero then no pin change will take place.



**Compare Match Output Mode – TnCCLR = 0 (n=0)**

- Note: 1. With  $TnCCLR=0$ , a Comparator P match will clear the counter  
 2. The TM output pin is controlled only by the TnAF flag  
 3. The output pin is reset to its initial state by a TnON bit rising edge



**Compare Match Output Mode – TnCCLR = 1 (n=0)**

- Note: 1. With  $TnCCLR=1$ , a Comparator A match will clear the counter  
 2. The TM output pin is controlled only by the TnAF flag  
 3. The output pin is reset to its initial state by a TnON bit rising edge  
 4. The TnPF flag is not generated when  $TnCCLR=1$

### Timer/Counter Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the TM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

### PWM Output Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register should be set to 10 respectively. The PWM function within the TM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the TM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM mode, the TnCCLR bit has no effect on the PWM operation. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. Which register is used to control either frequency or duty cycle is determined using the TnDPX bit in the TMnC1 register. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The TnOC bit in the TMnC1 register is used to select the required polarity of the PWM waveform while the two TnIO1 and TnIO0 bits are used to enable the PWM output or to force the TM output pin to a fixed high or low level. The TnPOL bit is used to reverse the polarity of the PWM output waveform.

• **CTM, PWM Mode, Edge-aligned Mode, TnDPX=0**

CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	128	256	384	512	640	768	896	1024
Duty	CCRA							

If  $f_{SYS} = 16\text{MHz}$ , TM clock source is  $f_{SYS}/4$ , CCRP = 100b and CCRA = 128,

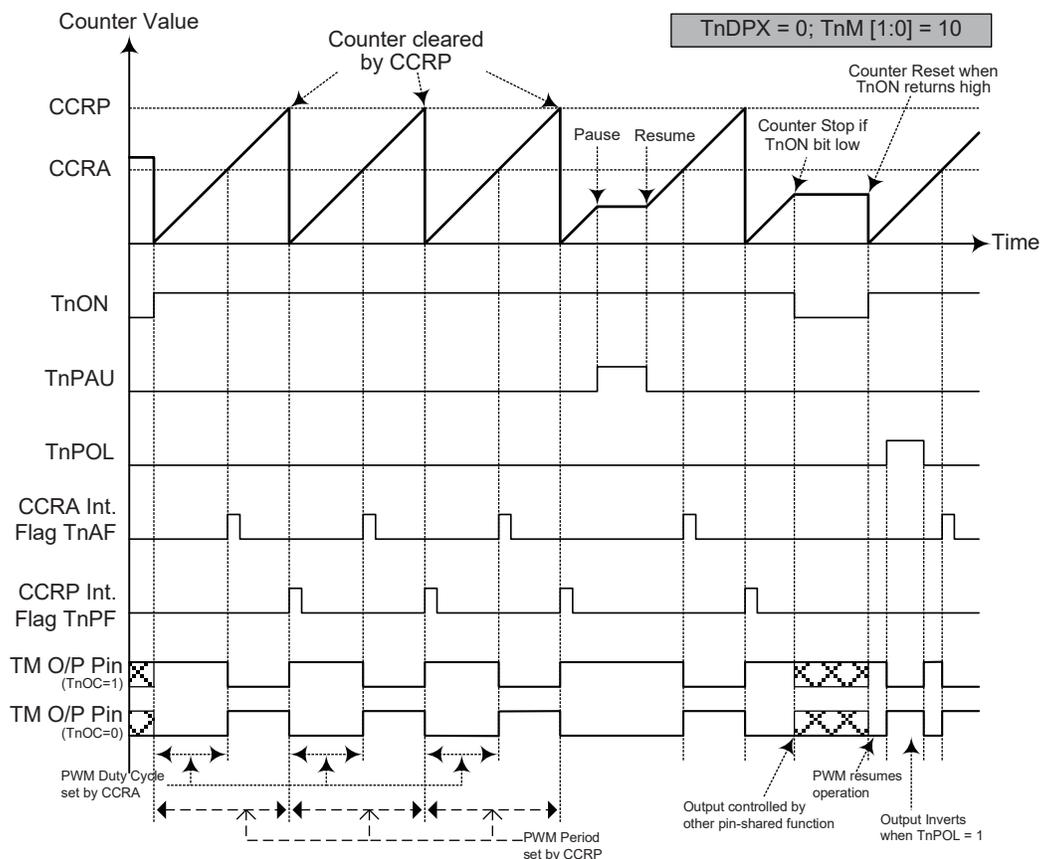
The CTM PWM output frequency =  $(f_{SYS}/4)/512 = f_{SYS}/2048 = 7.8125\text{ kHz}$ , duty =  $128/512 = 25\%$ .

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

• **CTM, PWM Mode, Edge-aligned Mode, TnDPX=1**

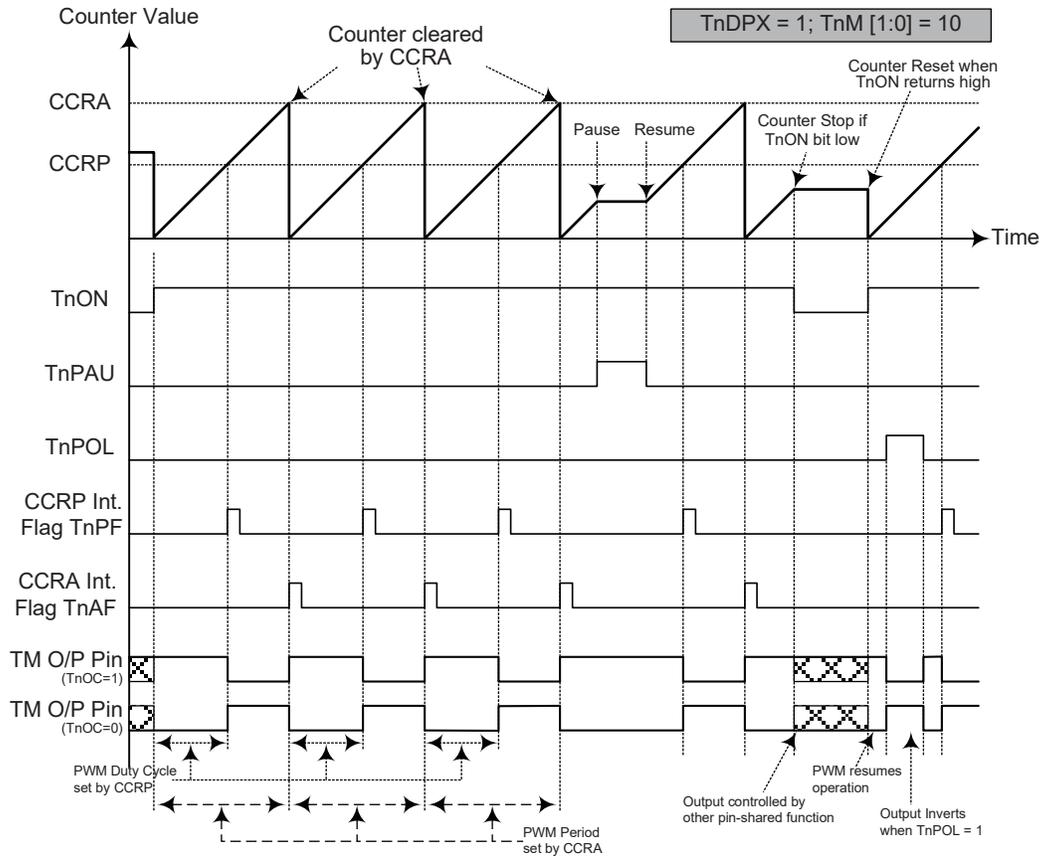
CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	CCRA							
Duty	128	256	384	512	640	768	896	1024

The PWM output period is determined by the CCRA register value together with the TM clock while the PWM duty cycle is defined by the CCRP register value.



**PWM Mode – TnDPX = 0 (n=0)**

- Note: 1. Here TnDPX=0 – Counter cleared by CCRP  
 2. A counter clear sets the PWM Period  
 3. The internal PWM function continues even when TnIO [1:0] = 00 or 01  
 4. The TnCCLR bit has no influence on PWM operation



**PWM Mode – TnDPX = 1 (n=0)**

- Note: 1. Here TnDPX = 1 – Counter cleared by CCRA
2. A counter clear sets the PWM Period
3. The internal PWM function continues even when TnIO [1:0] = 00 or 01
4. The TnCCLR bit has no influence on PWM operation

## Periodic Type TM – PTM (TM1, TM2)

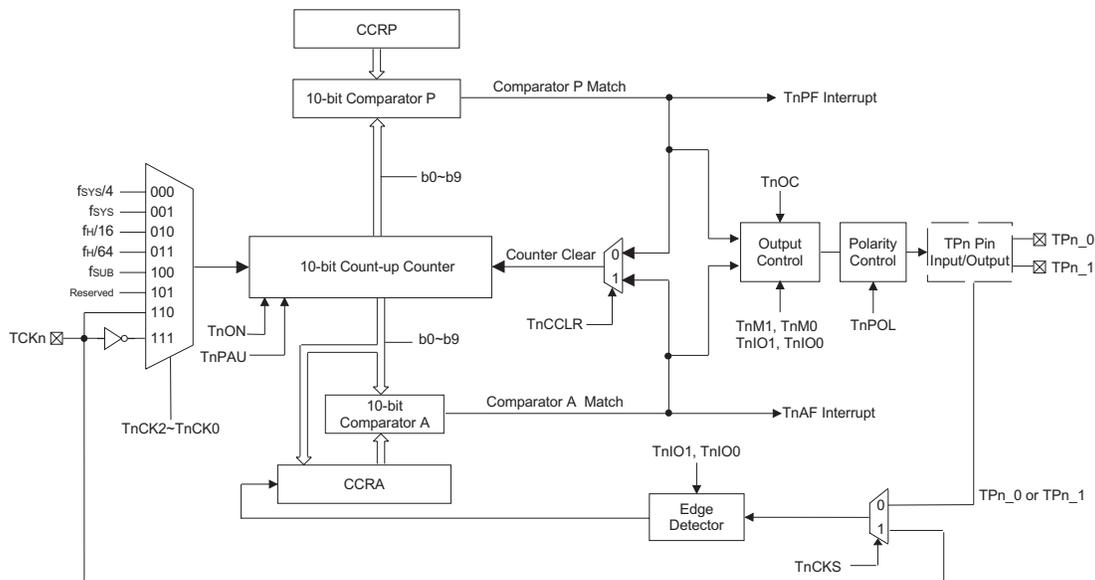
The Periodic Type TM contains five operating modes, which are Compare Match Output, Timer/Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Periodic TM can be controlled with an external input pin and can drive two external output pins.

Device	Name	TM No.	TM Input Pin	TM Output Pin
HT67F5650	10-bit PTM	1, 2	TCK1; TCK2	TP1_0, TP1_1;
HT67F5660				TP2_0, TP2_1

### Periodic TM Operation

At its core is a 10-bit count-up counter which is driven by a user selectable internal or external clock source. There are two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with the CCRA and CCRP registers.

The only way of changing the value of the 10-bit counter using the application program, is to clear the counter by changing the TnON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a TM interrupt signal will also usually be generated. The Periodic Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control the output pin. All operating setup conditions are selected using relevant internal registers.



**Periodic Type TM Block Diagram (n=1 or 2)**

### Periodic Type TM Register Description

Overall operation of the Periodic TM is controlled using a series of registers. A read only register pair exists to store the internal counter 10-bit value, while two read/write register pairs exist to store the internal 10-bit CCRA and CCRP value. The remaining two registers are control registers which setup the different operating and control modes.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PTMnC0	TnPAU	TnCK2	TnCK1	TnCK0	TnON	—	—	—
PTMnC1	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnCKS	TnCCLR
PTMnDL	D7	D6	D5	D4	D3	D2	D1	D0
PTMnDH	—	—	—	—	—	—	D9	D8
PTMnAL	D7	D6	D5	D4	D3	D2	D1	D0
PTMnAH	—	—	—	—	—	—	D9	D8
PTMnRPL	D7	D6	D5	D4	D3	D2	D1	D0
PTMnRPH	—	—	—	—	—	—	D9	D8

**10-bit Periodic TM Register List (n=1 or 2)**

#### PTMnC0 Register (n=1 or 2)

Bit	7	6	5	4	3	2	1	0
Name	TnPAU	TnCK2	TnCK1	TnCK0	TnON	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	—	—	—
POR	0	0	0	0	0	—	—	—

**Bit 7 TnPAU:** TMn Counter Pause Control  
0: Run  
1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

**Bit 6~4 TnCK2~TnCK0:** Select TMn Counter clock  
000:  $f_{SYS}/4$   
001:  $f_{SYS}$   
010:  $f_H/16$   
011:  $f_H/64$   
100:  $f_{SUB}$   
101: Reserved  
110: TCKn rising edge clock  
111: TCKn falling edge clock

These three bits are used to select the clock source for the TM. Selecting the Reserved clock input will effectively disable the internal counter. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source  $f_{SYS}$  is the system clock, while  $f_H$  and  $f_{SUB}$  are other internal clocks, the details of which can be found in the oscillator section.

Bit 3 **TnON**: TMn Counter On/Off Control  
 0: Off  
 1: On

This bit controls the overall on/off function of the TM. Setting the bit high enables the counter to run, clearing the bit disables the TM. Clearing this bit to zero will stop the counter from counting and turn off the TM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again.

If the TM is in the Compare Match Output Mode then the TM output pin will be reset to its initial condition, as specified by the TM Output control bit, when the bit changes from low to high.

Bit 2~0 Unimplemented, read as "0"

**PTMnC1 Register (n=1 or 2)**

Bit	7	6	5	4	3	2	1	0
Name	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnCKS	TnCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **TnM1~TnM0**: Select TMn Operation Mode  
 00: Compare Match Output Mode  
 01: Capture Input Mode  
 10: PWM Mode or Single Pulse Output Mode  
 11: Timer/Counter Mode

These bits setup the required operating mode for the TM. To ensure reliable operation the TM should be switched off before any changes are made to the TnM1 and TnM0 bits. In the Timer/Counter Mode, the TM output pin control must be disabled.

Bit 5~4 **TnIO1~TnIO0**: Select TPn\_0, TPn\_1 output function

Compare Match Output Mode

- 00: No change
- 01: Output low
- 10: Output high
- 11: Toggle output

PWM Mode/Single Pulse Output Mode

- 00: PWM Output inactive state
- 01: PWM Output active state
- 10: PWM output
- 11: Single pulse output

Capture Input Mode

- 00: Input capture at rising edge of TPn\_0, TPn\_1, TCKn
- 01: Input capture at falling edge of TPn\_0, TPn\_1, TCKn
- 10: Input capture at falling/rising edge of TPn\_0, TPn\_1, TCKn
- 11: Input capture disabled

Timer/counter Mode

Unused

These two bits are used to determine how the TM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the TM is running.

In the Compare Match Output Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When these bits are both zero, then no change will take place on the output. The initial value of the TM output pin should be setup using the TnOC bit. Note that the output level requested by the TnIO1

and TnIO0 bits must be different from the initial value setup using the TnOC bit otherwise no change will occur on the TM output pin when a compare match occurs. After the TM output pin changes state, it can be reset to its initial level by changing the level of the TnON bit from low to high.

In the PWM Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to change the values of the TnIO1 and TnIO0 bits only after the TM has been switched off. Unpredictable PWM outputs will occur if the TnIO1 and TnIO0 bits are changed when the TM is running.

Bit 3 **TnOC**: TPn\_0, TPn\_1 Output control bit

Compare Match Output Mode

0: Initial low

1: Initial high

PWM Mode/ Single Pulse Output Mode

0: Active low

1: Active high

This is the output control bit for the TM output pin. Its operation depends upon whether TM is being used in the Compare Match Output Mode or in the PWM Mode/ Single Pulse Output Mode. It has no effect if the TM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the TM output pin before a compare match occurs. In the PWM Mode it determines if the PWM signal is active high or active low.

Bit 2 **TnPOL**: TPn\_0, TPn\_1 Output polarity Control

0: Non-invert

1: Invert

This bit controls the polarity of the TPn\_0, TPn\_1 output pin. When the bit is set high the TM output pin will be inverted and not inverted when the bit is zero. It has no effect if the TM is in the Timer/Counter Mode.

Bit 1 **TnCKS**: TMn capture trigger source select

0: From TPn\_0, TPn\_1 pin

1: From TCKn pin

Bit 0 **TnCCLR**: Select TMn Counter clear condition

0: TMn Comparator P match

1: TMn Comparator A match

This bit is used to select the method which clears the counter. Remember that the Periodic TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the TnCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The TnCCLR bit is not used in the PWM, Single Pulse or Input Capture Mode.

#### PTMnDL Register (n=1 or 2)

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PTMnDL**: TMn Counter Low Byte Register bit 7 ~ bit 0

TMn 10-bit Counter bit 7 ~ bit 0

**PTMnDH Register (n=1 or 2)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R	R
POR	—	—	—	—	—	—	0	0

Bit 7~2 Unimplemented, read as "0"

Bit 1~0 **PTMnDH**: TMn Counter High Byte Register bit 1 ~ bit 0  
TMn 10-bit Counter bit 9 ~ bit 8

**PTMnAL Register (n=1 or 2)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PTMnAL**: TMn CCRA Low Byte Register bit 7 ~ bit 0  
TMn 10-bit CCRA bit 7 ~ bit 0

**PTMnAH Register (n=1 or 2)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2 Unimplemented, read as "0"

Bit 1~0 **PTMnAH**: TMn CCRA High Byte Register bit 1 ~ bit 0  
TMn 10-bit CCRA bit 9 ~ bit 8

**PTMnRPL Register (n=1 or 2)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PTMnRPL**: TMn CCRP Low Byte Register bit 7 ~ bit 0  
TMn 10-bit CCRP bit 7 ~ bit 0

**PTMnRPH Register (n=1 or 2)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2 Unimplemented, read as "0"

Bit 1~0 **PTMnRPH**: TMn CCRP High Byte Register bit 1 ~ bit 0  
TMn 10-bit CCRP bit 9 ~ bit 8

## Periodic Type TM Operating Modes

The Periodic Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the TnM1 and TnM0 bits in the PTMnC1 register.

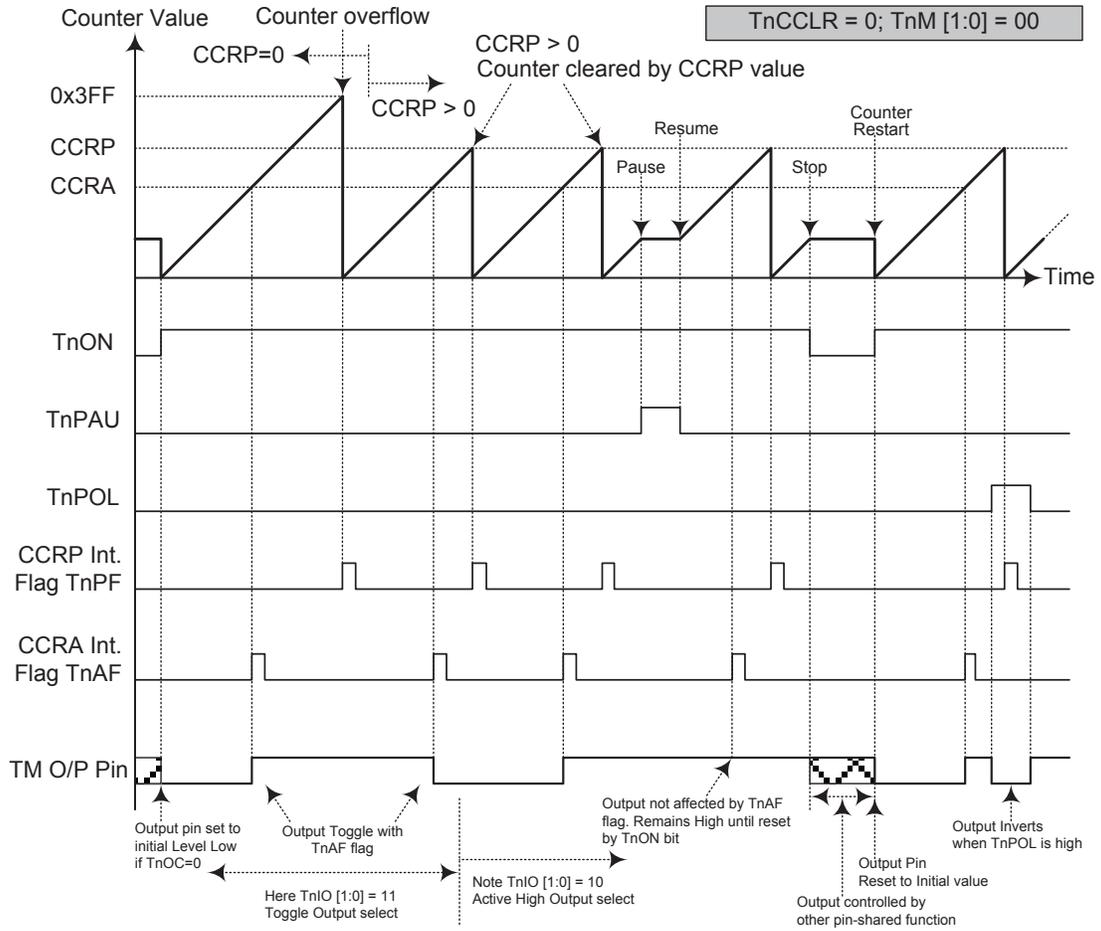
### Compare Match Output Mode

To select this mode, bits TnM1 and TnM0 in the PTMnC1 register, should be all cleared to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the TnCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match occurs from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both the TnAF and TnPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the TnCCLR bit in the PTMnC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the TnAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when TnCCLR is high no TnPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA cannot be cleared to zero.

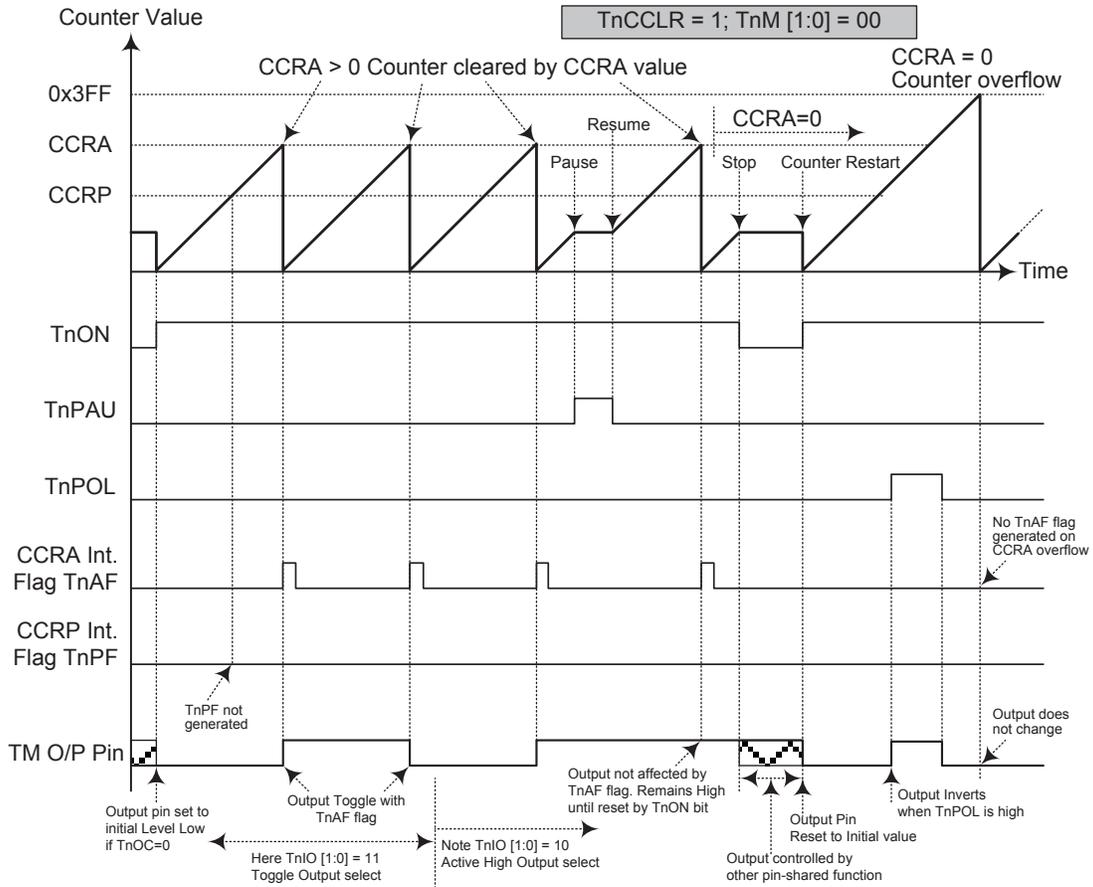
If the CCRA bits are all zero, the counter will overflow when it reaches its maximum 10-bit, 3FF Hex, value, however here the TnAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the TM output pin, will change state. The TM output pin condition however only changes state when a TnAF interrupt request flag is generated after a compare match occurs from Comparator A. The TnPF interrupt request flag, generated from a compare match from Comparator P, will have no effect on the TM output pin. The way in which the TM output pin changes state are determined by the condition of the TnIO1 and TnIO0 bits in the PTMnC1 register. The TM output pin can be selected using the TnIO1 and TnIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the TM output pin, which is setup after the TnON bit changes from low to high, is setup using the TnOC bit. Note that if the TnIO1, TnIO0 bits are zero then no pin change will take place.



**Compare Match Output Mode – TnCCLR = 0 (n=1 or 2)**

- Note: 1. With  $TnCCLR = 0$  – a Comparator P match will clear the counter  
2. The TM output pin is controlled only by the TnAF flag  
3. The output pin is reset to initial state by a TnON bit rising edge



**Compare Match Output Mode – TnCCLR = 1 (n=1 or 2)**

- Note: 1. With TnCCLR = 1 – a Comparator A match will clear the counter
2. The TM output pin is controlled only by the TnAF flag
  3. The output pin is reset to initial state by a TnON rising edge
  4. The TnPF flag is not generated when TnCCLR = 1

**Timer/Counter Mode**

To select this mode, bits TnM1 and TnM0 in the PTMnC1 register should all be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the TM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

**PWM Output Mode**

To select this mode, bits TnM1 and TnM0 in the PTMnC1 register should be set to 10 respectively and also the TnIO1 and TnIO0 bits should be set to 10 respectively. The PWM function within the TM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the TM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM mode, the TnCCLR bit has no effect as the PWM period. Both of the CCRP and CCRA registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The TnOC bit in the PTMnC1 register is used to select the required polarity of the PWM waveform while the two TnIO1 and TnIO0 bits are used to enable the PWM output or to force the TM output pin to a fixed high or low level. The TnPOL bit is used to reverse the polarity of the PWM output waveform.

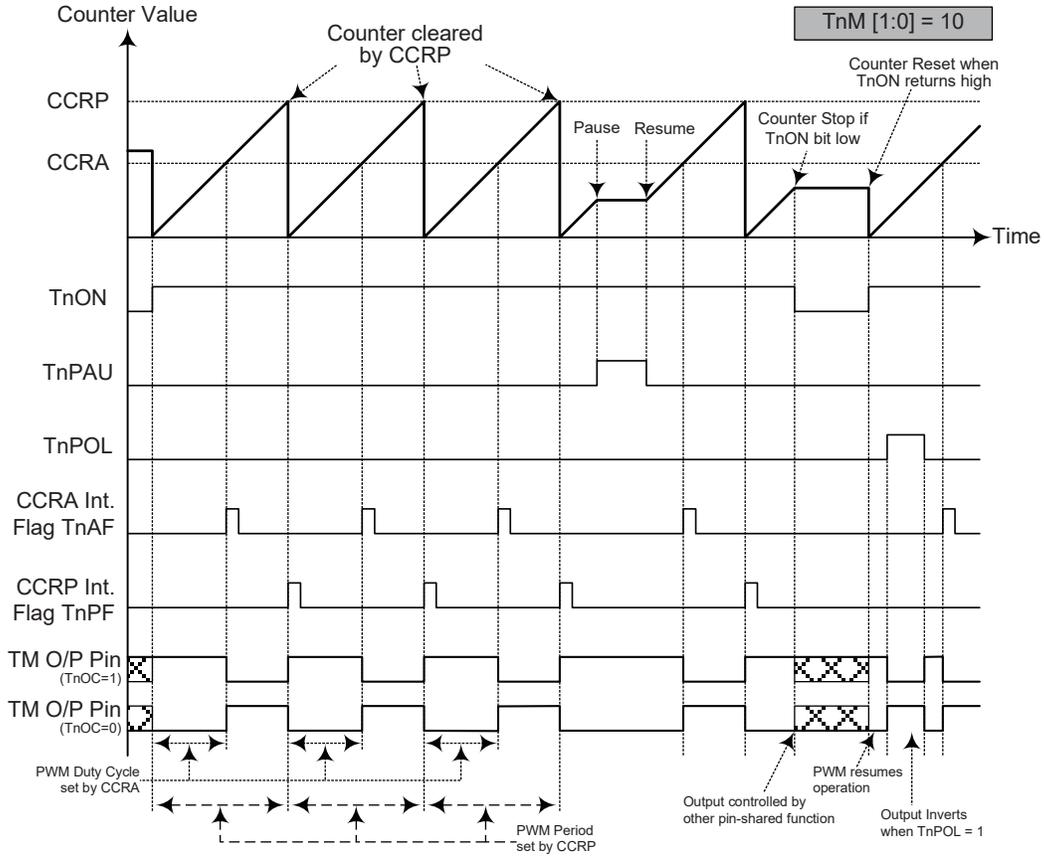
• **10-bit PTM, PWM Mode**

CCRP	0	1~1023
Period	1024	1~1023
Duty	CCRA	

If  $f_{SYS} = 16\text{MHz}$ , TM clock source select  $f_{SYS}/4$ , CCRP = 100b and CCRA = 128,

The PTM PWM output frequency =  $(f_{SYS}/4) / 512 = f_{SYS}/2048 = 7.8125\text{kHz}$ , duty =  $128/512 = 25\%$ ,

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.



**PWM Mode (n=1 or 2)**

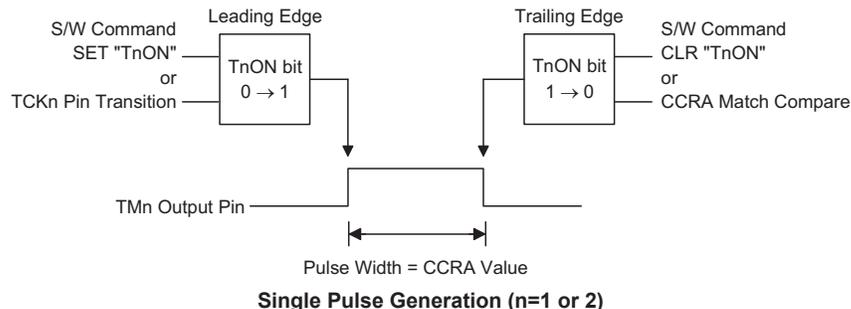
- Note:
1. Here Counter cleared by CCRP
  2. A counter clear sets the PWM Period
  3. The internal PWM function continues running even when  $TnIO[1:0] = 00$  or  $01$
  4. The  $TnCCLR$  bit has no influence on PWM operation

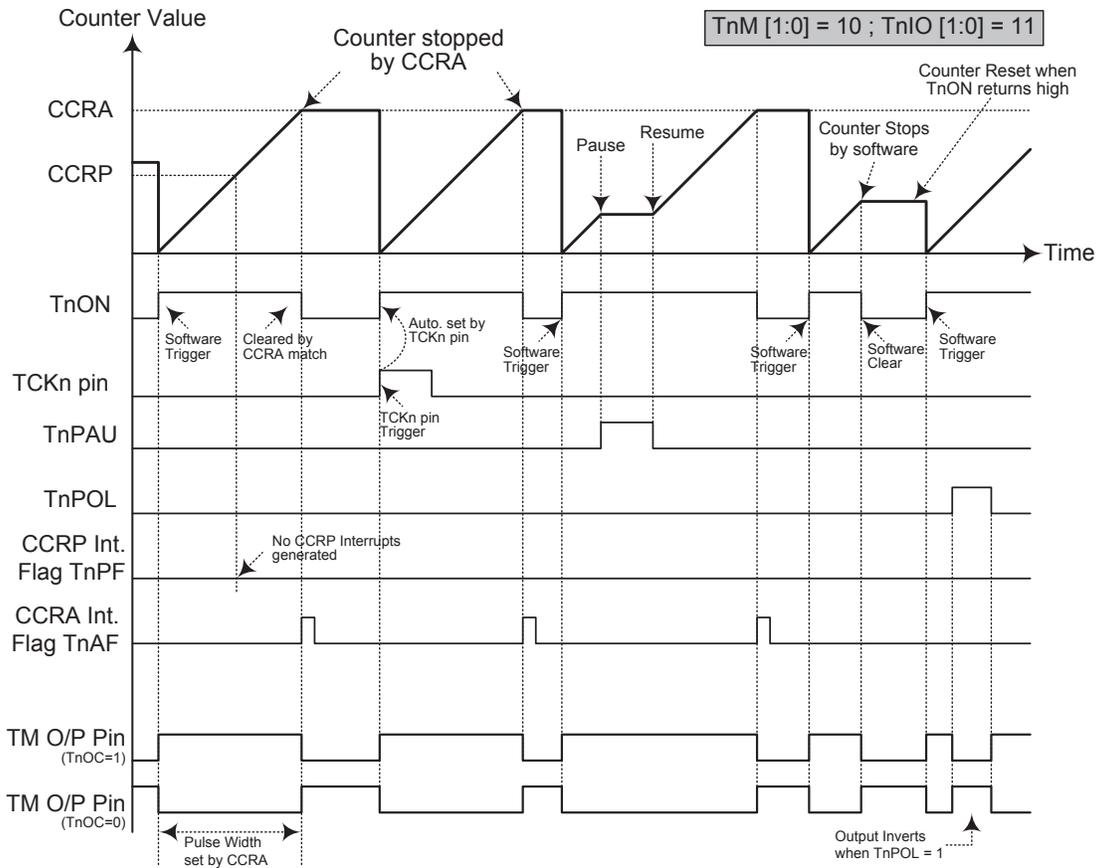
### Single Pulse Output Mode

To select this mode, the required bit pairs, TnM1 and TnM0 should be set to 10 respectively and also the corresponding TnIO1 and TnIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the TM output pin.

The trigger for the pulse output leading edge is a low to high transition of the TnON bit, which can be implemented using the application program. However in the Single Pulse Mode, the TnON bit can also be made to automatically change from low to high using the external TCKn pin, which will in turn initiate the Single Pulse output. When the TnON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The TnON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the TnON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However a compare match from Comparator A will also automatically clear the TnON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate TM interrupts. The counter can only be reset back to zero when the TnON bit changes from low to high when the counter restarts. In the Single Pulse Mode CCRP is not used. The TnCCLR bit is also not used.





**Single Pulse Mode (n=1 or 2)**

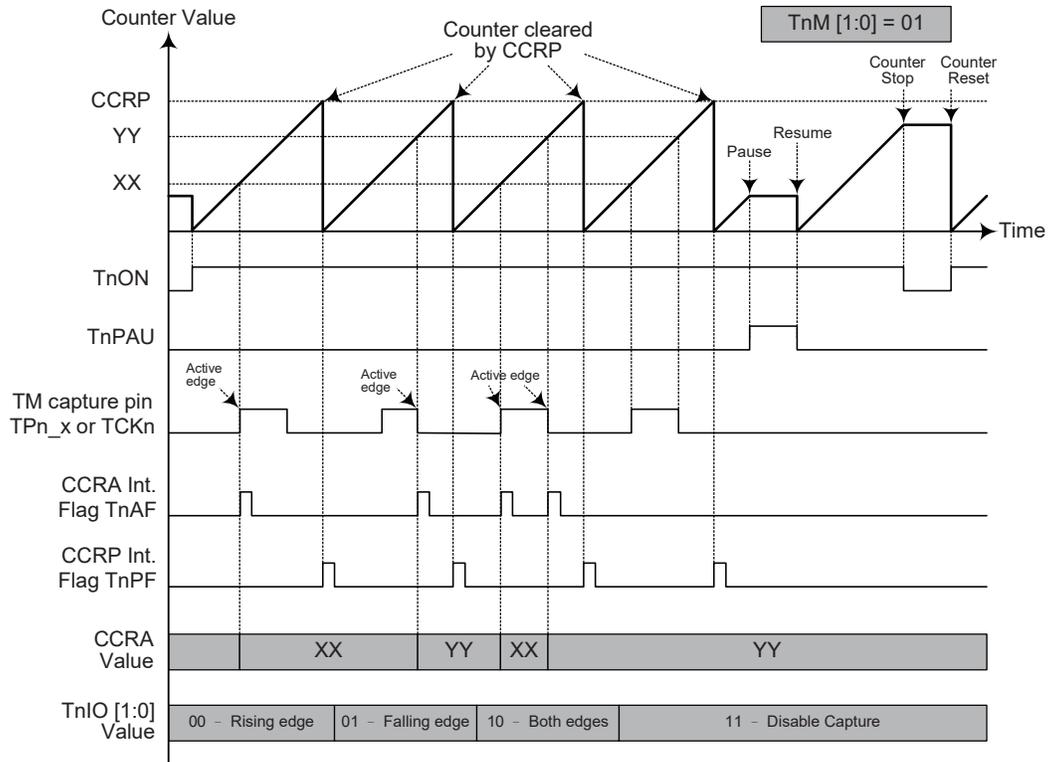
- Note: 1. Counter stopped by CCRA  
 2. CCRP is not used  
 3. The pulse is triggered by the TCKn pin or by setting the TnON bit high  
 4. A TCKn pin active edge will automatically set the TnON bit high  
 5. In the Single Pulse Mode, TnIO [1:0] must be set to "11" and cannot be changed.

### **Capture Input Mode**

To select this mode bits TnM1 and TnM0 in the PTMnC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external signal is supplied on the TPn\_0, TPn\_1 or TCKn pin, selected by the TnCKS bit in the PTMnC1 register. The input pin active edge can be either a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the TnIO1 and TnIO0 bits in the PTMnC1 register. The counter is started when the TnON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the TPn\_0, TPn\_1 or TCKn pin the present value in the counter will be latched into the CCRA register and a TM interrupt generated. Irrespective of what events occur on the TPn\_0, TPn\_1 or TCKn pin the counter will continue to free run until the TnON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a TM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The TnIO1 and TnIO0 bits can select the active trigger edge on the TPn\_0, TPn\_1 or TCKn pin to be a rising edge, falling edge or both edge types. If the TnIO1 and TnIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the TPn\_0, TPn\_1 or TCKn pin, however it must be noted that the counter will continue to run.

As the TPn\_0, TPn\_1 or TCKn pin is pin shared with other functions, care must be taken if the TMn is in the Capture Input Mode. This is because if the pin is setup as an output, then any transitions on this pin may cause an input capture operation to be executed. The TnCCLR, TnOC and TnPOL bits are not used in this Mode.



**Capture Input Mode (n=1 or 2)**

- Note: 1. TnM[1:0] = 01 and active edge set by the TnIO[1:0] bits  
 2. A TM Capture input pin active edge transfers counter value to CCRA  
 3. The TnCCLR bit is not used  
 4. No output function – TnOC and TnPOL bits are not used  
 5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero

## Standard Type TM – STM (TM3)

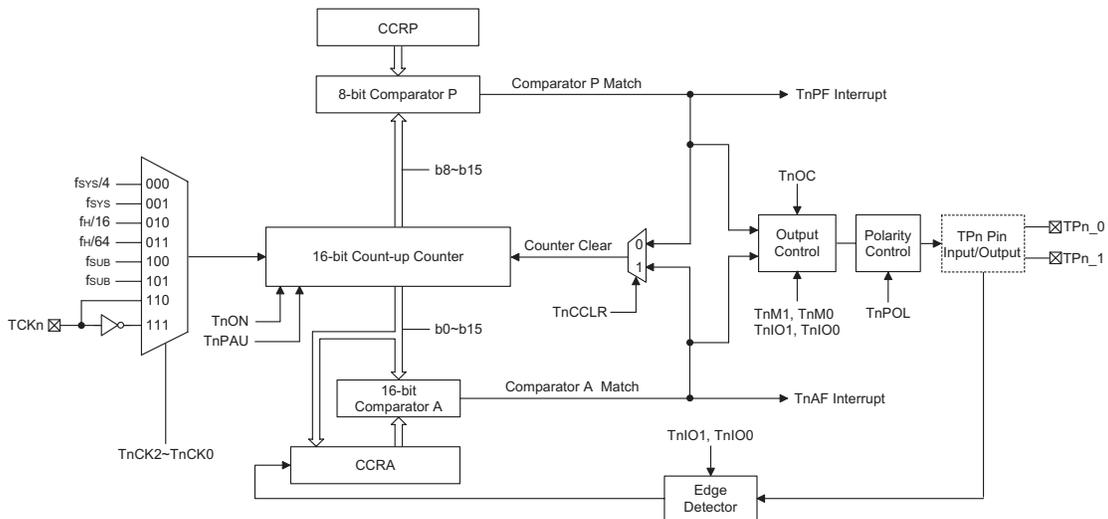
The Standard Type TM contains five operating modes, which are Compare Match Output, Timer/Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Standard TM can also be controlled with an external input pin and can drive two external output pins.

Device	Name	TM No.	TM Input Pin	TM Output Pin
HT67F5650	16-bit STM	3	TCK3	TP3_0, TP3_1
HT67F5660				

### Standard TM Operation

There is a 16-bit wide STM. At the core is a 16-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP comparator is 8-bit wide whose value is compared with the highest 8 bits in the counter while the CCRA is the 16 bits and therefore compares all counter bits.

The only way of changing the value of the 16-bit counter using the application program, is to clear the counter by changing the TnON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a TM interrupt signal will also usually be generated. The Standard Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control the output pin. All operating setup conditions are selected using relevant internal registers.



**Standard Type TM Block Diagram (n=3)**

### Standard Type TM Register Description

Overall operation of the Standard TM is controlled using a series of registers. A read only register pair exists to store the internal counter 16-bit value, while a read/write register pair exists to store the internal 16-bit CCRA value. There is also a read/write register used to store the internal 8-bit CCRP value. The remaining two registers are control registers which setup the different operating and control modes.

Register Name	Bit							
	7	6	5	4	3	2	1	0
STMnC0	TnPAU	TnCK2	TnCK1	TnCK0	TnON	—	—	—
STMnC1	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
STMnDL	D7	D6	D5	D4	D3	D2	D1	D0
STMnDH	D15	D14	D13	D12	D11	D10	D9	D8
STMnAL	D7	D6	D5	D4	D3	D2	D1	D0
STMnAH	D15	D14	D13	D12	D11	D10	D9	D8
STMnRP	D7	D6	D5	D4	D3	D2	D1	D0

**16-bit Standard TM Registers List (n=3)**

#### STMnC0 Register (n=3)

Bit	7	6	5	4	3	2	1	0
Name	TnPAU	TnCK2	TnCK1	TnCK0	TnON	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	—	—	—
POR	0	0	0	0	0	—	—	—

**Bit 7 TnPAU:** TMn Counter Pause Control  
0: Run  
1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

**Bit 6~4 TnCK2~TnCK0:** Select TMn Counter clock  
000:  $f_{SYS}/4$   
001:  $f_{SYS}$   
010:  $f_H/16$   
011:  $f_H/64$   
100:  $f_{SUB}$   
101:  $f_{SUB}$   
110: TCKn rising edge clock  
111: TCKn falling edge clock

These three bits are used to select the clock source for the TM. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source  $f_{SYS}$  is the system clock, while  $f_H$  and  $f_{SUB}$  are other internal clocks, the details of which can be found in the oscillator section.

Bit 3 **TnON**: TMn Counter On/Off Control  
0: Off  
1: On

This bit controls the overall on/off function of the TM. Setting the bit high enables the counter to run, clearing the bit disables the TM. Clearing this bit to zero will stop the counter from counting and turn off the TM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value. If the TM is in the Compare Match Output Mode or the PWM output Mode or Single Pulse Output Mode then the TM output pin will be reset to its initial condition, as specified by the TnOC bit, when the TnON bit changes from low to high.

Bit 2~0 Unimplemented, read as "0"

### STMnC1 Register (n=3)

Bit	7	6	5	4	3	2	1	0
Name	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **TnM1~TnM0**: Select TMn Operating Mode  
00: Compare Match Output Mode  
01: Capture Input Mode  
10: PWM Mode or Single Pulse Output Mode  
11: Timer/Counter Mode

These bits setup the required operating mode for the TM. To ensure reliable operation the TM should be switched off before any changes are made to the TnM1 and TnM0 bits. In the Timer/Counter Mode, the TM output pin state is undefined.

Bit 5~4 **TnIO1~TnIO0**: Select TPn\_0 or TPn\_1 output function

Compare Match Output Mode

- 00: No change
- 01: Output low
- 10: Output high
- 11: Toggle output

PWM Mode/Single Pulse Output Mode

- 00: PWM Output inactive state
- 01: PWM Output active state
- 10: PWM output
- 11: Single pulse output

Capture Input Mode

- 00: Input capture at rising edge of TPn\_0 or TPn\_1
- 01: Input capture at falling edge of TPn\_0 or TPn\_1
- 10: Input capture at falling/rising edge of TPn\_0 or TPn\_1
- 11: Input capture disabled

Timer/Counter Mode

Unused

These two bits are used to determine how the TM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the TM is running.

In the Compare Match Output Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the TM output pin should be setup using the TnOC bit in the STMnC1 register. Note that the output

level requested by the TnIO1 and TnIO0 bits must be different from the initial value setup using the TnOC bit otherwise no change will occur on the TM output pin when a compare match occurs. After the TM output pin changes state, it can be reset to its initial level by changing the level of the TnON bit from low to high.

In the PWM Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the TnIO1 and TnIO0 bits only after the TM has been switched off. Unpredictable PWM outputs will occur if the TnIO1 and TnIO0 bits are changed when the TM is running.

Bit 3 **TnOC**: TPn\_0 or TPn\_1 Output control bit

Compare Match Output Mode

0: Initial low

1: Initial high

PWM Mode/Single Pulse Output Mode

0: Active low

1: Active high

This is the output control bit for the TM output pin. Its operation depends upon whether TM is being used in the Compare Match Output Mode or in the PWM Mode/Single Pulse Output Mode. It has no effect if the TM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the TM output pin before a compare match occurs. In the PWM Mode it determines if the PWM signal is active high or active low.

Bit 2 **TnPOL**: TPn\_0 or TPn\_1 Output polarity Control

0: Non-invert

1: Invert

This bit controls the polarity of the TPn\_0 or TPn\_1 output pin. When the bit is set high the TM output pin will be inverted and not inverted when the bit is zero. It has no effect if the TM is in the Timer/Counter Mode.

Bit 1 **TnDPX**: TMn PWM period/duty Control

0: CCRP - period; CCRA - duty

1: CCRP - duty; CCRA - period

This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0 **TnCCLR**: Select TMn Counter clear condition

0: TMn Comparator P match

1: TMn Comparator A match

This bit is used to select the method which clears the counter. Remember that the Compact TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the TnCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The TnCCLR bit is not used in the PWM Mode, Single Pulse or Input Capture Mode.

#### STMnDL Register (n=3)

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D7~D0**: TMn Counter Low Byte Register bit 7 ~ bit 0

TMn 16-bit Counter bit 7 ~ bit 0

**STMnDH Register (n=3)**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D15~D8**: TMn Counter High Byte Register bit 7 ~ bit 0  
TMn 16-bit Counter bit 15 ~ bit 8

**STMnAL Register (n=3)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D7~D0**: TMn CCRA Low Byte Register bit 7 ~ bit 0  
TMn 16-bit CCRA bit 7 ~ bit 0

**STMnAH Register (n=3)**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D15~D8**: TMn CCRA High Byte Register bit 7 ~ bit 0  
TMn 16-bit CCRA bit 15 ~ bit 8

**STMnRP Register (n=3)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **D7~D0**: TMn CCRP Register bit 7 ~ bit 0, compared with the TMn Counter bit 15~bit 8.  
Comparator P Match Period  
0: 65536 TMn clocks  
1~255: 256×(1~255) TMn clocks

These eight bits are used to setup the value on the internal CCRP 8-bit register, which are then compared with the internal counter's highest eight bits. The result of this comparison can be selected to clear the internal counter if the TnCCLR bit is set to zero. Setting the TnCCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest eight counter bits, the compare values exist in 256 clock cycle multiples. Clearing all eight bits to zero is in effect allowing the counter to overflow at its maximum value.

## Standard Type TM Operating Modes

The Standard Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the TnM1 and TnM0 bits in the STMnC1 register.

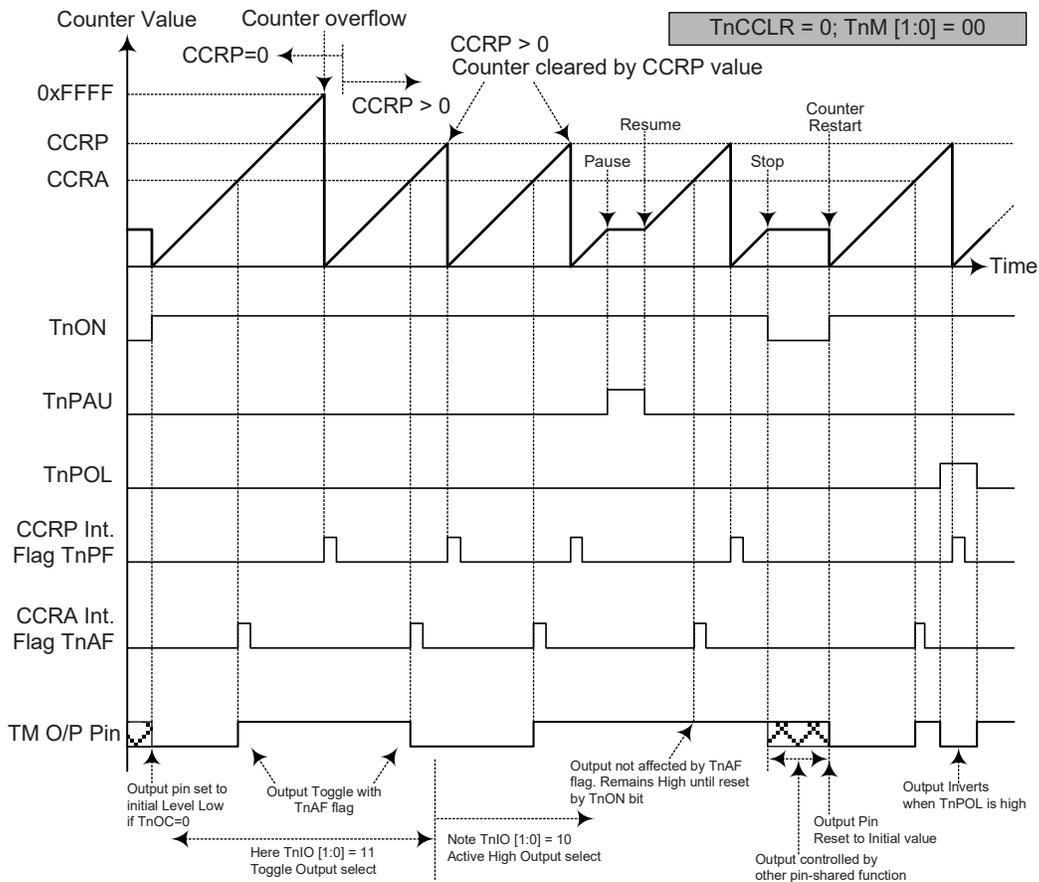
### Compare Output Mode

To select this mode, bits TnM1 and TnM0 in the STMnC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the TnCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both TnAF and TnPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the TnCCLR bit in the STMnC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the TnAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when TnCCLR is high no TnPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA cannot be set to "0".

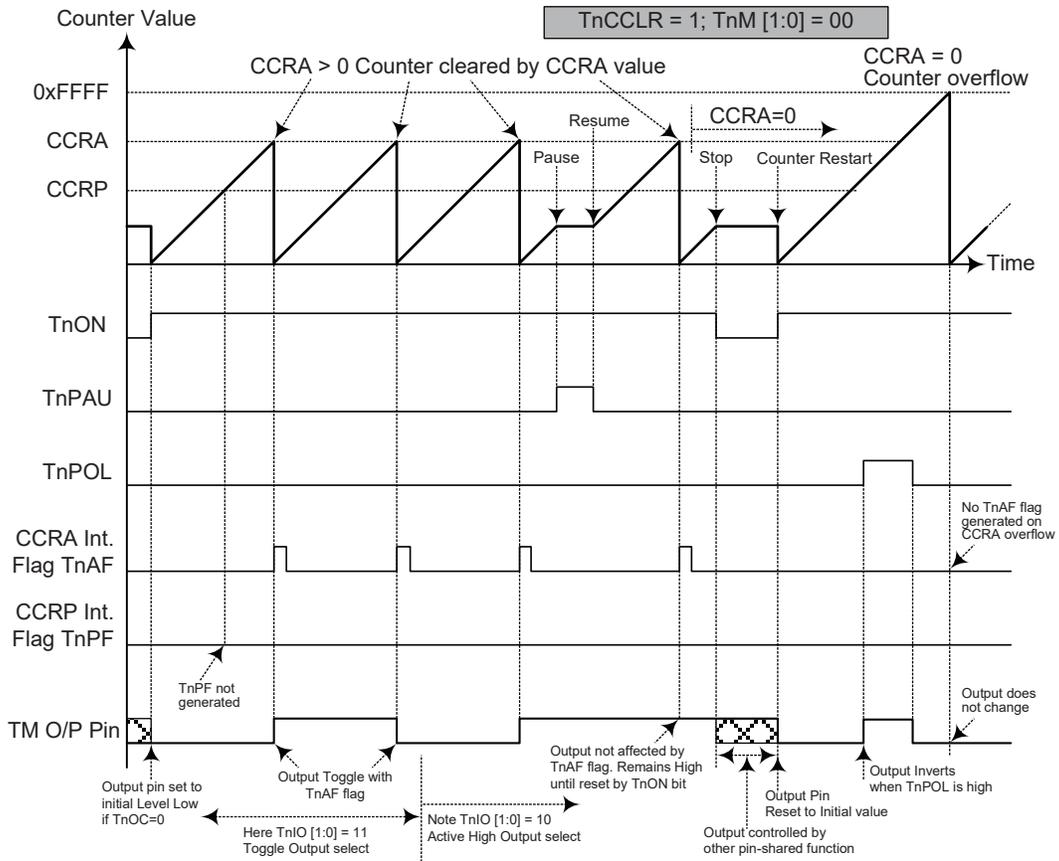
If the CCRA bits are all zero, the counter will overflow when it reaches its maximum 16-bit, FFFF Hex, value, however here the TnAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the TM output pin, will change state. The TM output pin condition however only changes state when a TnAF interrupt request flag is generated after a compare match occurs from Comparator A. The TnPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the TM output pin. The way in which the TM output pin changes state are determined by the condition of the TnIO1 and TnIO0 bits in the STMnC1 register. The TM output pin can be selected using the TnIO1 and TnIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the TM output pin, which is setup after the TnON bit changes from low to high, is setup using the TnOC bit. Note that if the TnIO1 and TnIO0 bits are zero then no pin change will take place.



**Compare Match Output Mode – TnCCLR = 0 (n=3)**

- Note: 1. With TnCCLR=0 a Comparator P match will clear the counter  
 2. The TM output pin is controlled only by the TnAF flag  
 3. The output pin is reset to its initial state by a TnON bit rising edge



**Compare Match Output Mode – TnCCLR = 1 (n=3)**

- Note: 1. With  $TnCCLR=1$  a Comparator A match will clear the counter
2. The TM output pin is controlled only by the TnAF flag
3. The output pin is reset to its initial state by a TnON bit rising edge
4. A TnPF flag is not generated when  $TnCCLR=1$

### Timer/Counter Mode

To select this mode, bits TnM1 and TnM0 in the STMnC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the TM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

### PWM Output Mode

To select this mode, bits TnM1 and TnM0 in the STMnC1 register should be set to 10 respectively and also the TnIO1 and TnIO0 bits should be set to 10 respectively. The PWM function within the TM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the TM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM mode, the TnCCLR bit has no effect as the PWM period. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. Which register is used to control either frequency or duty cycle is determined using the TnDPX bit in the STMnC1 register. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The TnOC bit in the STMnC1 register is used to select the required polarity of the PWM waveform while the two TnIO1 and TnIO0 bits are used to enable the PWM output or to force the TM output pin to a fixed high or low level. The TnPOL bit is used to reverse the polarity of the PWM output waveform.

- **16-bit STM, PWM Mode, Edge-aligned Mode, TnDPX=0**

CCRP	1~255	0
Period	CCRP×256	65536
Duty	CCRA	

If  $f_{SYS} = 16\text{MHz}$ , TM clock source select  $f_{SYS}/4$ , CCRP = 2 and CCRA = 128,

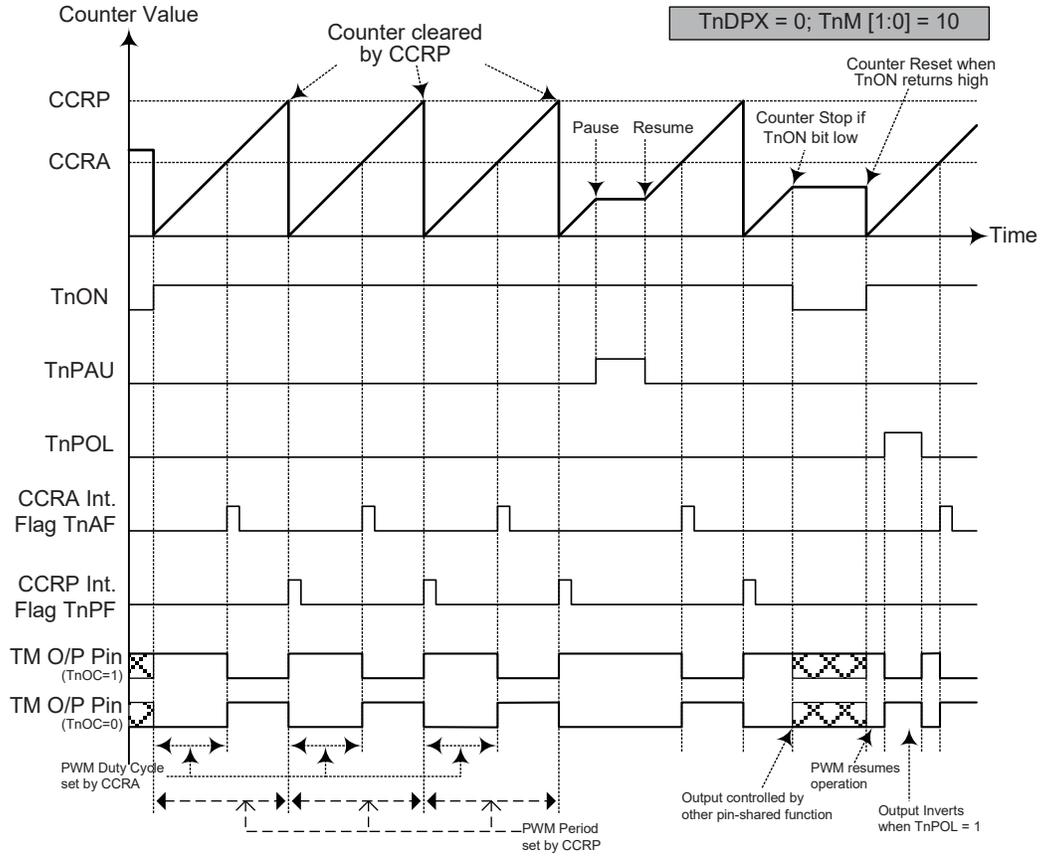
The STM PWM output frequency =  $(f_{SYS}/4)/(2 \times 256) = f_{SYS}/2048 = 7.8125\text{kHz}$ , duty =  $128/(2 \times 256) = 25\%$ .

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

- **16-bit STM, PWM Mode, Edge-aligned Mode, TnDPX=1**

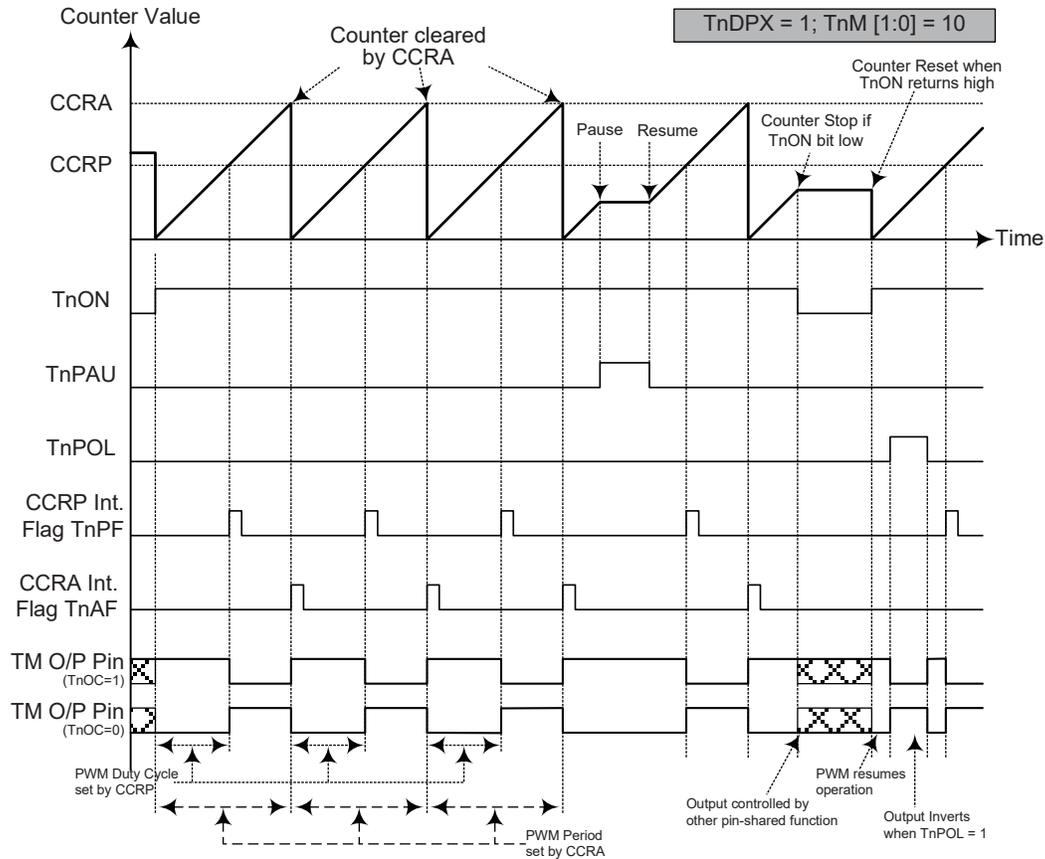
CCRP	1~255	0
Period	CCRA	
Duty	CCRP×256	65536

The PWM output period is determined by the CCRA register value together with the TM clock while the PWM duty cycle is defined by the (CCRP×256) except when the CCRP value is equal to 000b.



**PWM Mode – TnDPX = 0 (n=3)**

- Note: 1. Here TnDPX=0 – Counter cleared by CCRP
2. A counter clear sets the PWM Period
3. The internal PWM function continues running even when TnIO [1:0] = 00 or 01
4. The TnCCLR bit has no influence on PWM operation



**PWM Mode – TnDPX = 1 (n=3)**

Note: 1. Here TnDPX=1 – Counter cleared by CCRA

2. A counter clear sets the PWM Period

3. The internal PWM function continues even when TnIO [1:0] = 00 or 01

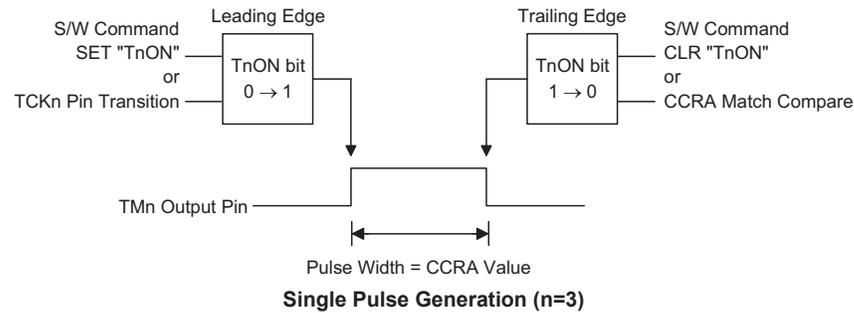
4. The TnCCLR bit has no influence on PWM operation

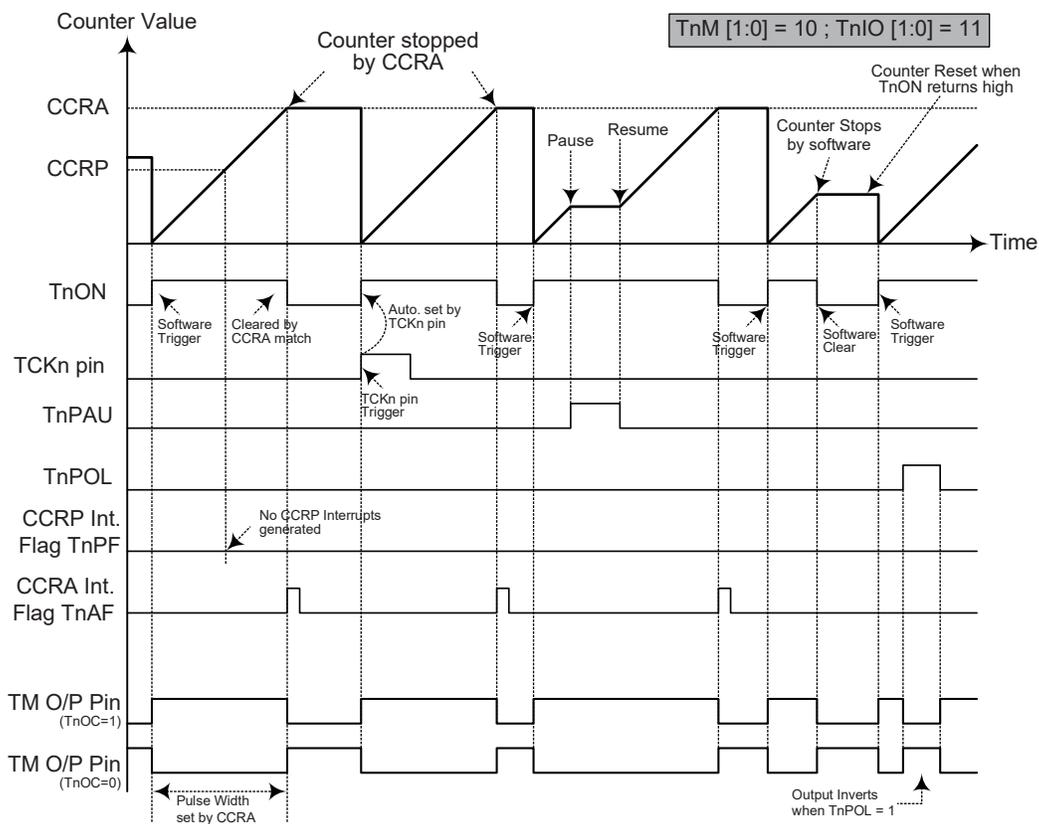
### Single Pulse Mode

To select this mode, bits TnM1 and TnM0 in the STMnC1 register should be set to 10 respectively and also the TnIO1 and TnIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the TM output pin.

The trigger for the pulse output leading edge is a low to high transition of the TnON bit, which can be implemented using the application program. However in the Single Pulse Mode, the TnON bit can also be made to automatically change from low to high using the external TCKn pin, which will in turn initiate the Single Pulse output. When the TnON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The TnON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the TnON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However a compare match from Comparator A will also automatically clear the TnON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate a TM interrupt. The counter can only be reset back to zero when the TnON bit changes from low to high when the counter restarts. In the Single Pulse Mode CCRP is not used. The TnCCLR and TnDPX bits are not used in this Mode.





**Single Pulse Mode (n=3)**

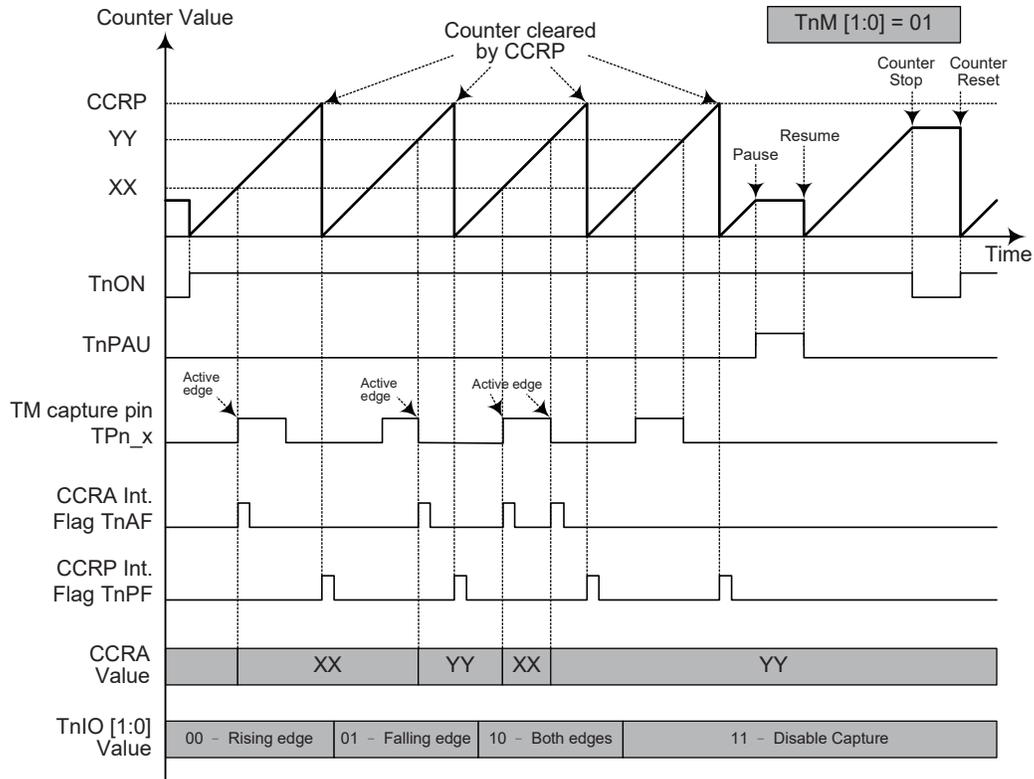
- Note:
1. Counter stopped by CCRA
  2. CCRP is not used
  3. The pulse is triggered by the TCKn pin or by setting the TnON bit high
  4. A TCKn pin active edge will automatically set the TnON bit high
  5. In the Single Pulse Mode, TnIO [1:0] must be set to "11" and cannot be changed.

### **Capture Input Mode**

To select this mode bits TnM1 and TnM0 in the STMnC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external signal is supplied on the TPn\_0 or TPn\_1 pin, whose active edge can be a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the TnIO1 and TnIO0 bits in the STMnC1 register. The counter is started when the TnON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the TPn\_0 or TPn\_1 pin the present value in the counter will be latched into the CCRA registers and a TM interrupt generated. Irrespective of what events occur on the TPn\_0 or TPn\_1 pin the counter will continue to free run until the TnON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a TM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The TnIO1 and TnIO0 bits can select the active trigger edge on the TPn\_0 or TPn\_1 pin to be a rising edge, falling edge or both edge types. If the TnIO1 and TnIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the TPn\_0 or TPn\_1 pin, however it must be noted that the counter will continue to run.

As the TPn\_0 or TPn\_1 pin is pin shared with other functions, care must be taken if the TM is in the Input Capture Mode. This is because if the pin is setup as an output, then any transitions on this pin may cause an input capture operation to be executed. The TnCCLR and TnDPX bits are not used in this Mode.

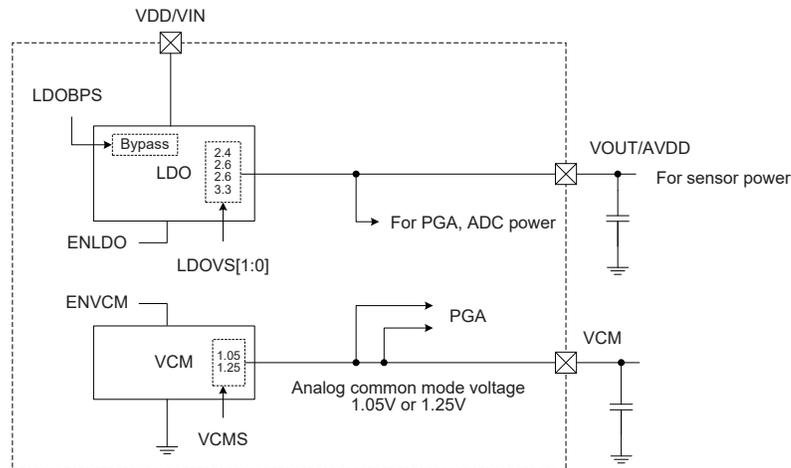


#### Capture Input Mode (n=3)

- Note: 1. TnM [1:0] = 01 and active edge set by the TnIO [1:0] bits
2. A TM Capture input pin active edge transfers the counter value to CCRA
3. TnCCLR bit not used
4. No output function – TnOC and TnPOL bits are not used
5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero.

## Internal Power Supply

Each device contains the LDO and VCM for the regulated power supply. The accompanying block diagram illustrates the basic functional operation. The internal LDO can provide the fixed voltage for PGA, ADC or the external components; as well the VCM can be used as the reference voltage for ADC module. There are four LDO voltage levels, 2.4V, 2.6V, 2.9V or 3.3V, decided by LDOVS1~LDOVS0 bits in the PWRC register, as well the VCM has two output voltage levels, 1.05V or 1.25V, selected by the VCMS bit in the PGAC1 register. The LDO and VCM functions can be controlled by the ENLDO and ENVCM bits respectively and can be powered off to reduce the power consumption. In addition, the LDO bypass function can be enabled or disabled by the LDOBPS bit in the PWRC register.



**Internal Power Supply Block Diagram**

Registers			Output Voltage	
ADOFF	ENLDO	ENVCM	VOUT/AVDD	VCM
1	0	x	Disable	Disable
1	1	x	Enable	Disable
0	0	0	Disable	Disable
0	1	0	Enable	Disable
0	0	1	Disable	Disable
0	1	1	Enable	Enable

"x" means don't care

**Power Control Table**

**PWRC Register**

Bit	7	6	5	4	3	2	1	0
Name	ENLDO	ENVCM	—	—	—	LDOBPS	LDOVS1	LDOVS0
R/W	R/W	R/W	—	—	—	R/W	R/W	R/W
POR	0	0	—	—	—	0	0	0

- Bit 7      **ENLDO:** LDO function control bit  
 0: Disable  
 1: Enable  
 If the LDO is disabled, there will be no power consumption and LDO output pin is output low.
- Bit 6      **ENVCM:** VCM function control bit  
 0: Disable  
 1: Enable  
 If the VCM is disabled, there will be no power consumption and VCM output pin is floating.
- Bit 5~3    Unimplemented, read as "0"
- Bit 2      **LDOBPS:** LDO Bypass function control bit  
 0: Disable  
 1: Enable
- Bit 1~0    **LDOVS1~LDOVS0:** LDO output voltage selection  
 00: 2.4V  
 01: 2.6V  
 10: 2.9V  
 11: 3.3V

**PGAC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	VCMS	INIS	—	—	DCSET2	DCSET1	DCSET0	—
R/W	R/W	R/W	—	—	R/W	R/W	R/W	—
POR	1	0	—	—	0	0	0	—

- Bit 7      **VCMS:** Analog Common mode voltage selection  
 0: 1.05V  
 1: 1.25V
- Bit 6      **INIS:** The selected input ends, IN1 and IN2, connection control bit  
 Described elsewhere.
- Bit 5~4    Unimplemented, read as "0"
- Bit 3~1    **DCSET2~DCSET0:** The DI+/DI- differential input offset voltage adjustment control  
 Described elsewhere.
- Bit 0      Unimplemented, read as "0"

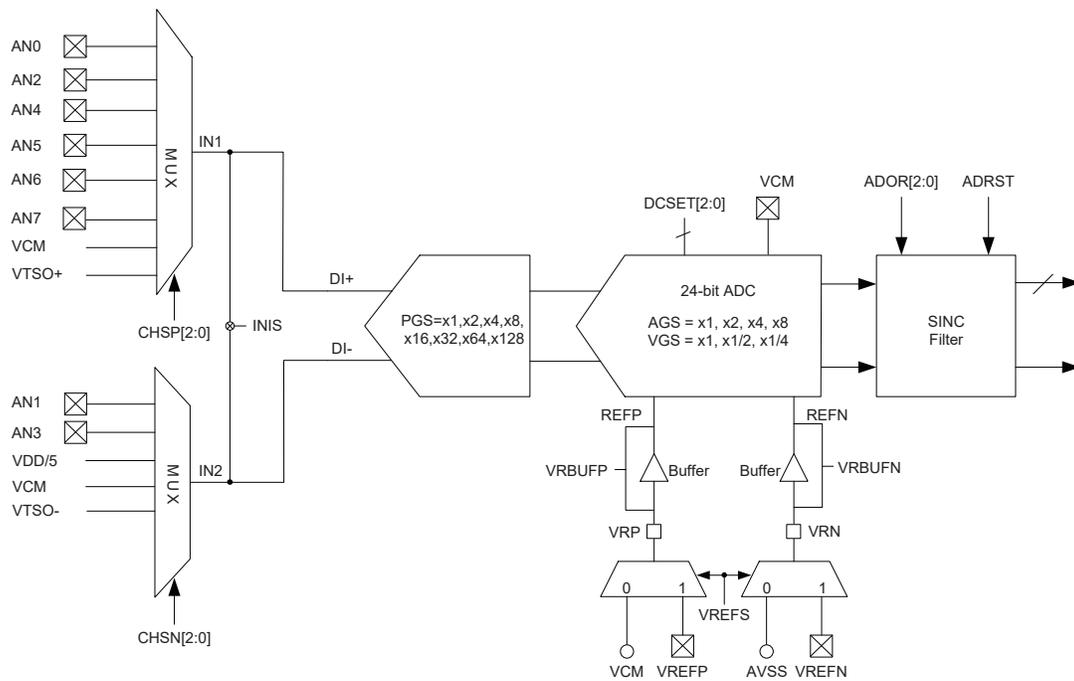
## Analog to Digital Converter – ADC

The need to interface to real world analog signals is a common requirement for many electronic systems. However, to properly process these signals by a microcontroller, they must first be converted into digital signals by A/D converters. By integrating the A/D conversion electronic circuitry into the microcontroller, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirements.

### A/D Overview

Each device contains a high accuracy multi-channel 24-bit Delta Sigma analog-to-digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into a 24-bit digital value.

In addition, the PGA gain control, ADC gain control and ADC reference gain control determine the amplification gain for ADC input signal. The designer can select the best gain combination for the desired amplification applied to the input signal. The following block diagram illustrates the ADC basic operational function. The ADC input channel can be arranged as four single-ended A/D input channels and two differential input channels. The input signal can be amplified by PGA before entering the 24-bit Delta Sigma ADC. The Delta Sigma ADC modulator will output one bit converted data to SINC filter which can transform the converted one-bit data to 24 bits and store them into the specific data registers. Additionally, these devices also provide a temperature sensor to compensate the A/D converter deviation caused by the temperature. With high accuracy and performance, these devices are very suitable for Weight Scale and similarly related products.



**A/D Converter Structure**

### A/D Data Rate Definition

The Delta Sigma ADC data rate can be calculated by the equation list below:

$$\text{Data Rate} = \text{ADC clock} / \text{ADOR}[2:0]$$

$$\text{ADC clock: } f_{\text{ADCK}} = f_{\text{MCLK}} / \text{FLMS}[2:0]$$

Where the ADC clock comes from  $f_{\text{MCLK}}$ , and FLMS[2:0] define a constant number which can only be 30 or 12, finally ADOR[2:0] define chopper average function (CHOP) and Over-Sampling Rating (OSR).

For example, if a data rate of 10Hz is desired, an  $f_{\text{MCLK}}$  clock source with a frequency of 4.9152MHz can be selected, then set FLMS[2:0] = 000b ( $f_{\text{MCLK}}$  divided by 30); finally set ADOR[2:0] = 001b to define CHOP = 2 and OSR = 8192.

$$\text{Thus Data Rate} = 4.9152\text{MHz} / (30 \times 2 \times 8192) = 10\text{Hz}$$

In addition, the A/D converter can provide a data output rate of 3.2kHz.

### A/D Converter Register Description

Overall operation of the A/D converter is controlled by using 9 registers. A group of read only registers exist to store the ADC data 24-bit value. The remaining 6 registers are control registers which set up the gain selections and control functions of the A/D converter.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PGAC0	—	VGS1	VGS0	AGS1	AGS0	PGS2	PGS1	PGS0
PGAC1	VCMS	INIS	—	—	DCSET2	DCSET1	DCSET0	—
PGACS	—	—	CHSN2	CHSN1	CHSN0	CHSP2	CHSP1	CHSP0
ADRL	D7	D6	D5	D4	D3	D2	D1	D0
ADRM	D15	D14	D13	D12	D11	D10	D9	D8
ADRH	D23	D22	D21	D20	D19	D18	D17	D16
ADCR0	ADRST	ADSLP	ADOFF	ADOR2	ADOR1	ADOR0	—	VREFS
ADCR1	FLMS2	FLMS1	FLMS0	VRBUFN	VRBUFP	ADCDL	EOC	—
ADCS	—	—	—	ADCK4	ADCK3	ADCK2	ADCK1	ADCK0

**A/D Converter Register List**

### Programmable Gain Amplifier – PGA

There are three registers related to the programmable gain control, PGAC0, PGAC1 and PGACS. The PGAC0 register is used to select the PGA gain, ADC gain and the ADC reference gain. As well, the PGAC1 register is used to define the input connection, differential input offset voltage adjustment control and the VCM voltage selection. In addition, The PGACS register is used to select the input ends for the PGA. Therefore, the input channels have to be determined by the CHSP2~0 and CHSN2~0 bits to determine which analog channel input pins, temperature detector inputs or internal power supply are actually connected to the internal differential A/D converter.

**PGAC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	VGS1	VGS0	AGS1	AGS0	PGS2	PGS1	PGS0
R/W	—	R/W						
POR	—	0	0	0	0	0	0	0

- Bit 7            Unimplemented, read as "0"
- Bit 6~5        **VGS1~VGS0**: VREF gain selection  
                  00: 1  
                  01: 1/2  
                  10: 1/4  
                  11: Reserved
- Bit 4~3        **AGS1~AGS0**: ADC gain selection  
                  00: 1  
                  01: 2  
                  10: 4  
                  11: 8
- Bit 2~0        **PGS2~PGS0**: PGA gain selection  
                  000: 1  
                  001: 2  
                  010: 4  
                  011: 8  
                  100: 16  
                  101: 32  
                  110: 64  
                  111: 128

**PGAC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	VCMS	INIS	—	—	DCSET2	DCSET1	DCSET0	—
R/W	R/W	R/W	—	—	R/W	R/W	R/W	—
POR	1	0	—	—	0	0	0	—

- Bit 7            **VCMS**: Analog Common mode voltage selection  
                  0: 1.05V  
                  1: 1.25V
- Bit 6            **INIS**: The selected input ends, IN1 and IN2, connection control bit  
                  0: Not shorted  
                  1: Shorted
- Bit 5~4        Unimplemented, read as "0"
- Bit 3~1        **DCSET2~DCSET0**: The DI+/DI- differential input offset voltage adjustment control  
                  000: +0V  
                  001: +0.25V<sub>R</sub>  
                  010: +0.5V<sub>R</sub>  
                  011: +0.75V<sub>R</sub>  
                  100: +0V  
                  101: -0.25V<sub>R</sub>  
                  110: -0.5V<sub>R</sub>  
                  111: -0.75V<sub>R</sub>
- Bit 0            Unimplemented, read as "0"

### PGACS Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	CHSN2	CHSN1	CHSN0	CHSP2	CHSP1	CHSP0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

- Bit 7~6 Unimplemented, read as "0"
- Bit 5~3 **CHSN2~CHSN0**: PGA negative input ends selection  
 000: AN1  
 001: AN3  
 010: reserved  
 011: reserved  
 100: reserved  
 101: VDD/5  
 110: VCM  
 111: Temperature sensor VTSO-
- Bit 2~0 **CHSP2~CHSP0**: PGA positive input ends selection  
 000: AN0  
 001: AN2  
 010: AN4  
 011: AN5  
 100: AN6  
 101: AN7  
 110: VCM  
 111: Temperature sensor VTSO+

Note: If the PGA is assigned the single end input to DI+, then the DI- input must be selected the VCM.

### A/D Converter Data Registers – ADRL, ADRM, ADRH

Each device contains an internal 24-bit Delta Sigma A/D converter, it requires three data registers to store the converted value. These are a high byte register, known as ADRH, a middle byte register, known as ADRM, and a low byte register, known as ADRL. After the conversion process takes place, these registers can be directly read by the microcontroller to obtain the digitised conversion value. D0~D23 are the A/D conversion result data bits.

#### ADRH Register

Bit	7	6	5	4	3	2	1	0
Name	D23	D22	D21	D20	D19	D18	D17	D16
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0 A/D conversion data Register bit 23~bit 16

#### ADRM Register

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0 A/D conversion data Register bit 15~bit 8

### ADRL Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0      A/D conversion data Register bit 7~bit 0

### A/D Converter Control Registers – ADCR0, ADCR1, ADCS

To control the function and operation of the A/D converter, three control registers known as ADCR0, ADCR1 and ADCS are provided. These 8-bit registers define functions such as the selection of which reference source is used to the internal ADC, the ADC clock source, the ADC output data rate as well as controlling the power-up function and monitoring the ADC end of conversion status.

#### ADCR0 Register

Bit	7	6	5	4	3	2	1	0
Name	ADRST	ADSLP	ADOFF	ADOR2	ADOR1	ADOR0	—	VREFS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W
POR	0	0	1	0	0	0	—	0

Bit 7      **ADRST**: ADC software reset control bit.  
0: Disable  
1: Enable

This bit is used to reset the ADC internal digital SINC filter. The bit is normally low but if set high and then cleared low again, the A/D converter will initiate a conversion process data.

Bit 6      **ADSLP**: ADC sleep mode control bit  
0: Normal mode  
1: Sleep mode

This bit is used for ADC sleep mode control bit. To set this bit high will force the ADC enter sleep mode which can reduce the power consumption and prevent the ADC start-up time.

Bit 5      **ADOFF**: ADC module power on/off control bit  
0: ADC module power on  
1: ADC module power off

This bit controls the power of the ADC module. This bit should be cleared to zero to enable the A/D converter. If the bit is set high then the ADC will be switched off reducing the device power consumption. As the ADC will consume a limited amount of power, even when not executing a conversion, this may be an important consideration in power sensitive battery powered applications.

Note: 1. It is recommended to set ADOFF=1 before entering IDLE/SLEEP Mode for saving power.

2. ADOFF=1 will power down the ADC module, no matter the settings of ADSLP and ADRST bits.

3. The relationship about these bits, ADOFF, ADSLP and ADRST, will be further described elsewhere.

- Bit 4 ~ 2    **ADOR2~ADOR0**: Output data rate selection  
 Normal Mode: Output Data Rate  
     000: CHOP = 2, OSR=16384  
     001: CHOP = 2, OSR=8192  
     010: CHOP = 2, OSR=4096  
     011: CHOP = 2, OSR=2048  
     100: CHOP = 2, OSR=1024  
     101: CHOP = 2, OSR=512  
     110: CHOP = 2, OSR=256  
     111: CHOP = 2, OSR=128  
 Low Latency Mode: Output Data Rate  
     000: CHOP = 1, OSR=16384  
     001: CHOP = 1, OSR=8192  
     010: CHOP = 1, OSR=4096  
     011: CHOP = 1, OSR=2048  
     100: CHOP = 1, OSR=1024  
     101: CHOP = 1, OSR=512  
     110: CHOP = 1, OSR=256  
     111: CHOP = 1, OSR=128
- Bit 1        Unimplemented, read as „0”
- Bit 0        **VREFS**: ADC reference source selection  
     0: Internal reference (VCM, AVSS)  
     1: External reference (VREFP,VREFN)

**ADCR1 Register**

Bit	7	6	5	4	3	2	1	0
Name	FLMS2	FLMS1	FLMS0	VRBUFN	VRBUFP	ADCDL	EOC	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	0	0	0	0	0	0	0	—

- Bit 7 ~ 5    **FLMS2~FLMS0**: ADC output data mode and clock division ratio selection  
     000: Normal Mode, ADC clock =  $f_{MCLK} / 30$   
     010: Normal Mode, ADC clock =  $f_{MCLK} / 12$   
     100: Low Latency Mode, ADC clock =  $f_{MCLK} / 30$   
     110: Low Latency Mode, ADC clock =  $f_{MCLK} / 12$   
     Others: Reserved
- Bit 4        **VRBUFN**: VRN Buffer Enable  
     0: Disable  
     1: Enable
- Bit 3        **VRBUFP**: VRP Buffer Enable  
     0: Disable  
     1: Enable
- Bit 2        **ADCDL**: ADC converted data latch function  
     0: Disable data latch  
     1: Enable data latch

If the ADC converted data latch function is enabled, the latest converted data value will be latched and not be updated by any subsequent converted results until this function is disabled. Although the converted data is latched into the data registers, the ADC circuits remain operational, but will not generate interrupt and EOC will not change. It is recommended that this bit should be set high before reading the converted data in the ADRL, ADRM and ADRH registers. After the converted data has been read out, the bit can then be cleared to low to disable the ADC data latch function and allow further conversion values to be stored. In this way, the possibility of obtaining undesired data during ADC conversions can be prevented.

- Bit 1      **EOC**: End of A/D conversion flag  
             0: A/D conversion in progress  
             1: A/D conversion ended  
             This bit must be cleared by software.
- Bit 0      Unimplemented, read as "0"

**ADCS Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	ADCK4	ADCK3	ADCK2	ADCK1	ADCK0
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	0	0	0	0	0

- Bit 7~5      Unimplemented, read as "0"
- Bit 4~0      **ADCK4~ADCK0**: Select ADC clock source ( $f_{MCLK}$ )  
             00000~11110:  $f_{SYS}/2 / (ADCK[4:0]+1)$   
             11111:  $f_{SYS}$   
             Due to the ADC clock source,  $f_{MCLK}$ , is typically designed as 4.9152MHz and the MCU might be selected to work at different system clock, therefore, the designer should use the ADCK4~ADCK0 bits to get the fixed 4.9152MHz ADC working clock source. For example, if the system clock is 9.8304MHz, the ADCK[4:0] must be 0 to get the  $f_{MCLK}=4.9152MHz$ .

**A/D Operation**

The ADC provides three operational modes, which are Power down mode, Sleep mode and Reset mode, controlled respectively by the ADOFF, ADSLP and ADRST bits in the ADCR0 register. The following table illustrates the operating mode selection.

ADOFF	ADSLP	ADRST	Operating mode	Description
1	x	x	Power down mode	PGA off, ADC off
0	1	x	Sleep mode	PGA on, ADC off
0	0	1	Reset mode	PGA on, ADC on, SINC Reset

"x" unknown

**A/D operation mode selection**

To enable the ADC, the first step is to disable the ADC power down and sleep mode, to make sure the ADC is powered up. The ADRST bit in the ADCR0 register is used to start and reset the A/D converter after power on. When the microcontroller sets this bit from low to high and then low again, an analog to digital converted data in SINC filter will be initiated. After this setup is complete, the ADC is ready for operation. These three bits are used to control the overall start operation of the internal analog to digital converter.

The EOC bit in the ADCR1 register is used to indicate when the analog to digital conversion process is complete. This bit will be automatically set high by the microcontroller after a conversion cycle has ended. In addition, the corresponding A/D interrupt request flag will be set in the interrupt control register, and if the interrupts are enabled, an appropriate internal interrupt signal will be generated. This A/D internal interrupt signal will direct the program flow to the associated A/D internal interrupt address for processing. If the A/D internal interrupt is disabled, the microcontroller can be used to poll the EOC bit in the ADCR1 register to check whether it has been set "1" as an alternative method of detecting the end of an A/D conversion cycle. The ADC converted data will be updated continuously by the new converted data. If the ADC converted data latch function is enabled, the latest converted data will be latched and the following new converted data will be discarded until this data latch function is disabled.

The clock source for the A/D converter should be typically fixed at a value of 4.9152MHz, which originates from the system clock  $f_{SYS}$ , and can be chosen to be either  $f_{SYS}$  or a subdivided version of  $f_{SYS}$ . The division ratio value is determined by the ADCK4~ADCK0 bits in the ADCS register to obtain a 4.9152MHz clock source for the ADC.

The differential reference voltage supply to the A/D Converter can be supplied from either the internal power supply pins, VCM and AVSS, or from an external reference source supplied on pins, VREFP and VREFN. The desired selection is made using the VREFS bit in the ADCR0 register.

### Summary of A/D Conversion Steps

The following summarises the individual steps that should be executed in order to implement an A/D conversion process.

- Step 1  
Enable power LDO, VCM for PGA and ADC.
- Step 2  
Select PGA, ADC and  $V_{REF}$  gains by PGAC0 register.
- Step 3  
Select PGA settings for input pins connection,  $V_{CM}$  option by PGAC1 register.
- Step 4  
Select the required A/D conversion clock 4.9152MHz by correctly programming bits ADCK4~ADCK0 in the ADCS register.
- Step 5  
Select output data rate.
- Step 6  
Select which channel is to be connected to the internal PGA by correctly programming the CHSP2~CHSP0 and CHSN2~CHSN0 bits which are also contained in the PGACS register.
- Step 7  
Release power down mode and sleep mode by ADOFF and ADSLP bits in ADCR0 register.
- Step 8  
Reset the A/D by setting the ADRST to high in the ADCR0 register and clearing this bit to zero to release reset status.
- Step 9  
If the interrupts are to be used, the interrupt control registers must be correctly configured to ensure the A/D converter interrupt function is active. The master interrupt control bit, EMI, and the A/D converter interrupt bit, ADE, must both be set high to do this.
- Step 10  
To check when the analog to digital conversion process is complete, the EOC bit in the ADCR1 register can be polled. The conversion process is complete when this bit goes low. When this occurs the A/D data registers ADRL, ADRM and ADRH can be read to obtain the conversion value. As an alternative method, if the interrupts are enabled and the stack is not full, the program can wait for an A/D interrupt to occur.

Note: When checking for the end of the conversion process, if the method of polling the EOC bit in the ADCR1 register is used, the interrupt enable step above can be omitted.

### Programming Considerations

During microcontroller operations where the A/D converter is not being used, the A/D internal circuitry can be switched off to reduce power consumption, by setting bit ADOFF high in the ADCR0 register. When this happens, the internal A/D converter circuits will not consume power irrespective of what analog voltage is applied to their input lines.

### A/D Transfer Function

Each device contains a 24-bit Delta Sigma A/D converter, its full-scale converted digitised value is from 8388607 to -8388608 in decimal value. The converted data format is formed by a two's complement binary value. The MSB of the converted data is the signed bit. Since the full-scale analog input value is equal to the  $V_{CM}$  or  $\Delta V_{REF}$  voltage, selected by the VREFS bit in ADCR0 register, this gives a single bit analog input value of  $V_{CM}$  or  $\Delta V_{REF}$  divided by 8388608.

$$1 \text{ LSB} = (V_{CM} \text{ or } \Delta V_{REF}) / 8388608$$

The A/D Converter input voltage value can be calculated using the following equation:

$$\Delta SI\_I = (PGAGN \times ADGN \times \Delta DI_{\pm}) + (DCSET \times \Delta VR\_I)$$

$$\Delta VR\_I = VREGN \times \Delta VR_{\pm}$$

$$ADC\_Conversion\_Data = (\Delta SI\_I \div \Delta VR\_I) \times K$$

Where K is equal to  $2^{23}$

Note: The PGAGN, ADGN, VREGN values are decided by PGS, AGS, VGS control bits.

$\Delta SI\_I$ : Differential Input Signal after process

PGAGN: Programmable Gain Amplifier gain

ADGN: ADC gain

$\Delta DI_{\pm}$ : Differential Input signal

DCSET: Offset voltage

$\Delta VR_{\pm}$ : Differential Reference voltage

$\Delta VR\_I$ : Differential Reference input voltage after process

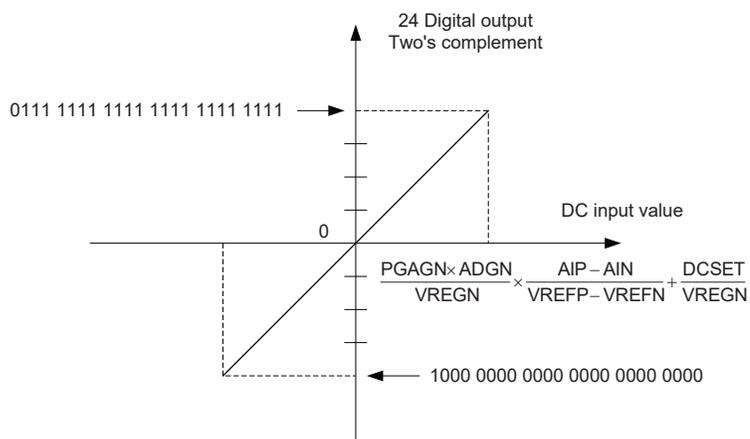
VREGN: Reference voltage gain

Due to the digital system design of the Delta Sigma ADC, the maximum number of the ADC converted value is 8388607 and the minimum value is -8388608, therefore, we can have the middle number 0. The ADC\_Conversion\_Data equation illustrates this range of converted data variation.

A/D conversion data (2's compliment, Hexadecimal)	Decimal Value
0x7FFFFFFF	8388607
0x800000	-8388608

The above ADC conversion data table illustrates the range of ADC conversion data.

The following diagram shows the relationship between the DC input value and the ADC converted data which is presented by the Two's Complement.



### A/D Converted Data

The ADC converted data is related to the input voltage and the PGA selections. The format of the ADC output is a two's complement binary code. The length of this output code is 24 bits and the MSB is a signed bit. When the MSB is "0", which represents the input is "positive", on the other hand, as the MSB is "1", it represents the input is "negative". The maximum value is 8388607 and the minimum value is -8388608. If the input signal is over the maximum value, the converted data is limited by the 8388607, and if the input signal is less than the minimum value, the converted data is limited by -8388608.

### A/D Converted data to voltage

The designer can recover the converted data by the following equations:

If MSB=0 (Positive Converted data):

$$\text{Input Voltage} = (\text{Converted data}-0) \times (\text{LSB}/\text{PGA})$$

If the MSB=1(Negative Converted data):

$$\text{Input voltage} = (\text{Two's complement of converted data}-0) \times (\text{LSB}/\text{PGA})$$

Note: Two's complement = One's complement + 1

## A/D Programming Example

### Example: Using an EOC polling method to detect the end of conversion

```

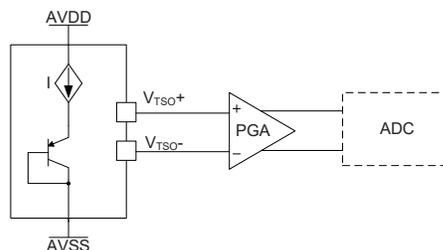
#include ht67f5660.inc
data .section 'data'
    adc_result_data_l db ?
    adc_result_data_m db ?
    adc_result_data_h db ?
code .section 'code'
start:
    clr     ADE                ; disable ADC interrupt
    mov     a, 0C3H            ; Power control for PGA, ADC
    mov     PWRC, a           ; PWRC=11000011, LDO enable, VCM enable, LDO Bypass disable,
                                ; LDO output voltage: 3.3V

    mov     a, 000H
    mov     PGACO, a          ; PGA gain=1, ADC gain=1, VREF gain=1
    mov     a, 080H
    mov     PGACL, a          ; VCM=1.25V, INIS, INX, DCSET in default value
    clr     VRBUF             ; disable buffer for VREF+
    clr     VRBUFN            ; disable buffer for VREF-
    set     VREFS             ; for using external reference
    clr     ADOR2             ; for 10Hz output data rate, ADOR[2:0]=001, FLMS[2:0]=000
    clr     ADOR1
    set     ADOR0
    clr     FLMS2
    clr     FLMS1
    clr     FLMS0
    clr     ADOFF             ; ADC exit power down mode.
    set     ADRST             ; ADC in reset mode
    clr     ADRST             ; ADC in conversion (continuous mode)
    clr     EOC               ; Clear "EOC" flag
loop:
    snz     EOC               ; Polling "EOC" flag
    jmp     loop              ; Wait for read data
    clr     adc_result_data_h
    clr     adc_result_data_m
    clr     adc_result_data_l
    set     ADCDL             ; enable data latch
    mov     a, ADRL
    mov     adc_result_data_l, a ; Get Low byte ADC value
    mov     a, ADRM
    mov     adc_result_data_m, a ; Get Middle byte ADC value
    mov     a, ADRH
    mov     adc_result_data_h, a ; Get High byte ADC value
get_adc_value_ok:
    clr     ADCDL             ; disable data latch
    clr     EOC               ; Clearing read flag
    jmp     loop              ; for next data read
end

```

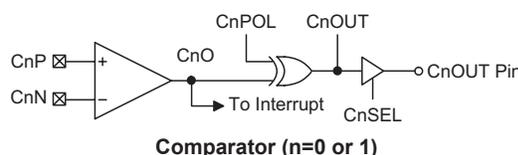
## Temperature sensor

Each device provides an internal temperature sensor to compensate the device performance. By selecting the PGA input channels to VTSO+ and VTSO-, the ADC can get the temperature information and the designer can do some compensation to the A/D converted data. The following block diagram illustrates the functional operation for the temperature sensor.



## Comparators

Two independent analog comparators are contained within these devices. These functions offer flexibility via its register controlled features such as power-down, polarity select, hysteresis etc. In sharing its pins with normal I/O pins the comparator does not waste precious I/O pins if there functions are otherwise unused.



### Comparator Operation

Each device contains two comparator functions which are used to compare two analog voltages and provide an output based on their difference. Full control over the internal comparators is provided via two control registers, CP0C and CP1C, one assigned to each comparator. The comparator output is recorded via a bit in their respective control register, but can also be transferred out onto a shared I/O pin. Additional comparator functions include, output polarity, hysteresis functions and power down control. Any pull-high resistors connected to the shared comparator input pins will be automatically disconnected when the comparator is enabled. As the comparator inputs approach their switching level, some spurious output signals may be generated on the comparator output due to the slow rising or falling nature of the input signals. This can be minimised by selecting the hysteresis function will apply a small amount of positive feedback to the comparator. Ideally the comparator should switch at the point where the positive and negative inputs signals are at the same voltage level; however, unavoidable input offsets introduce some uncertainties here. The hysteresis function, if enabled, also increases the switching offset value.

### Comparator Register

There are two registers for overall comparator operation, one for each comparator. As corresponding bits in the two registers have identical functions, they following register table applies to both registers.

Register Name	Bit							
	7	6	5	4	3	2	1	0
CP0C	C0SEL	C0EN	C0POL	C0OUT	C0OS	—	—	C0HYEN
CP1C	C1SEL	C1EN	C1POL	C1OUT	C1OS	—	—	C1HYEN

**Comparator Registers List**

**CP0C Register**

Bit	7	6	5	4	3	2	1	0
Name	C0SEL	C0EN	C0POL	C0OUT	C0OS	—	—	C0HYEN
R/W	R/W	R/W	R/W	R	R/W	—	—	R/W
POR	1	0	0	0	0	—	—	1

- Bit 7 C0SEL:** Select Comparator pins or I/O pins  
 0: I/O pin select  
 1: Comparator pin select  
 This is the Comparator pin or I/O pin select bit. If the bit is high the comparator will be selected and the two comparator input pins will be enabled. As a result, these two pins will lose their I/O pin functions. Any pull-high configuration options associated with the comparator shared pins will also be automatically disconnected.
- Bit 6 C0EN:** Comparator On/Off control  
 0: Off  
 1: On  
 This is the Comparator on/off control bit. If the bit is zero the comparator will be switched off and no power consumed even if analog voltages are applied to its inputs. For power sensitive applications this bit should be cleared to zero if the comparator is not used or before the device enters the SLEEP or IDLE mode.
- Bit 5 C0POL:** Comparator output polarity  
 0: Output not inverted  
 1: Output inverted  
 This is the comparator polarity bit. If the bit is zero then the C0OUT bit will reflect the non-inverted output condition of the comparator. If the bit is high the comparator C0OUT bit will be inverted.
- Bit 4 C0OUT:** Comparator output bit  
 C0POL=0  
 0: C0P < C0N  
 1: C0P > C0N  
 C0POL=1  
 0: C0P > C0N  
 1: C0P < C0N  
 This bit stores the comparator output bit. The polarity of the bit is determined by the voltages on the comparator inputs and by the condition of the C0POL bit.
- Bit 3 C0OS:** Output path select  
 0: C0OUT pin  
 1: Internal use  
 This is the comparator output path select control bit. If the bit is cleared to zero and the C0SEL bit is 1 the comparator output is connected to an external C0OUT pin. If the bit is set high or the C0SEL bit is 0 the comparator output signal is only used internally by the device allowing the shared comparator output pin to retain its normal I/O operation.
- Bit 2~1** Unimplemented, read as "0"
- Bit 0 C0HYEN:** Hysteresis Control  
 0: Off  
 1: On  
 This is the hysteresis control bit and if set high will apply a limited amount of hysteresis to the comparator, as specified in the Comparator Electrical Characteristics table. The positive feedback induced by hysteresis reduces the effect of spurious switching near the comparator threshold.

**CP1C Register**

Bit	7	6	5	4	3	2	1	0
Name	C1SEL	C1EN	C1POL	C1OUT	C1OS	—	—	C1HYEN
R/W	R/W	R/W	R/W	R	R/W	—	—	R/W
POR	1	0	0	0	0	—	—	1

- Bit 7**     **C1SEL:** Select Comparator pins or I/O pins  
0: I/O pin select  
1: Comparator pin select  
This is the Comparator pin or I/O pin select bit. If the bit is high the comparator will be selected and the two comparator input pins will be enabled. As a result, these two pins will lose their I/O pin functions. Any pull-high configuration options associated with the comparator shared pins will also be automatically disconnected.
- Bit 6**     **C1EN:** Comparator On/Off control  
0: Off  
1: On  
This is the Comparator on/off control bit. If the bit is zero the comparator will be switched off and no power consumed even if analog voltages are applied to its inputs. For power sensitive applications this bit should be cleared to zero if the comparator is not used or before the device enters the SLEEP or IDLE mode.
- Bit 5**     **C1POL:** Comparator output polarity  
0: output not inverted  
1: output inverted  
This is the comparator polarity bit. If the bit is zero then the C1OUT bit will reflect the non-inverted output condition of the comparator. If the bit is high the comparator C1OUT bit will be inverted.
- Bit 4**     **C1OUT:** Comparator output bit  
C1POL=0  
0: C1P < C1N  
1: C1P > C1N  
C1POL=1  
0: C1P > C1N  
1: C1P < C1N  
This bit stores the comparator output bit. The polarity of the bit is determined by the voltages on the comparator inputs and by the condition of the C1POL bit.
- Bit 3**     **C1OS:** Output path select  
0: C1OUT pin  
1: Internal use  
This is the comparator output path select control bit. If the bit is cleared to zero and the C1SEL bit is 1 the comparator output is connected to an external C1OUT pin. If the bit is set high or the C1SEL bit is 0 the comparator output signal is only used internally by the device allowing the shared comparator output pin to retain its normal I/O operation.
- Bit 2~1**    Unimplemented, read as "0"
- Bit 0**     **C1HYEN:** Hysteresis Control  
0: Off  
1: On  
This is the hysteresis control bit and if set high will apply a limited amount of hysteresis to the comparator, as specified in the Comparator Electrical Characteristics table. The positive feedback induced by hysteresis reduces the effect of spurious switching near the comparator threshold.

### **Comparator Interrupt**

Each also possesses its own interrupt function. When any one of the changes state, its relevant interrupt flag will be set, and if the corresponding interrupt enable bit is set, then a jump to its relevant interrupt vector will be executed. Note that it is the changing state of the CnOUT bit and generates an interrupt. If the microcontroller is in the SLEEP or IDLE Mode and the Comparator is enabled, then if the external input lines cause the Comparator output to change state, the resulting generated interrupt flag will also generate a wake-up. If it is required to disable a wake-up from occurring, then the interrupt flag should be first set high before entering the SLEEP or IDLE Mode.

### **Programming Considerations**

If the comparator is enabled, it will remain active when the microcontroller enters the SLEEP or IDLE Mode, however as it will consume a certain amount of power, the user may wish to consider disabling it before the SLEEP or IDLE Mode is entered.

As comparator pins are shared with normal I/O pins, the I/O registers for these pins will be read as zero (port control register is "1") or read as port data register value (port control register is "0") if the comparator function is enabled.

## Serial Interface Module – SIM

Each device contains a Serial Interface Module, which includes both the four line SPI interface and the two line I<sup>2</sup>C interface types, to allow an easy method of communication with external peripheral hardware. Having relatively simple communication protocols, these serial interface types allow the microcontroller to interface to external SPI or I<sup>2</sup>C based hardware such as sensors, Flash memory, etc. As both interface types share the same pins and registers, the choice of whether the SPI or I<sup>2</sup>C type is used is made using the SIM operating mode control bits, named SIM2~SIM0, in the SIMC0 register. These pull-high resistors of the SIM pin-shared I/O pins are selected using pull-high control registers when the SIM function is enabled and the corresponding pins are used as SIM input pins.

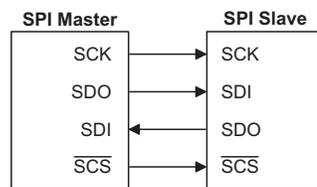
### SPI Interface

The SPI interface is often used to communicate with external peripheral devices such as sensors, Flash memory devices etc. Originally developed by Motorola, the four line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

The communication is full duplex and operates as a slave/master type, where the device can be either master or slave. Although the SPI interface specification can control multiple slave devices from a single master, but this device is provided only one  $\overline{SCS}$  pin. If the master needs to control multiple slave devices from a single master, the master can use I/O pin to select the slave devices.

### SPI Interface Operation

The SPI interface is a full duplex synchronous serial data link. It is a four line interface with pin names SDI, SDO, SCK and  $\overline{SCS}$ . Pins SDI and SDO are the Serial Data Input and Serial Data Output lines; SCK is the Serial Clock line and  $\overline{SCS}$  is the Slave Select line. As the SPI interface pins are pin-shared with normal I/O pins and with the I<sup>2</sup>C function pins, the SPI interface must first be enabled by setting the correct bits in the SIMC0 and SIMC2 registers. The SPI can be disabled or enabled using the SIMEN bit in the SIMC0 register. Communication between devices connected to the SPI interface is carried out in a slave/master mode with all data transfer initiations being implemented by the master. The Master also controls the clock signal. As each device only contains a single  $\overline{SCS}$  pin only one slave device can be utilized. The  $\overline{SCS}$  pin is controlled by software, set CSEN bit to "1" to enable  $\overline{SCS}$  pin function, set CSEN bit to "0" the  $\overline{SCS}$  pin will be floating state.

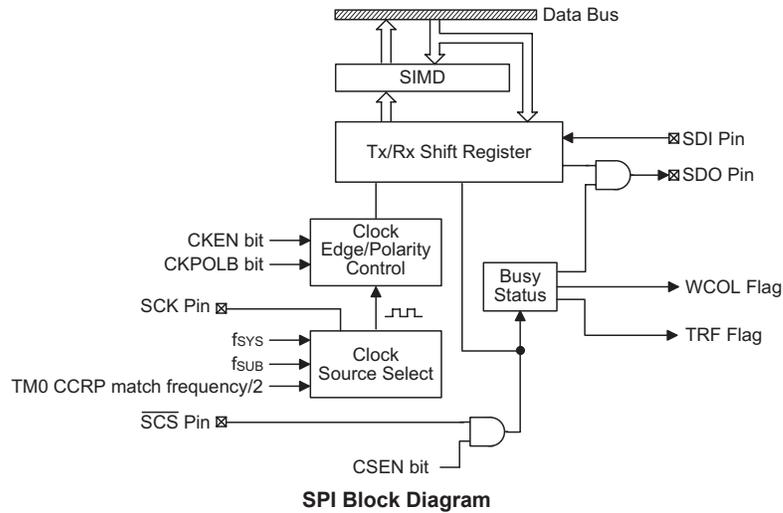


SPI Master/Slave Connection

The SPI function in these devices offers the following features:

- Full duplex synchronous data transfer
- Both Master and Slave modes
- LSB first or MSB first data transmission modes
- Transmission complete flag
- Rising or falling active clock edge

The status of the SPI interface pins is determined by a number of factors such as whether these devices are in the master or slave mode and upon the condition of certain control bits such as CSEN and SIMEN.



### SPI Registers

There are three internal registers which control the overall operation of the SPI interface. These are the SIMD data register and two registers SIMC0 and SIMC2. Note that the SIMC1 register is only used by the I<sup>2</sup>C interface.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	—	SIMDBNC1	SIMDBNC0	SIMEN	SIMICF
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMC2	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF

**SIM Registers List**

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I<sup>2</sup>C functions. Before these devices write data to the SPI bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the SPI bus, these devices can read it from the SIMD register. Any transmission or reception of data from the SPI bus must be made via the SIMD register.

#### • SIMD Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

There are also two control registers for the SPI interface, SIMC0 and SIMC2. Note that the SIMC2 register also has the name SIMA which is used by the I<sup>2</sup>C function. The SIMC1 register is not used by the SPI function, only by the I<sup>2</sup>C function. Register SIMC0 is used to control the enable/disable function and to set the data transmission clock frequency. Although not connected with the SPI function, the SIMC0 register is also used to control the Peripheral Clock Prescaler. Register SIMC2 is used for other control functions such as LSB/MSB selection, write collision flag etc.

• SIMC0 Register

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	—	SIMDBNC1	SIMDBNC0	SIMEN	SIMICF
R/W	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W
POR	1	1	1	—	0	0	0	0

Bit 7~5 **SIM2~SIM0**: SIM Operating Mode Control  
 000: SPI master mode; SPI clock is  $f_{SYS}/4$   
 001: SPI master mode; SPI clock is  $f_{SYS}/16$   
 010: SPI master mode; SPI clock is  $f_{SYS}/64$   
 011: SPI master mode; SPI clock is  $f_{SUB}$   
 100: SPI master mode; SPI clock is TM0 CCRP match frequency/2  
 101: SPI slave mode  
 110: I<sup>2</sup>C slave mode  
 111: Unused mode

These bits setup the overall operating mode of the SIM function. As well as selecting if the I<sup>2</sup>C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from  $f_{SUB}$  or the TM0. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4 Unimplemented, read as "0"

Bit 3~2 **SIMDBNC1~SIMDBNC0**: I<sup>2</sup>C Debounce Time Selection  
 00: No debounce  
 01: 2 system clock debounce  
 1x: 4 system clock debounce

Bit 1 **SIMEN**: SIM Control  
 0: Disable  
 1: Enable

The bit is the overall on/off control for the SIM interface. When the  $\overline{SIMEN}$  bit is cleared to zero to disable the SIM interface, the SDI, SDO, SCK and  $\overline{SCS}$ , or SDA and SCL lines will be in a floating condition and the SIM operating current will be reduced to a minimum value. When the bit is high the SIM interface is enabled. The SIM configuration option must have first enabled the SIM interface for this bit to be effective. If the SIM is configured to operate as an SPI interface via the SIM2~SIM0 bits, the contents of the SPI control registers will remain at the previous settings when the  $\overline{SIMEN}$  bit changes from low to high and should therefore be first initialised by the application program. If the SIM is configured to operate as an I<sup>2</sup>C interface via the SIM2~SIM0 bits and the  $\overline{SIMEN}$  bit changes from low to high, the contents of the I<sup>2</sup>C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialised by the application program while the relevant I<sup>2</sup>C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0 **SIMICF**: SIM Incompleted Flag  
 0: SIM incompleted is not occurred  
 1: SIM incompleted is occurred

The SIMICF bit is determined by  $\overline{SCS}$  pin. When  $\overline{SCS}$  pin is set high, it will clear the SPI counter. Meanwhile, the interrupt is occurred and the incompleted flag, SIMICF, is set high.

• **SIMC2 Register**

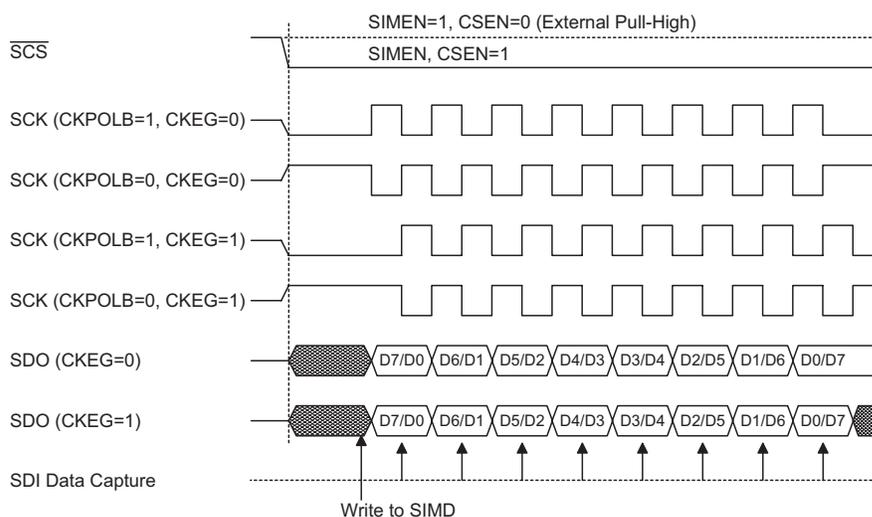
Bit	7	6	5	4	3	2	1	0
Name	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7~6 D7~D6:** Undefined bit  
This bit can be read or written by user software program.
- Bit 5 CKPOLB:** Determines the base condition of the clock line  
0: The SCK line will be high when the clock is inactive  
1: The SCK line will be low when the clock is inactive  
The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive.
- Bit 4 CKEG:** Determines SPI SCK active clock edge type  
CKPOLB=0  
0: SCK is high base level and data capture at SCK rising edge  
1: SCK is high base level and data capture at SCK falling edge  
CKPOLB=1  
0: SCK is low base level and data capture at SCK falling edge  
1: SCK is low base level and data capture at SCK rising edge  
The CKEG and CKPOLB bits are used to setup the way that the clock signal outputs and inputs data on the SPI bus. These two bits must be configured before data transfer is executed otherwise an erroneous clock edge may be generated. The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive. The CKEG bit determines active clock edge type which depends upon the condition of CKPOLB bit.
- Bit 3 MLS:** SPI Data shift order  
0: LSB  
1: MSB  
This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.
- Bit 2 CSEN:** SPI  $\overline{SCS}$  pin Control  
0: Disable  
1: Enable  
The CSEN bit is used as an enable/disable for the  $\overline{SCS}$  pin. If this bit is low, then the  $\overline{SCS}$  pin will be disabled and placed into a floating condition. If the bit is high the  $\overline{SCS}$  pin will be enabled and used as a select pin.  
Note that using the CSEN bit can be disabled or enabled via configuration option.
- Bit 1 WCOL:** SPI Write Collision flag  
0: No collision  
1: Collision  
The WCOL flag is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SIMD register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program. Note that using the WCOL bit can be disabled or enabled via configuration option.
- Bit 0 TRF:** SPI Transmit/Receive Complete flag  
0: Data is being transferred  
1: SPI data transmission is completed  
The TRF bit is the Transmit/Receive Complete flag and is set high automatically when an SPI data transmission is completed, but must be cleared to zero by the application program. It can be used to generate an interrupt.

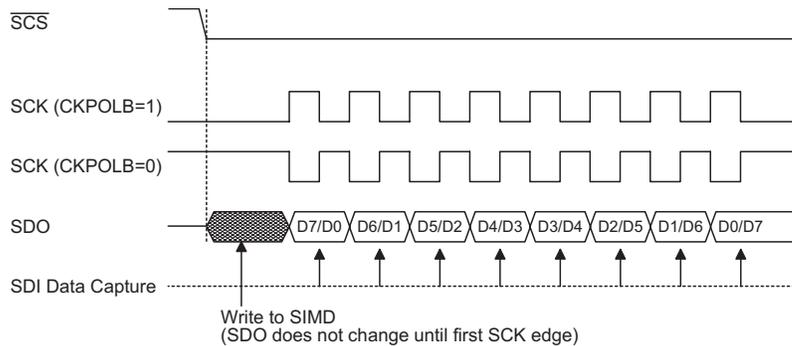
### SPI Communication

After the SPI interface is enabled by setting the SIMEN bit high, then in the Master Mode, when data is written to the SIMD register, transmission/reception will begin simultaneously. When the data transfer is complete, the TRF flag will be set automatically, but must be cleared using the application program. In the Slave Mode, when the clock signal from the master has been received, any data in the SIMD register will be transmitted and any data on the SDI pin will be shifted into the SIMD register. The master should output an  $\overline{SCS}$  signal to enable the slave device before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the  $\overline{SCS}$  signal depending upon the configurations of the CKPOLB bit and CKEG bit. The accompanying timing diagram shows the relationship between the slave data and  $\overline{SCS}$  signal for various configurations of the CKPOLB and CKEG bits.

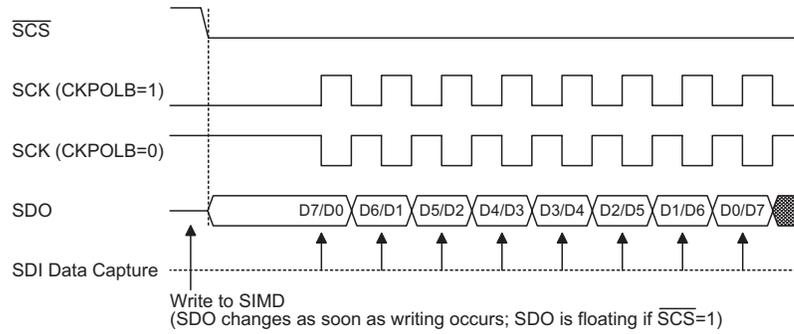
The SPI will continue to function even in the IDLE Mode.



**SPI Master Mode Timing**

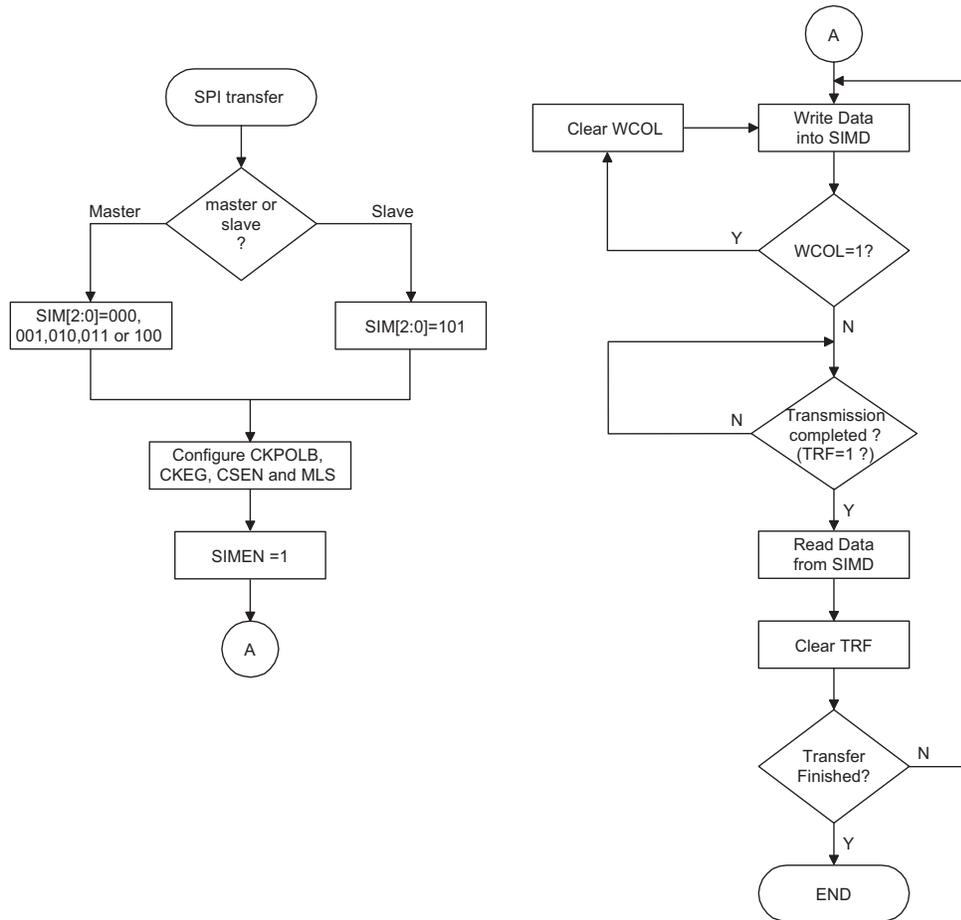


**SPI Slave Mode Timing – CKEG=0**



Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always enabled and ignores the  $\overline{SCS}$  level.

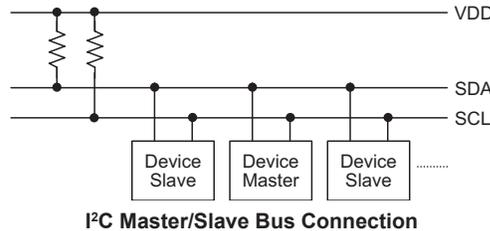
**SPI Slave Mode Timing – CKEG=1**



**SPI Transfer Control Flowchart**

## I<sup>2</sup>C Interface

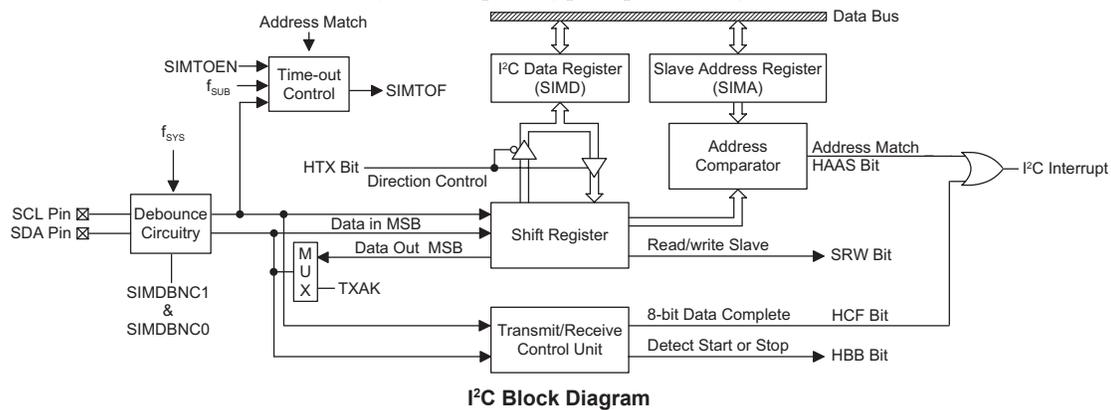
The I<sup>2</sup>C interface is used to communicate with external peripheral devices such as sensors etc. Originally developed by Philips, it is a two line low speed serial interface for synchronous serial data transfer. The advantage of only two lines for communication, relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.

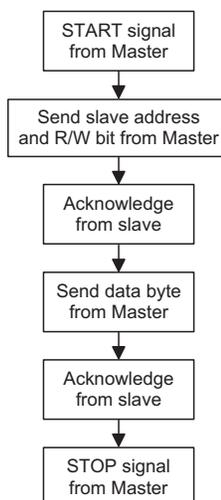


### I<sup>2</sup>C Interface Operation

The I<sup>2</sup>C serial interface is a two line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I<sup>2</sup>C bus is identified by a unique address which will be transmitted and received on the I<sup>2</sup>C bus.

When two devices communicate with each other on the bidirectional I<sup>2</sup>C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data; however, it is the master device that has overall control of the bus. For these devices, which only operate in slave mode, there are two methods of transferring data on the I<sup>2</sup>C bus, the slave transmit mode and the slave receive mode. The pull-up control function pin-shared with SCL/SDA pin is still applicable even if I<sup>2</sup>C device is activated and the related internal pull-up register could be controlled by its corresponding pull-up control register.





### I<sup>2</sup>C Registers

There are three control registers associated with the I<sup>2</sup>C bus, SIMC0, SIMC1 and SIMTOC, one address register, SIMA and one data register, SIMD. The SIMD register, which is shown in the above SPI section, is used to store the data being transmitted and received on the I<sup>2</sup>C bus. Before the microcontroller writes data to the I<sup>2</sup>C bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the I<sup>2</sup>C bus, the microcontroller can read it from the SIMD register. Any transmission or reception of data from the I<sup>2</sup>C bus must be made via the SIMD register. Note that the SIMA register also has the name SIMC2 which is used by the SPI function. Bit SIMEN and bits SIM2~SIM0 in register SIMC0 are used by the I<sup>2</sup>C interface. The SIMTOC register is used for I<sup>2</sup>C time-out control.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	—	SIMDBNC1	SIMDBNC0	SIMEN	SIMICF
SIMC1	HCF	HAAS	HBB	HTX	TXAK	SRW	RNIC	RXAK
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMA	IICA6	IICA5	IICA4	IICA3	IICA2	IICA1	IICA0	D0
SIMTOC	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0

**I<sup>2</sup>C Registers List**

• SIMC0 Register

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	—	SIMDBNC1	SIMDBNC0	SIMEN	SIMICF
R/W	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W
POR	1	1	1	—	0	0	0	0

Bit 7~5 **SIM2~SIM0**: SIM Operating Mode Control  
 000: SPI master mode; SPI clock is  $f_{SYS}/4$   
 001: SPI master mode; SPI clock is  $f_{SYS}/16$   
 010: SPI master mode; SPI clock is  $f_{SYS}/64$   
 011: SPI master mode; SPI clock is  $f_{SUB}$   
 100: SPI master mode; SPI clock is TM0 CCRP match frequency/2  
 101: SPI slave mode  
 110: I<sup>2</sup>C slave mode  
 111: Unused mode

These bits setup the overall operating mode of the SIM function. As well as selecting if the I<sup>2</sup>C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from  $f_{SUB}$  or the TM0. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4 Unimplemented, read as "0"

Bit 3~2 **SIMDBNC1~SIMDBNC0**: I<sup>2</sup>C Debounce Time Selection  
 00: No debounce  
 01: 2 system clock debounce  
 1x: 4 system clock debounce

Bit 1 **SIMEN**: SIM Control  
 0: Disable  
 1: Enable

The bit is the overall on/off control for the SIM interface. When the SIMEN bit is cleared to zero to disable the SIM interface, the SDI, SDO, SCK and  $\overline{SCS}$ , or SDA and SCL lines will be in a floating condition and the SIM operating current will be reduced to a minimum value. When the bit is high the SIM interface is enabled. The SIM configuration option must have first enabled the SIM interface for this bit to be effective. If the SIM is configured to operate as an SPI interface via the SIM2~SIM0 bits, the contents of the SPI control registers will remain at the previous settings when the SIMEN bit changes from low to high and should therefore be first initialised by the application program. If the SIM is configured to operate as an I<sup>2</sup>C interface via the SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I<sup>2</sup>C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialised by the application program while the relevant I<sup>2</sup>C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0 **SIMICF**: SIM Incompleted Flag  
 SIMICF is of no used in I<sup>2</sup>C mode of SIM, please ignore this flag when operate in I<sup>2</sup>C mode.

• **SIMC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	HCF	HAAS	HBB	HTX	TXAK	SRW	RNIC	RXAK
R/W	R	R	R	R/W	R/W	R	R/W	R
POR	1	0	0	0	0	0	0	1

- Bit 7 HCF:** I<sup>2</sup>C Bus data transfer completion flag  
 0: Data is being transferred  
 1: Completion of an 8-bit data transfer  
 The HCF flag is the data transfer flag. This flag will be zero when data is being transferred. Upon completion of an 8-bit data transfer the flag will go high and an interrupt will be generated.
- Bit 6 HAAS:** I<sup>2</sup>C Bus address match flag  
 0: Not address match  
 1: Address match  
 The HAAS flag is the address match flag. This flag is used to determine if the slave device address is the same as the master transmit address. If the addresses match then this bit will be high, if there is no match then the flag will be low.
- Bit 5 HBB:** I<sup>2</sup>C Bus busy flag  
 0: I<sup>2</sup>C Bus is not busy  
 1: I<sup>2</sup>C Bus is busy  
 The HBB flag is the I<sup>2</sup>C busy flag. This flag will be "1" when the I<sup>2</sup>C bus is busy which will occur when a START signal is detected. The flag will be cleared to zero when the bus is free which will occur when a STOP signal is detected.
- Bit 4 HTX:** Select I<sup>2</sup>C slave device is transmitter or receiver  
 0: Slave device is the receiver  
 1: Slave device is the transmitter
- Bit 3 TXAK:** I<sup>2</sup>C Bus transmit acknowledge flag  
 0: Slave send acknowledge flag  
 1: Slave do not send acknowledge flag  
 The TXAK bit is the transmit acknowledge flag. After the slave device receipt of 8-bits of data, this bit will be transmitted to the bus on the 9th clock from the slave device. The slave device must always set TXAK bit to "0" before further data is received.
- Bit 2 SRW:** I<sup>2</sup>C Slave Read/Write flag  
 0: Slave device should be in receive mode  
 1: Slave device should be in transmit mode  
 The SRW flag is the I<sup>2</sup>C Slave Read/Write flag. This flag determines whether the master device wishes to transmit or receive data from the I<sup>2</sup>C bus. When the transmitted address and slave address is match, that is when the HAAS flag is set high, the slave device will check the SRW flag to determine whether it should be in transmit mode or receive mode. If the SRW flag is high, the master is requesting to read data from the bus, so the slave device should be in transmit mode. When the SRW flag is zero, the master will write data to the bus, therefore the slave device should be in receive mode to read this data.
- Bit 1 RNIC:** I<sup>2</sup>C Running Not using Internal Clock.  
 0: I<sup>2</sup>C running using internal clock.  
 1: I<sup>2</sup>C running NOT using internal clock.  
 The I<sup>2</sup>C module can run without using internal clock, and generate an interrupt if the SIM interrupt is enabled, which can be used in sleep mode, idle (slow) mode and normal (slow) mode.  
 Note: If RNIC=1 and MCU is in halt, slave-receiver can work well but slave-transmitter doesn't work since it needs system clock.
- Bit 0 RXAK:** I<sup>2</sup>C Bus Receive acknowledge flag  
 0: Slave receives acknowledge flag  
 1: Slave does not receive acknowledge flag

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I<sup>2</sup>C bus. Before these devices write data to the I<sup>2</sup>C bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the I<sup>2</sup>C bus, these devices can read it from the SIMD register. Any transmission or reception of data from the I<sup>2</sup>C bus must be made via the SIMD register.

• **SIMD Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

• **SIMA Register**

Bit	7	6	5	4	3	2	1	0
Name	IICA6	IICA5	IICA4	IICA3	IICA2	IICA1	IICA0	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1 **IICA6~IICA0**: I<sup>2</sup>C slave address

IICA6~ IICA0 is the I<sup>2</sup>C slave address bit 6 ~ bit 0.

The SIMA register is also used by the SPI interface but has the name SIMC2. The SIMA register is the location where the 7-bit slave address of the slave device is stored. Bits 7~ 1 of the SIMA register define the device slave address. Bit 0 is not defined.

When a master device, which is connected to the I<sup>2</sup>C bus, sends out an address, which matches the slave address in the SIMA register, the slave device will be selected. Note that the SIMA register is the same register address as SIMC2 which is used by the SPI interface.

Bit 0 Undefined bit

This bit can be read or written by user software program.

• **SIMTOC Register**

Bit	7	6	5	4	3	2	1	0
Name	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SIMTOEN**: I<sup>2</sup>C interface Time-out control

0: Disable  
 1: Enable

Bit 6 **SIMTOF**: I<sup>2</sup>C interface Time-out flag

0: No occurred  
 1: Occurred

The SIMTOF flag is set by the time-out circuitry when the time-out event occurs and cleared by software program.

Bit 5~0 **SIMTOS5~SIMTOS0**: I<sup>2</sup>C interface Time-out period selection

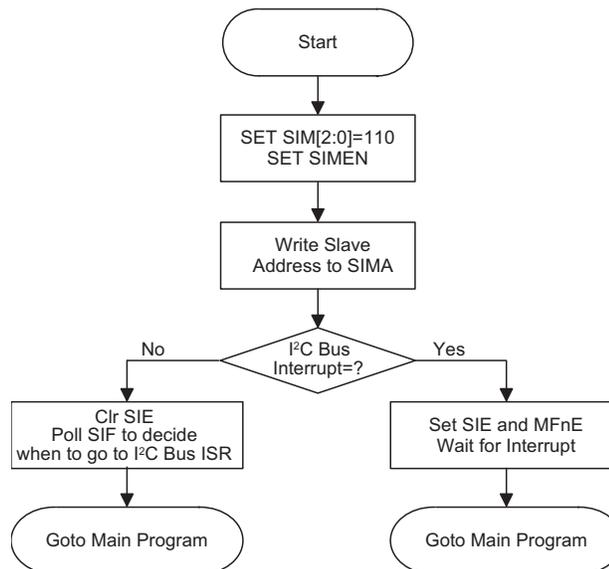
The I<sup>2</sup>C Time-Out clock source is  $f_{SUB}/32$ .

The I<sup>2</sup>C Time-Out time is  $([SIMTOS5:SIMTOS0] + 1) \times (32/f_{SUB})$

### I<sup>2</sup>C Bus Communication

Communication on the I<sup>2</sup>C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I<sup>2</sup>C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the bus. The first seven bits of the data will be the slave address with the first bit being the MSB. If the address of the slave device matches that of the transmitted address, the HAAS bit in the SIMC1 register will be set and an I<sup>2</sup>C interrupt will be generated. After entering the interrupt service routine, the slave device must first check the condition of the HAAS bit to determine whether the interrupt source originates from an address match or from the completion of an 8-bit data transfer. During a data transfer, note that after the 7-bit slave address has been transmitted, the following bit, which is the 8th bit, is the read/write bit whose value will be placed in the SRW bit. This bit will be checked by the slave device to determine whether to go into transmit or receive mode. Before any transfer of data to or from the I<sup>2</sup>C bus, the microcontroller must initialise the bus, the following are steps to achieve this:

- Step 1  
Set the SIM2~SIM0 bits to "110" and the SIMEN bits to "1" in the SIMC0 register to enable the I<sup>2</sup>C bus.
- Step 2  
Write the slave address of these devices to the I<sup>2</sup>C bus address register SIMA.
- Step 3  
Set the SIE and SIM Multi-Function interrupt enable bit of the interrupt control register to enable the SIM interrupt and Multi-function interrupt.



**I<sup>2</sup>C Bus Initialisation Flow Chart**

### **I<sup>2</sup>C Bus Start Signal**

The START signal can only be generated by the master device connected to the I<sup>2</sup>C bus and not by the slave device. This START signal will be detected by all devices connected to the I<sup>2</sup>C bus. When detected, this indicates that the I<sup>2</sup>C bus is busy and therefore the HBB bit will be set. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.

### **Slave Address**

The transmission of a START signal by the master will be detected by all devices on the I<sup>2</sup>C bus. To determine which slave device the master wishes to communicate with, the address of the slave device will be sent out immediately following the START signal. All slave devices, after receiving this 7-bit address data, will compare it with their own 7-bit slave address. If the address sent out by the master matches the internal address of the microcontroller slave device, then an internal I<sup>2</sup>C bus interrupt signal will be generated. The next bit following the address, which is the 8th bit, defines the read/write status and will be saved to the SRW bit of the SIMC1 register. The slave device will then transmit an acknowledge bit, which is a low level, as the 9th bit. The slave device will also set the status flag HAAS when the addresses match.

As an I<sup>2</sup>C bus interrupt can come from two sources, when the program enters the interrupt subroutine, the HAAS bit should be examined to see whether the interrupt source has come from a matching slave address or from the completion of a data byte transfer. When a slave address is matched, these devices must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.

### **I<sup>2</sup>C Bus Read/Write Signal**

The SRW bit in the SIMC1 register defines whether the slave device wishes to read data from the I<sup>2</sup>C bus or write data to the I<sup>2</sup>C bus. The slave device should examine this bit to determine if it is to be a transmitter or a receiver. If the SRW flag is "1" then this indicates that the master device wishes to read data from the I<sup>2</sup>C bus, therefore the slave device must be setup to send data to the I<sup>2</sup>C bus as a transmitter. If the SRW flag is "0" then this indicates that the master wishes to send data to the I<sup>2</sup>C bus, therefore the slave device must be setup to read data from the I<sup>2</sup>C bus as a receiver.

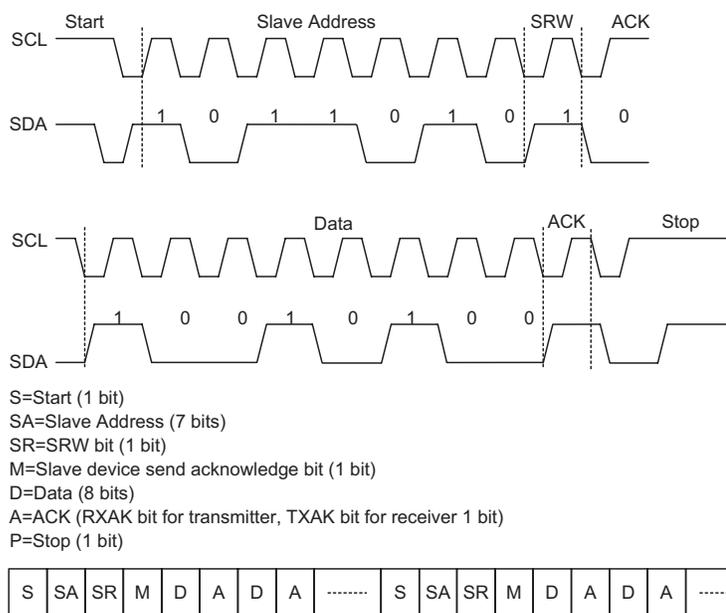
### **I<sup>2</sup>C Bus Slave Address Acknowledge Signal**

After the master has transmitted a calling address, any slave device on the I<sup>2</sup>C bus, whose own internal address matches the calling address, must generate an acknowledge signal. The acknowledge signal will inform the master that a slave device has accepted its calling address. If no acknowledge signal is received by the master then a STOP signal must be transmitted by the master to end the communication. When the HAAS flag is high, the addresses have matched and the slave device must check the SRW flag to determine if it is to be a transmitter or a receiver. If the SRW flag is high, the slave device should be setup to be a transmitter so the HTX bit in the SIMC1 register should be set high. If the SRW flag is low, then the microcontroller slave device should be setup as a receiver and the HTX bit in the SIMC1 register should be cleared to zero.

**I<sup>2</sup>C Bus Data and Acknowledge Signal**

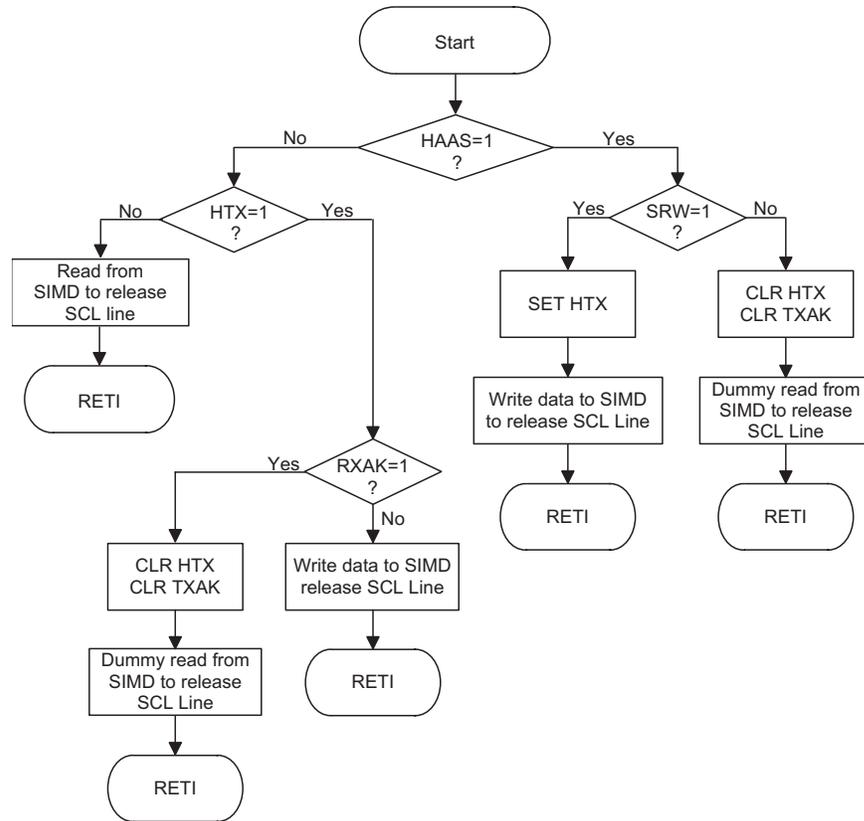
The transmitted data is 8-bits wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8-bits of data, the receiver must transmit an acknowledge signal, level "0", before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I<sup>2</sup>C Bus. The corresponding data will be stored in the SIMD register. If setup as a transmitter, the slave device must first write the data to be transmitted into the SIMD register. If setup as a receiver, the slave device must read the transmitted data from the SIMD register.

When the slave receiver receives the data byte, it must generate an acknowledge bit, known as TXAK, on the 9th clock. The slave device, which is setup as a transmitter will check the RXAK bit in the SIMC1 register to determine if it is to send another data byte, if not then it will release the SDA line and await the receipt of a STOP signal from the master.



**I<sup>2</sup>C Communication Timing Diagram**

Note: \*When a slave address is matched, these devices must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.



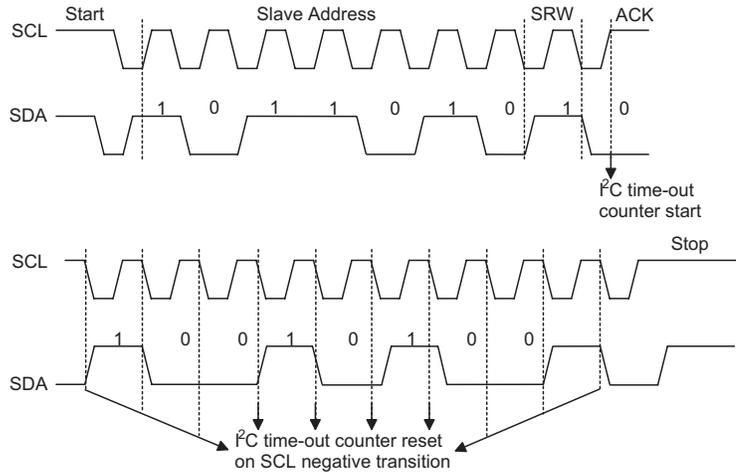
I<sup>2</sup>C Bus ISR Flow Chart

**I<sup>2</sup>C Time Out function**

In order to reduce the I<sup>2</sup>C lockup problem due to reception of erroneous clock sources, a time-out function is provided. If the clock source connected to the I<sup>2</sup>C bus is not received for a while, then the I<sup>2</sup>C circuitry and the SIMC1 register will be reset, the SIMTOF bit in the SIMTOC register will be set high after a certain time-out period. The Time Out function enable/disable and the time-out period are managed by the SIMTOC register.

• **I<sup>2</sup>C Time Out operation**

The time-out counter starts to count on an I<sup>2</sup>C bus "START" & "address match" condition, and is cleared by an SCL falling edge. Before the next SCL falling edge arrives, if the time elapsed is greater than the time-out period specified by the SIMTOC register, then a time-out condition will occur. The time-out function will stop when an I<sup>2</sup>C "STOP" condition occurs. There are 64 time-out period selections which can be selected using the SIMTOS0~SIMTOS5 bits in the SIMTOC register.



**I<sup>2</sup>C Time-out Diagram**

When an I<sup>2</sup>C time-out counter overflow occurs, the counter will stop and the SIMTOEN bit will be cleared to zero and the SIMTOF bit will be set high to indicate that a time-out condition has occurred. When an I<sup>2</sup>C time-out occurs, the I<sup>2</sup>C internal circuitry will be reset and the registers will be reset into the following condition:

Register	After I <sup>2</sup> C Time-out
SIMD, SIMA, SIMC0	No change
SIMC1	Reset to POR condition

**I<sup>2</sup>C Registers after Time-out**

## **UART Module Serial Interface with IR Carrier**

### **UART Module Features**

- Full-duplex, Universal Asynchronous Receiver and Transmitter (UART) communication
- 8 or 9 bits character length
- Even, odd or no parity options
- One or two stop bits
- Baud rate generator with 8-bit prescaler
- Parity, framing, noise and overrun error detection
- Support for interrupt on address detect (last character bit=1)
- Transmitter and receiver enabled independently
- 2-byte Deep FIFO Receive Data Buffer
- Transmit and Receive Multiple Interrupt Generation Sources:
  - ♦ Transmitter Empty
  - ♦ Transmitter Idle
  - ♦ Receiver Full
  - ♦ Receiver Overrun
  - ♦ Address Mode Detect

### **UART Module Overview**

The embedded UART Module is full-duplex asynchronous serial communications UART interface that enables communication with external devices that contain a serial interface. The UART function has many features and can transmit and receive data serially by transferring a frame of data with eight or nine data bits per transmission as well as being able to detect errors when the data is overwritten or incorrectly framed. The UART function possesses its own internal interrupt which can be used to indicate when a reception occurs or when a transmission terminates.

### **UART External Pin Interfacing**

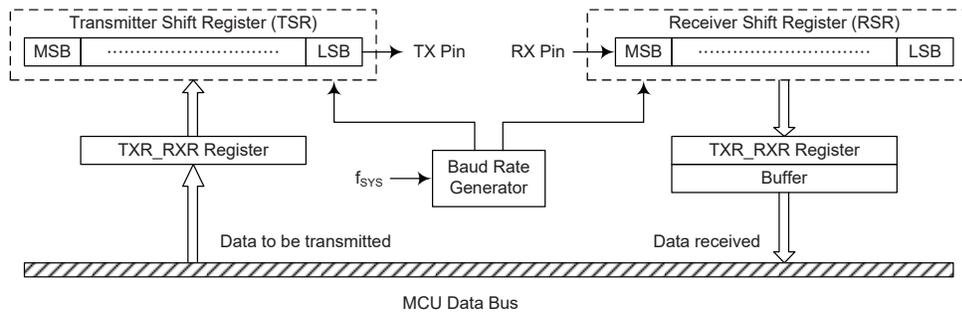
To communicate with an external serial interface, the internal UART has two external pins known as TX and RX. The TX pin is the UART transmitter pin, which can be used as a general purpose I/O or other pin-shared functional pin if the pin is not configured as a UART transmitter, which occurs when the TXEN bit in the UCR2 control register is equal to zero. Similarly, the RX pin is the UART receiver pin, which can also be used as a general purpose I/O or other pin-shared functional pin, if the pin is not configured as a receiver, which occurs if the RXEN bit in the UCR2 register is equal to zero. Along with the UARTEN bit, the TXEN and RXEN bits, if set, will automatically setup these I/O or other pin-shared functional pins to their respective TX output and RX input conditions and disable any pull-high resistor option which may exist on the RX pin.

### UART Data Transfer Scheme

The block diagram shows the overall data transfer structure arrangement for the UART. The actual data to be transmitted from the MCU is first transferred to the TXR\_RXR register by the application program. The data will then be transferred to the Transmit Shift Register from where it will be shifted out, LSB first, onto the TX pin at a rate controlled by the Baud Rate Generator. Only the TXR\_RXR register is mapped onto the MCU Data Memory, the Transmit Shift Register is not mapped and is therefore inaccessible to the application program.

Data to be received by the UART is accepted on the external RX pin, from where it is shifted in, LSB first, to the Receiver Shift Register at a rate controlled by the Baud Rate Generator. When the shift register is full, the data will then be transferred from the shift register to the internal TXR\_RXR register, where it is buffered and can be manipulated by the application program. Only the TXR\_RXR register is mapped onto the MCU Data Memory, the Receiver Shift Register is not mapped and is therefore inaccessible to the application program.

It should be noted that the actual register for data transmission and reception, although referred to in the text, only exists as a single shared register in the Data Memory. This shared register known as the TXR\_RXR register is used for both data transmission and data reception.



**UART Data Transfer Scheme**

### UART Status and Control Registers

There are five control registers associated with the UART function. The USR, UCR1 and UCR2 registers control the overall function of the UART, while the BRG register controls the Baud rate. The actual data to be transmitted and received on the serial interface is managed through the TXR\_RXR data register.

Register Name	Bit							
	7	6	5	4	3	2	1	0
USR	PERR	NF	FERR	OERR	RIDLE	RXIF	TIDLE	TXIF
UCR1	UARTEN	BNO	PREN	PRT	STOPS	TXBRK	RX8	TX8
UCR2	TXEN	RXEN	BRGH	ADDEN	WAKE	RIE	TIIE	TEIE
TXR_RXR	TXRX7	TXRX6	TXRX5	TXRX4	TXRX3	TXRX2	TXRX1	TXRX0
BRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0

**UART Register Summary**

### USR register

The USR register is the status register for the UART, which can be read by the program to determine the present status of the UART. All flags within the USR register are read only. Further explanation on each of the flags is given below:

Bit	7	6	5	4	3	2	1	0
Name	PERR	NF	FERR	OERR	RIDLE	RXIF	TIDLE	TXIF
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	1	0	1	1

- Bit 7 PERR:** Parity error flag  
 0: No parity error is detected  
 1: Parity error is detected  
 The PERR flag is the parity error flag. When this read only flag is "0", it indicates a parity error has not been detected. When the flag is "1", it indicates that the parity of the received word is incorrect. This error flag is applicable only if Parity mode (odd or even) is selected. The flag can also be cleared by a software sequence which involves a read to the status register USR followed by an access to the TXR\_RXR data register.
- Bit 6 NF:** Noise flag  
 0: No noise is detected  
 1: Noise is detected  
 The NF flag is the noise flag. When this read only flag is "0", it indicates no noise condition. When the flag is "1", it indicates that the UART has detected noise on the receiver input. The NF flag is set during the same cycle as the RXIF flag but will not be set in the case of an overrun. The NF flag can be cleared by a software sequence which will involve a read to the status register USR followed by an access to the TXR\_RXR data register.
- Bit 5 FERR:** Framing error flag  
 0: No framing error is detected  
 1: Framing error is detected  
 The FERR flag is the framing error flag. When this read only flag is "0", it indicates that there is no framing error. When the flag is "1", it indicates that a framing error has been detected for the current character. The flag can also be cleared by a software sequence which will involve a read to the status register USR followed by an access to the TXR\_RXR data register.
- Bit 4 OERR:** Overrun error flag  
 0: No overrun error is detected  
 1: Overrun error is detected  
 The OERR flag is the overrun error flag which indicates when the receiver buffer has overflowed. When this read only flag is "0", it indicates that there is no overrun error. When the flag is "1", it indicates that an overrun error occurs which will inhibit further transfers to the TXR\_RXR receive data register. The flag is cleared by a software sequence, which is a read to the status register USR followed by an access to the TXR\_RXR data register.
- Bit 3 RIDLE:** Receiver status  
 0: Data reception is in progress (data being received)  
 1: No data reception is in progress (receiver is idle)  
 The RIDLE flag is the receiver status flag. When this read only flag is "0", it indicates that the receiver is between the initial detection of the start bit and the completion of the stop bit. When the flag is "1", it indicates that the receiver is idle. Between the completion of the stop bit and the detection of the next start bit, the RIDLE bit is "1" indicating that the UART receiver is idle and the RX pin stays in logic high condition.

- Bit 2**      **RXIF:** Receive TXR\_RXR data register status  
0: TXR\_RXR data register is empty  
1: TXR\_RXR data register has available data  
The RXIF flag is the receive data register status flag. When this read only flag is "0", it indicates that the TXR\_RXR read data register is empty. When the flag is "1", it indicates that the TXR\_RXR read data register contains new data. When the contents of the shift register are transferred to the TXR\_RXR register, an interrupt is generated if RIE=1 in the UCR2 register. If one or more errors are detected in the received word, the appropriate receive-related flags NF, FERR, and/or PERR are set within the same clock cycle. The RXIF flag is cleared when the USR register is read with RXIF set, followed by a read from the TXR\_RXR register, and if the TXR\_RXR register has no data available.
- Bit 1**      **TIDLE:** Transmission idle  
0: Data transmission is in progress (data being transmitted)  
1: No data transmission is in progress (transmitter is idle)  
The TIDLE flag is known as the transmission complete flag. When this read only flag is "0", it indicates that a transmission is in progress. This flag will be set high when the TXIF flag is "1" and when there is no transmit data or break character being transmitted. When TIDLE is equal to "1", the TX pin becomes idle with the pin state in logic high condition. The TIDLE flag is cleared by reading the USR register with TIDLE set and then writing to the TXR\_RXR register. The flag is not generated when a data character or a break is queued and ready to be sent.
- Bit 0**      **TXIF:** Transmit TXR\_RXR data register status  
0: Character is not transferred to the transmit shift register  
1: Character has transferred to the transmit shift register (TXR\_RXR data register is empty)  
The TXIF flag is the transmit data register empty flag. When this read only flag is "0", it indicates that the character is not transferred to the transmitter shift register. When the flag is "1", it indicates that the transmitter shift register has received a character from the TXR\_RXR data register. The TXIF flag is cleared by reading the UART status register (USR) with TXIF set and then writing to the TXR\_RXR data register. Note that when the TXEN bit is set, the TXIF flag bit will also be set since the transmit data register is not yet full.

### UCR1 register

The UCR1 register together with the UCR2 register are the two UART control registers that are used to set the various options for the UART function, such as overall on/off control, parity control, data transfer bit length etc. Further explanation on each of the bits is given below:

Bit	7	6	5	4	3	2	1	0
Name	UARTEN	BNO	PREN	PRT	STOPS	TXBRK	RX8	TX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	W
POR	0	0	0	0	0	0	x	0

"x" unknown

**Bit 7**      **UARTEN:** UART function enable control

- 0: Disable UART. TX and RX pins are used as I/O or other pin-shared functional pins
- 1: Enable UART. TX and RX pins function as UART pins

The UARTEN bit is the UART enable bit. When this bit is equal to "0", the UART will be disabled and the RX pin as well as the TX pin will be as General Purpose I/O or other pin-shared functional pins. When the bit is equal to "1", the UART will be enabled and the TX and RX pins will function as defined by the TXEN and RXEN enable control bits.

When the UART is disabled, it will empty the buffer so any character remaining in the buffer will be discarded. In addition, the value of the baud rate counter will be reset. If the UART is disabled, all error and status flags will be reset. Also the TXEN, RXEN, TXBRK, RXIF, OERR, FERR, PERR and NF bits will be cleared, while the TIDLE, TXIF and RIDLE bits will be set. Other control bits in UCR1, UCR2 and BRG registers will remain unaffected. If the UART is active and the UARTEN bit is cleared, all pending transmissions and receptions will be terminated and the module will be reset as defined above. When the UART is re-enabled, it will restart in the same configuration.

**Bit 6**      **BNO:** Number of data transfer bits selection

- 0: 8-bit data transfer
- 1: 9-bit data transfer

This bit is used to select the data length format, which can have a choice of either 8-bit or 9-bit format. When this bit is equal to "1", a 9-bit data length format will be selected. If the bit is equal to "0", then an 8-bit data length format will be selected. If 9-bit data length format is selected, then bits RX8 and TX8 will be used to store the 9th bit of the received and transmitted data respectively.

**Bit 5**      **PREN:** Parity function enable control

- 0: Parity function is disabled
- 1: Parity function is enabled

This is the parity enable bit. When this bit is equal to "1", the parity function will be enabled. If the bit is equal to "0", then the parity function will be disabled. Replace the most significant bit position with a parity bit.

**Bit 4**      **PRT:** Parity type selection bit

- 0: Even parity for parity generator
- 1: Odd parity for parity generator

This bit is the parity type selection bit. When this bit is equal to "1", odd parity type will be selected. If the bit is equal to "0", then even parity type will be selected.

**Bit 3**      **STOPS:** Number of Stop bits selection

- 0: One stop bit format is used
- 1: Two stop bits format is used

This bit determines if one or two stop bits are to be used. When this bit is equal to "1", two stop bits are used. If this bit is equal to "0", then only one stop bit is used.

- Bit 2     **TXBRK:** Transmit break character  
           0: No break character is transmitted  
           1: Break characters transmit
- The TXBRK bit is the Transmit Break Character bit. When this bit is "0", there are no break characters and the TX pin operates normally. When the bit is "1", there are transmit break characters and the transmitter will send logic zeros. When this bit is equal to "1", after the buffered data has been transmitted, the transmitter output is held low for a minimum of a 13-bit length and until the TXBRK bit is reset.
- Bit 1     **RX8:** Receive data bit 8 for 9-bit data transfer format (read only)
- This bit is only used if 9-bit data transfers are used, in which case this bit location will store the 9th bit of the received data known as RX8. The BNO bit is used to determine whether data transfers are in 8-bit or 9-bit format.
- Bit 0     **TX8:** Transmit data bit 8 for 9-bit data transfer format (write only)
- This bit is only used if 9-bit data transfers are used, in which case this bit location will store the 9th bit of the transmitted data known as TX8. The BNO bit is used to determine whether data transfers are in 8-bit or 9-bit format.

### UCR2 register

The UCR2 register is the second of the two UART control registers and serves several purposes. One of its main functions is to control the basic enable/disable operation of the UART Transmitter and Receiver as well as enabling the various UART interrupt sources. The register also serves to control the baud rate speed, receiver wake-up enable and the address detect enable. Further explanation on each of the bits is given below:

Bit	7	6	5	4	3	2	1	0
Name	TXEN	RXEN	BRGH	ADDEN	WAKE	RIE	TIIE	TEIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7     **TXEN:** UART Transmitter enabled control  
           0: UART transmitter is disabled  
           1: UART transmitter is enabled
- The bit named TXEN is the Transmitter Enable Bit. When this bit is equal to "0", the transmitter will be disabled with any pending data transmissions being aborted. In addition the buffers will be reset. In this situation the TX pin will be used as an I/O or other pin-shared functional pin.
- If the TXEN bit is equal to "1" and the UARTEN bit is also equal to "1", the transmitter will be enabled and the TX pin will be controlled by the UART. Clearing the TXEN bit during a transmission will cause the data transmission to be aborted and will reset the transmitter. If this situation occurs, the TX pin will be used as an I/O or other pin-shared functional pin.
- Bit 6     **RXEN:** UART Receiver enabled control  
           0: UART receiver is disabled  
           1: UART receiver is enabled
- The bit named RXEN is the Receiver Enable Bit. When this bit is equal to "0", the receiver will be disabled with any pending data receptions being aborted. In addition the receive buffers will be reset. In this situation the RX pin will be used as an I/O or other pin-shared functional pin. If the RXEN bit is equal to "1" and the UARTEN bit is also equal to "1", the receiver will be enabled and the RX pin will be controlled by the UART. Clearing the RXEN bit during a reception will cause the data reception to be aborted and will reset the receiver. If this situation occurs, the RX pin will be used as an I/O or other pin-shared functional pin.

- Bit 5      **BRGH:** Baud Rate speed selection  
            0: Low speed baud rate  
            1: High speed baud rate  
            The bit named BRGH selects the high or low speed mode of the Baud Rate Generator. This bit, together with the value placed in the baud rate register BRG, controls the Baud Rate of the UART. If this bit is equal to "1", the high speed mode is selected. If the bit is equal to "0", the low speed mode is selected.
- Bit 4      **ADDEN:** Address detect function enable control  
            0: Address detect function is disabled  
            1: Address detect function is enabled  
            The bit named ADDEN is the address detect function enable control bit. When this bit is equal to "1", the address detect function is enabled. When it occurs, if the 8th bit, which corresponds to RX7 if BNO=0 or the 9th bit, which corresponds to RX8 if BNO=1, has a value of "1", then the received word will be identified as an address, rather than data. If the corresponding interrupt is enabled, an interrupt request will be generated each time the received word has the address bit set, which is the 8th or 9th bit depending on the value of BNO. If the address bit known as the 8th or 9th bit of the received word is "0" with the address detect function being enabled, an interrupt will not be generated and the received data will be discarded.
- Bit 3      **WAKE:** RX pin falling edge wake-up function enable control  
            0: RX pin wake-up function is disabled  
            1: RX pin wake-up function is enabled  
            The bit enables or disables the receiver wake-up function. If this bit is equal to 1 and the device is in IDLE0 or SLEEP mode, a falling edge on the RX pin will wake up the device. If this bit is equal to 0 and the device is in IDLE or SLEEP mode, any edge transitions on the RX pin will not wake up the device.
- Bit 2      **RIE:** Receiver interrupt enable control  
            0: Receiver related interrupt is disabled  
            1: Receiver related interrupt is enabled  
            This bit enables or disables the receiver interrupt. If this bit is equal to "1" and when the receiver overrun flag OERR or receive data available flag RXIF is set, the UART interrupt request flag will be set. If this bit is equal to "0", the UART interrupt request flag will not be influenced by the condition of the OERR or RXIF flags.
- Bit 1      **TIE:** Transmitter Idle interrupt enable control  
            0: Transmitter idle interrupt is disabled  
            1: Transmitter idle interrupt is enabled  
            This bit enables or disables the transmitter idle interrupt. If this bit is equal to "1" and when the transmitter idle flag TIDLE is set, due to a transmitter idle condition, the UART interrupt request flag will be set. If this bit is equal to "0", the UART interrupt request flag will not be influenced by the condition of the TIDLE flag.
- Bit 0      **TEIE:** Transmitter Empty interrupt enable control  
            0: Transmitter empty interrupt is disabled  
            1: Transmitter empty interrupt is enabled  
            This bit enables or disables the transmitter empty interrupt. If this bit is equal to "1" and when the transmitter empty flag TXIF is set, due to a transmitter empty condition, the UART interrupt request flag will be set. If this bit is equal to "0", the UART interrupt request flag will not be influenced by the condition of the TXIF flag.

**TXR\_RXR register**

Bit	7	6	5	4	3	2	1	0
Name	TXRX7	TXRX6	TXRX5	TXRX4	TXRX3	TXRX2	TXRX1	TXRX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0     **TXRX7~TXRX0**: UART Transmit/Receive Data bit 7 ~ bit 0

**BRG Register**

Bit	7	6	5	4	3	2	1	0
Name	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0
R/W								
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0     **BRG7~BRG0**: Baud Rate values

By programming the BRGH bit in UCR2 Register which allows selection of the related formula described above and programming the required value in the BRG register, the required baud rate can be setup.

Note: Baud rate=  $f_{SYS} / [64 \times (N+1)]$  if BRGH=0.

Baud rate=  $f_{SYS} / [16 \times (N+1)]$  if BRGH=1.

**Baud Rate Generator**

To setup the speed of the serial data communication, the UART function contains its own dedicated baud rate generator. The baud rate is controlled by its own internal free running 8-bit timer, the period of which is determined by two factors. The first of these is the value placed in the baud rate register BRG and the second is the value of the BRGH bit with the control register UCR2. The BRGH bit decides if the baud rate generator is to be used in a high speed mode or low speed mode, which in turn determines the formula that is used to calculate the baud rate. The value N in the BRG register which is used in the following baud rate calculation formula determines the division factor. Note that N is the decimal value placed in the BRG register and has a range of between 0 and 255.

UCR2 BRGH Bit	0	1
Baud Rate (BR)	$f_{SYS} / [64 (N+1)]$	$f_{SYS} / [16 (N+1)]$

By programming the BRGH bit which allows selection of the related formula and programming the required value in the BRG register, the required baud rate can be setup. Note that because the actual baud rate is determined using a discrete value, N, placed in the BRG register, there will be an error associated between the actual and requested value. The following example shows how the BRG register value N and the error value can be calculated.

**Calculating the Register and Error Values**

For a clock frequency of 4MHz, and with BRGH cleared to zero determine the BRG register value N, the actual baud rate and the error value for a desired baud rate of 4800.

From the above table the desired baud rate  $BR = f_{SYS} / [64 (N+1)]$

Re-arranging this equation gives  $N = [f_{SYS} / (BR \times 64)] - 1$

Giving a value for  $N = [4000000 / (4800 \times 64)] - 1 = 12.0208$

To obtain the closest value, a decimal value of 12 should be placed into the BRG register. This gives an actual or calculated baud rate value of  $BR = 4000000 / [64 \times (12+1)] = 4808$

Therefore the error is equal to  $(4808 - 4800) / 4800 = 0.16\%$

The following tables show actual values of baud rate and error values for the two values of BRGH.

Baud Rate K/BPS	Baud Rates for BRGH=0								
	f <sub>sys</sub> =4MHz			f <sub>sys</sub> =3.579545MHz			f <sub>sys</sub> =7.159MHz		
	BRG	Kbaud	Error (%)	BRG	Kbaud	Error (%)	BRG	Kbaud	Error (%)
0.3	207	0.300	0.16	185	0.300	0.00	—	—	—
1.2	51	1.202	0.16	46	1.190	-0.83	92	1.203	0.23
2.4	25	2.404	0.16	22	2.432	1.32	46	2.380	-0.83
4.8	12	4.808	0.16	11	4.661	-2.90	22	4.863	1.32
9.6	6	8.929	-6.99	5	9.321	-2.90	11	9.332	-2.90
19.2	2	20.833	8.51	2	18.643	-2.90	5	18.643	-2.90
38.4	—	—	—	—	—	—	2	32.286	-2.90
57.6	0	62.500	8.51	0	55.930	-2.90	1	55.930	-2.90
115.2	—	—	—	—	—	—	0	111.859	-2.90

Baud Rates and Error Values for BRGH = 0

Baud Rate K/BPS	Baud Rates for BRGH=1								
	f <sub>sys</sub> =4MHz			f <sub>sys</sub> =3.579545MHz			f <sub>sys</sub> =7.159MHz		
	BRG	Kbaud	Error (%)	BRG	Kbaud	Error (%)	BRG	Kbaud	Error (%)
0.3	—	—	—	—	—	—	—	—	—
1.2	207	1.202	0.16	185	1.203	0.23	—	—	—
2.4	103	2.404	0.16	92	2.406	0.23	185	2.406	0.23
4.8	51	4.808	0.16	46	4.76	-0.83	92	4.811	0.23
9.6	25	9.615	0.16	22	9.727	1.32	46	9.520	-0.83
19.2	12	19.231	0.16	11	18.643	-2.90	22	19.454	1.32
38.4	6	35.714	-6.99	5	37.286	-2.90	11	37.286	-2.90
57.6	3	62.5	8.51	3	55.930	-2.90	7	55.930	-2.90
115.2	1	125	8.51	1	111.86	-2.90	3	111.86	-2.90
250	0	250	0	—	—	—	—	—	—

Baud Rates and Error Values for BRGH = 1

## UART Setup and Control

For data transfer, the UART function utilizes a non-return-to-zero, more commonly known as NRZ, format. This is composed of one start bit, eight or nine data bits, and one or two stop bits. Parity is supported by the UART hardware, and can be setup to be even, odd or no parity. For the most common data format, 8 data bits along with no parity and one stop bit, denoted as 8, N, 1, is used as the default setting, which is the setting at power-on. The number of data bits and stop bits, along with the parity, are setup by programming the corresponding BNO, PRT, PREN, and STOPS bits in the UCR1 register. The baud rate used to transmit and receive data is setup using the internal 8-bit baud rate generator, while the data is transmitted and received LSB first. Although the UART transmitter and receiver are functionally independent, they both use the same data format and baud rate. In all cases stop bits will be used for data transmission.

### Enabling/Disabling the UART

The basic on/off function of the internal UART function is controlled using the UARTEN bit in the UCR1 register. If the UARTEN, TXEN and RXEN bits are set, then these two UART pins will act as normal TX output pin and RX input pin respectively. If no data is being transmitted on the TX pin, then it will default to a logic high value.

Clearing the UARTEN bit will disable the TX and RX pins and allow these two pins to be used as normal I/O or other pin-shared functional pins. When the UART function is disabled the buffer will be reset to an empty condition, at the same time discarding any remaining residual data. Disabling the UART will also reset the error and status flags with bits TXEN, RXEN, TXBRK, RXIF, OERR, FERR, PERR and NF being cleared while bits TIDLE, TXIF and RIDLE will be set. The remaining control bits in the UCR1, UCR2 and BRG registers will remain unaffected. If the UARTEN bit in the UCR1 register is cleared while the UART is active, then all pending transmissions and receptions will be immediately suspended and the UART will be reset to a condition as defined above. If the UART is then subsequently re-enabled, it will restart again in the same configuration.

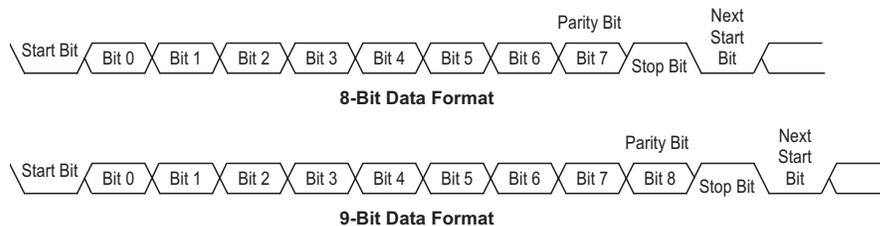
### Data, Parity and Stop bit Selection

The format of the data to be transferred is composed of various factors such as data bit length, parity on/off, parity type, address bits and the number of stop bits. These factors are determined by the setup of various bits within the UCR1 register. The BNO bit controls the number of data bits which can be set to either 8 or 9, the PRT bit controls the choice of odd or even parity, the PREN bit controls the parity on/off function and the STOPS bit decides whether one or two stop bits are to be used. The following table shows various formats for data transmission. The address bit identifies the frame as an address character. The number of stop bits, which can be either one or two, is independent of the data length.

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
<b>Example of 8-bit Data Formats</b>				
1	8	0	0	1
1	7	0	1	1
1	7	1	0	1
<b>Example of 9-bit Data Formats</b>				
1	9	0	0	1
1	8	0	1	1
1	8	1	0	1

**Transmitter Receiver Data Format**

The following diagram shows the transmit and receive waveforms for both 8-bit and 9-bit data formats.



## UART Transmitter

Data word lengths of either 8 or 9 bits can be selected by programming the BNO bit in the UCR1 register. When BNO bit is set, the word length will be set to 9 bits. In this case the 9th bit, which is the MSB, needs to be stored in the TX8 bit in the UCR1 register. At the transmitter core lies the Transmitter Shift Register, more commonly known as the TSR, whose data is obtained from the transmit data register, which is known as the TXR\_RXR register. The data to be transmitted is loaded into this TXR\_RXR register by the application program. The TSR register is not written to with new data until the stop bit from the previous transmission has been sent out. As soon as this stop bit has been transmitted, the TSR can then be loaded with new data from the TXR\_RXR register, if it is available. It should be noted that the TSR register, unlike many other registers, is not directly mapped into the Data Memory area and as such is not available to the application program for direct read/write operations. An actual transmission of data will normally be enabled when the TXEN bit is set, but the data will not be transmitted until the TXR\_RXR register has been loaded with data and the baud rate generator has defined a shift clock source. However, the transmission can also be initiated by first loading data into the TXR\_RXR register, after which the TXEN bit can be set. When a transmission of data begins, the TSR is normally empty, in which case a transfer to the TXR\_RXR register will result in an immediate transfer to the TSR. If during a transmission the TXEN bit is cleared, the transmission will immediately cease and the transmitter will be reset. The TX output pin will then return to the I/O or other pin-shared function.

### Transmitting Data

When the UART is transmitting data, the data is shifted on the TX pin from the shift register, with the least significant bit first. In the transmit mode, the TXR\_RXR register forms a buffer between the internal bus and the transmitter shift register. It should be noted that if 9-bit data format has been selected, then the MSB will be taken from the TX8 bit in the UCR1 register. The steps to initiate a data transfer can be summarized as follows:

- Make the correct selection of the BNO, PRT, PREN and STOPS bits to define the required word length, parity type and number of stop bits.
- Setup the BRG register to select the desired baud rate.
- Set the TXEN bit to ensure that the TX pin is used as a UART transmitter pin.
- Access the USR register and write the data that is to be transmitted into the TXR\_RXR register. Note that this step will clear the TXIF bit.
- This sequence of events can now be repeated to send additional data.

It should be noted that when TXIF=0, data will be inhibited from being written to the TXR\_RXR register. Clearing the TXIF flag is always achieved using the following software sequence:

1. A USR register access
2. A TXR\_RXR register write execution

The read-only TXIF flag is set by the UART hardware and if set indicates that the TXR\_RXR register is empty and that other data can now be written into the TXR\_RXR register without overwriting the previous data. If the TEIE bit is set then the TXIF flag will generate an interrupt.

During a data transmission, a write instruction to the TXR\_RXR register will place the data into the TXR\_RXR register, which will be copied to the shift register at the end of the present transmission. When there is no data transmission in progress, a write instruction to the TXR\_RXR register will place the data directly into the shift register, resulting in the commencement of data transmission, and the TXIF bit being immediately set. When a frame transmission is complete, which happens after stop bits are sent or after the break frame, the TIDLE bit will be set. To clear the TIDLE bit the following software sequence is used:

1. A USR register access
2. A TXR\_RXR register write execution

Note that both the TXIF and TIDLE bits are cleared by the same software sequence.

### Transmit Break

If the TXBRK bit is set then break characters will be sent on the next transmission. Break character transmission consists of a start bit, followed by  $13 \times N$  '0' bits and stop bits, where  $N=1, 2, \text{ etc.}$  If a break character is to be transmitted then the TXBRK bit must be first set by the application program, and then cleared to generate the stop bits. Transmitting a break character will not generate a transmit interrupt. Note that a break condition length is at least 13 bits long. If the TXBRK bit is continually kept at a logic high level then the transmitter circuitry will transmit continuous break characters. After the application program has cleared the TXBRK bit, the transmitter will finish transmitting the last break character and subsequently send out one or two stop bits. The automatic logic highs at the end of the last break character will ensure that the start bit of the next frame is recognized.

### UART Receiver

The UART is capable of receiving word lengths of either 8 or 9 bits. If the BNO bit is set, the word length will be set to 9 bits with the MSB being stored in the RX8 bit of the UCR1 register. At the receiver core lies the Receive Serial Shift Register, commonly known as the RSR. The data which is received on the RX external input pin is sent to the data recovery block. The data recovery block operating speed is 16 times that of the baud rate, while the main receive serial shifter operates at the baud rate. After the RX pin is sampled for the stop bit, the received data in RSR is transferred to the receive data register, if the register is empty. The data which is received on the external RX input pin is sampled three times by a majority detect circuit to determine the logic level that has been placed onto the RX pin. It should be noted that the RSR register, unlike many other registers, is not directly mapped into the Data Memory area and as such is not available to the application program for direct read/write operations.

### Receiving Data

When the UART receiver is receiving data, the data is serially shifted in on the external RX input pin, LSB first. In the read mode, the TXR\_RXR register forms a buffer between the internal bus and the receiver shift register. The TXR\_RXR register is a two byte deep FIFO data buffer, where two bytes can be held in the FIFO while a third byte can continue to be received. Note that the application program must ensure that the data is read from TXR\_RXR before the third byte has been completely shifted in, otherwise this third byte will be discarded and an overrun error OERR will be subsequently indicated. The steps to initiate a data transfer can be summarized as follows:

- Make the correct selection of BNO, PRT, PREN and STOPS bits to define the word length, parity type and number of stop bits.
- Setup the BRG register to select the desired baud rate.
- Set the RXEN bit to ensure that the RX pin is used as a UART receiver pin.

At this point the receiver will be enabled which will begin to look for a start bit.

When a character is received the following sequence of events will occur:

- The RXIF bit in the USR register will be set when TXR\_RXR register has data available; at least one more character can be read.
- When the contents of the shift register have been transferred to the TXR\_RXR register, then if the RIE bit is set, an interrupt will be generated.
- If during reception, a frame error, noise error, parity error, or an overrun error has been detected, then the error flags can be set.

The RXIF bit can be cleared using the following software sequence:

1. A USR register access
2. A TXR\_RXR register read execution

### **Receive Break**

Any break character received by the UART will be managed as a framing error. The receiver will count and expect a certain number of bit times as specified by the values programmed into the BNO and STOPS bits. If the break is much longer than 13 bit times, the reception will be considered as complete after the number of bit times specified by BNO and STOPS. The RXIF bit is set, FERR is set, zeros are loaded into the receive data register, interrupts are generated if appropriate and the RIDLE bit is set. If a long break signal has been detected and the receiver has received a start bit, the data bits and the invalid stop bit, which sets the FERR flag, the receiver must wait for a valid stop bit before looking for the next start bit. The receiver will not make the assumption that the break condition on the line is the next start bit. A break is regarded as a character that contains only zeros with the FERR flag set. The break character will be loaded into the buffer and no further data will be received until stop bits are received. It should be noted that the RIDLE read only flag will go high when the stop bits have not yet been received. The reception of a break character on the UART registers will result in the following:

- The framing error flag, FERR, will be set.
- The receive data register, TXR\_RXR, will be cleared.
- The OERR, NF, PERR, RIDLE or RXIF flags will possibly be set.

### **Idle Status**

When the receiver is reading data, which means it will be in between the detection of a start bit and the reading of a stop bit, the receiver status flag in the USR register, otherwise known as the RIDLE flag, will have a zero value. In between the reception of a stop bit and the detection of the next start bit, the RIDLE flag will have a high value, which indicates the receiver is in an idle condition.

### **Receiver Interrupt**

The read only receive interrupt flag RXIF in the USR register is set by an edge generated by the receiver. An interrupt is generated if RIE=1, when a word is transferred from the Receive Shift Register, RSR, to the Receive Data Register, TXR\_RXR. An overrun error can also generate an interrupt if RIE=1.

## **Managing Receiver Errors**

Several types of reception errors can occur within the UART module, the following section describes the various types and how they are managed by the UART.

### **Overrun Error – OERR Flag**

The TXR\_RXR register is composed of a two byte deep FIFO data buffer, where two bytes can be held in the FIFO register, while a third byte can continue to be received. Before this third byte has been entirely shifted in, the data should be read from the TXR\_RXR register. If this is not done, the overrun error flag OERR will be consequently indicated.

In the event of an overrun error occurring, the following will happen:

- The OERR flag in the USR register will be set.
- The TXR\_RXR contents will not be lost.
- The shift register will be overwritten.
- An interrupt will be generated if the RIE bit is set.

The OERR flag can be cleared by an access to the USR register followed by a read to the TXR\_RXR register.

**Noise Error – NF Flag**

Over-sampling is used for data recovery to identify valid incoming data and noise. If noise is detected within a frame the following will occur:

- The read only noise flag, NF, in the USR register will be set on the rising edge of the RXIF bit.
- Data will be transferred from the Shift register to the TXR\_RXR register.
- No interrupt will be generated. However this bit rises at the same time as the RXIF bit which itself generates an interrupt.

Note that the NF flag is reset by a USR register read operation followed by a TXR\_RXR register read operation.

**Framing Error – FERR Flag**

The read only framing error flag, FERR, in the USR register, is set if a zero is detected instead of stop bits. If two stop bits are selected, both stop bits must be high; otherwise the FERR flag will be set. The FERR flag is buffered along with the received data and is cleared on any reset.

**Parity Error – PERR Flag**

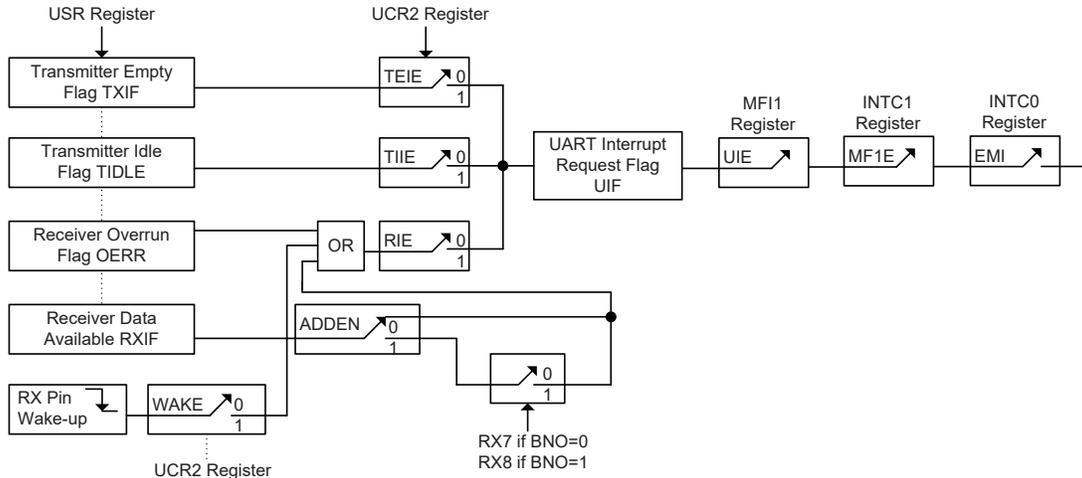
The read only parity error flag, PERR, in the USR register, is set if the parity of the received word is incorrect. This error flag is only applicable if the parity is enabled, PREN = 1, and if the parity type, odd or even is selected. The read only PERR flag is buffered along with the received data bytes. It is cleared on any reset. It should be noted that the FERR and PERR flags are buffered along with the corresponding word and should be read before reading the data word.

**UART Module Interrupt Structure**

Several individual UART conditions can generate a UART interrupt. When these conditions exist, a low pulse will be generated to get the attention of the microcontroller. These conditions are a transmitter data register empty, transmitter idle, receiver data available, receiver overrun, address detect and an RX pin wake-up. When any of these conditions are created, if the global interrupt enable bit, multi-function interrupt enable bit and its corresponding interrupt control bit are enabled and the stack is not full, the program will jump to its corresponding interrupt vector where it can be serviced before returning to the main program. Four of these conditions have the corresponding USR register flags which will generate a UART interrupt if its associated interrupt enable control bit in the UCR2 register is set. The two transmitter interrupt conditions have their own corresponding enable control bits, while the two receiver interrupt conditions have a shared enable control bit. These enable bits can be used to mask out individual UART interrupt sources.

The address detect condition, which is also a UART interrupt source, does not have an associated flag, but will generate a UART interrupt when an address detect condition occurs if its function is enabled by setting the ADDEN bit in the UCR2 register. An RX pin wake-up, which is also a UART interrupt source, does not have an associated flag, but will generate a UART interrupt if the microcontroller is woken up from IDLE0 or SLEEP mode by a falling edge on the RX pin, if the WAKE and RIE bits in the UCR2 register are set. Note that in the event of an RX wake-up interrupt occurring, there will be a certain period of delay, commonly known as the System Start-up Time, for the oscillator to restart and stabilize before the system resumes normal operation.

Note that the USR register flags are read only and cannot be cleared or set by the application program, neither will they be cleared when the program jumps to the corresponding interrupt servicing routine, as is the case for some of the other interrupts. The flags will be cleared automatically when certain actions are taken by the UART, the details of which are given in the UART register section. The overall UART interrupt can be disabled or enabled by the related interrupt enable control bits in the interrupt control registers of the microcontroller to decide whether the interrupt requested by the UART module is masked out or allowed.



UART Interrupt Scheme

### Address Detect Mode

Setting the Address Detect Mode bit, ADDEN, in the UCR2 register, enables this special mode. If this bit is enabled then an additional qualifier will be placed on the generation of a Receiver Data Available interrupt, which is requested by the RXIF flag. If the ADDEN bit is enabled, then when data is available, an interrupt will only be generated, if the highest received bit has a high value. Note that the MFnE, UIE and EMI interrupt enable bits must also be enabled for correct interrupt generation. This highest address bit is the 9th bit if BNO=1 or the 8th bit if BNO=0. If this bit is high, then the received word will be defined as an address rather than data. A Data Available interrupt will be generated every time the last bit of the received word is set. If the ADDEN bit is not enabled, then a Receiver Data Available interrupt will be generated each time the RXIF flag is set, irrespective of the data last bit status. The address detect mode and parity enable are mutually exclusive functions. Therefore if the address detect mode is enabled, then to ensure correct operation, the parity function should be disabled by resetting the parity enable bit to zero.

ADDEN	Bit 9 if BNO=1, Bit 8 if BNO=0	UART Interrupt Generated
0	0	√
	1	√
1	0	×
	1	√

ADDEN Bit Function

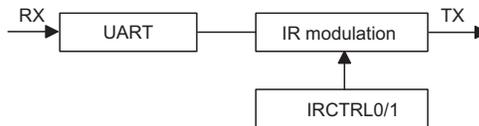
### UART Module Power Down and Wake-up

When the MCU system clock is switched off, the UART will cease to function. If the MCU executes the "HALT" instruction and switches off the system clock while a transmission is still in progress, then the transmission will be paused until the UART clock source derived from the microcontroller is activated. In a similar way, if the MCU executes the "HALT" instruction and switches off the system clock while receiving data, then the reception of data will likewise be paused. When the MCU enters the IDLE or SLEEP Mode, note that the USR, UCR1, UCR2, transmit and receive registers, as well as the BRG register will not be affected. It is recommended to make sure first that the UART data transmission or reception has been finished before the microcontroller enters the IDLE or SLEEP mode.

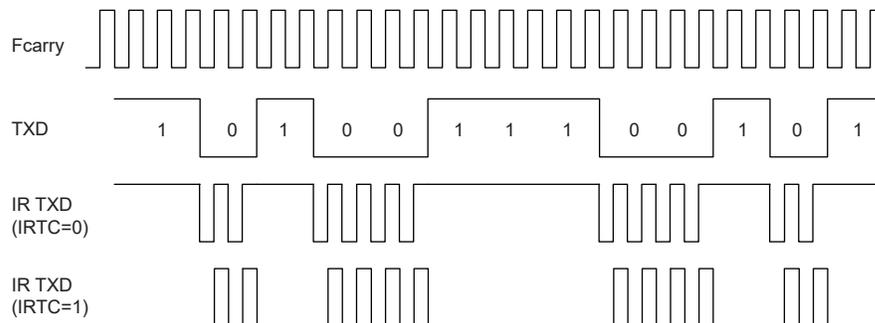
The UART function contains a receiver RX pin wake-up function, which is enabled or disabled by the WAKE bit in the UCR2 register. If this bit, along with the UART enable bit, UARTEN, the receiver enable bit, RXEN and the receiver interrupt bit, RIE, are all set before the MCU enters the IDLE0 or SLEEP Mode, then a falling edge on the RX pin will wake up the MCU from the IDLE0 or SLEEP Mode. Note that as it takes certain system clock cycles after a wake-up, before normal microcontroller operation resumes, any data received during this time on the RX pin will be ignored. For a UART wake-up interrupt to occur, in addition to the bits for the wake-up being set, the global interrupt enable bit, EMI, and the UART interrupt enable bit, UIE, must be set. If the EMI and UIE bits are not set then only a wake up event will occur and no interrupt will be generated. Note also that as it takes certain system clock cycles after a wake-up before normal microcontroller resumes, the UART interrupt will not be generated until after this time has elapsed.

### IR Modulation Interface

The UART interface has an integrated IR modulation interface. Infrared modulation frequency control by register IRCTRL0, its value is any integer between 0 and 127.



Infrared modulation: When TXD = 0 only, the IR modulation will produce infrared mixing and output data. To meet the needs of both PNP and NPN infrared driver tube, located in the register IRCTRL0 bit7 IRTC, control the polarity of the output of the infrared modulation. IRTC = 0 for positive polarity output, suitable for PNP transistor driver; IRTC = 1 for a negative output, suitable for the NPN driver. See below:



**IRCTRL0 Register**

Bit	7	6	5	4	3	2	1	0
Name	IRTC	IRDC6	IRDC5	IRDC4	IRDC3	IRDC2	IRDC1	IRDC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **IRTC**: IR modulation output polarity select  
 0: Negative  
 1: Positive

Bit 6~0 **IRDC6~IRDC0**: IR modulation frequency divider coefficient  
 $F_{carry} = (f_{sys}/(IRDC+1))/2$

**IRCTRL1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	IRME0
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1 Unimplemented, read as "0"

Bit 0 **IRME0**: UART TX IR modulation control  
 0: UART TX IR modulation disable  
 1: UART TX IR modulation enable

## Interrupts

Interrupts are an important part of any microcontroller system. When an external event or an internal function such as a Timer Module or an A/D converter requires microcontroller attention, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs. Each device contains several external interrupt and internal interrupts functions. The external interrupts are generated by the action of the external INT0~INT3 pins, while the internal interrupts are generated by various internal functions such as the TMs, Time Base, LVD, EEPROM and the A/D converter.

### Interrupt Registers

Overall interrupt control, which basically means the setting of request flags when certain microcontroller conditions occur and the setting of interrupt enable bits by the application program, is controlled by a series of registers, located in the Special Purpose Data Memory. The first is the INTC0~INTC3 registers which setup the primary interrupts, the second is the MFI0~MFI3 registers which setup the Multi-function interrupts. Finally there is an INTEG register to setup the external interrupt trigger edge type.

Each register contains a number of enable bits to enable or disable individual registers as well as interrupt flags to indicate the presence of an interrupt request. The naming convention of these follows a specific pattern. First is listed an abbreviated interrupt type, then the (optional) number of that interrupt followed by either an "E" for enable/disable bit or "F" for request flag.

Function	Enable Bit	Request Flag	Notes
Global	EMI	—	—
INTn Pin	INTnE	INTnF	n=0~3
Multi-function	MFnE	MFnF	n=0~3
A/D Converter	ADE	ADF	—
Time Base	TBnE	TBnF	n=0~1
LVD	LVE	LVF	—
EEPROM	DEE	DEF	—
SIM	SIE	SIF	—
I <sup>2</sup> C time out	I2CTOE	I2CTOF	—
UART	UIE	UIF	—
TM	TnPE	TnPF	n=0~3
	TnAE	TnAF	
Comparator	CPnE	CPnF	n=0~1

#### Interrupt Register Bit Naming Conventions

Register Name	Bit							
	7	6	5	4	3	2	1	0
INTEG	INT3S1	INT3S0	INT2S1	INT2S0	INT1S1	INT1S0	INT0S1	INT0S0
INTC0	—	MF0F	INT1F	INT0F	MF0E	INT1E	INT0E	EMI
INTC1	MF1F	TB1F	TB0F	ADF	MF1E	TB1E	TB0E	ADE
INTC2	CP1F	CP0F	MF3F	MF2F	CP1E	CP0E	MF3E	MF2E
INTC3	—	—	INT3F	INT2F	—	—	INT3E	INT2E
MFI0	—	—	T0AF	T0PF	—	—	T0AE	T0PE
MFI1	UIF	SIF	DEF	LVF	UIE	SIE	DEE	LVE
MFI2	I2CTOF	—	T1AF	T1PF	I2CTOE	—	T1AE	T1PE
MFI3	T3AF	T3PF	T2AF	T2PF	T3AE	T3PE	T2AE	T2PE

#### Interrupt Register Contents

### INTEG Register

Bit	7	6	5	4	3	2	1	0
Name	INT3S1	INT3S0	INT2S1	INT2S0	INT1S1	INT1S0	INT0S1	INT0S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7~6 **INT3S1~INT3S0**: interrupt edge control for INT3 pin  
 00: Disable  
 01: Rising edge  
 10: Falling edge  
 11: Rising and falling edges
- Bit 5~4 **INT2S1~INT2S0**: interrupt edge control for INT2 pin  
 00: Disable  
 01: Rising edge  
 10: Falling edge  
 11: Rising and falling edges
- Bit 3~2 **INT1S1~INT1S0**: interrupt edge control for INT1 pin  
 00: Disable  
 01: Rising edge  
 10: Falling edge  
 11: Rising and falling edges
- Bit 1~0 **INT0S1~INT0S0**: interrupt edge control for INT0 pin  
 00: Disable  
 01: Rising edge  
 10: Falling edge  
 11: Rising and falling edges

### INTC0 Register

Bit	7	6	5	4	3	2	1	0
Name	—	MFOF	INT1F	INT0F	MFOE	INT1E	INT0E	EMI
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	0	0	0	0	0

- Bit 7 Unimplemented, read as "0"
- Bit 6 **MFOF**: Multi-function Interrupt 0 Request Flag  
 0: No request  
 1: Interrupt request
- Bit 5 **INT1F**: INT1 interrupt request flag  
 0: No request  
 1: Interrupt request
- Bit 4 **INT0F**: INT0 interrupt request flag  
 0: No request  
 1: Interrupt request
- Bit 3 **MFOE**: Multi-function Interrupt 0 Control  
 0: Disable  
 1: Enable
- Bit 2 **INT1E**: INT1 interrupt control  
 0: Disable  
 1: Enable
- Bit 1 **INT0E**: INT0 interrupt control  
 0: Disable  
 1: Enable
- Bit 0 **EMI**: Global interrupt control  
 0: Disable  
 1: Enable

**INTC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	MF1F	TB1F	TB0F	ADF	MF1E	TB1E	TB0E	ADE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7      **MF1F**: Multi-function Interrupt 1 Request Flag  
0: No request  
1: Interrupt request
- Bit 6      **TB1F**: Time Base 1 Interrupt Request Flag  
0: No request  
1: Interrupt request
- Bit 5      **TB0F**: Time Base 0 Interrupt Request Flag  
0: No request  
1: Interrupt request
- Bit 4      **ADF**: A/D Converter Interrupt Request Flag  
0: No request  
1: Interrupt request
- Bit 3      **MF1E**: Multi-function Interrupt 1 Control  
0: Disable  
1: Enable
- Bit 2      **TB1E**: Time Base 1 Interrupt Control  
0: Disable  
1: Enable
- Bit 1      **TB0E**: Time Base 0 Interrupt Control  
0: Disable  
1: Enable
- Bit 0      **ADE**: A/D Converter Interrupt Control  
0: Disable  
1: Enable

**INTC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	CP1F	CP0F	MF3F	MF2F	CP1E	CP0E	MF3E	MF2E
R/W								
POR	0	0	0	0	0	0	0	0

- Bit 7      **CP1F**: Comparator 1 Interrupt Request Flag  
0: No request  
1: Interrupt request
- Bit 6      **CP0F**: Comparator 0 Interrupt Request Flag  
0: No request  
1: Interrupt request
- Bit 5      **MF3F**: Multi-function Interrupt 3 Request Flag  
0: No request  
1: Interrupt request
- Bit 4      **MF2F**: Multi-function Interrupt 2 Request Flag  
0: No request  
1: Interrupt request
- Bit 3      **CP1E**: Comparator 1 Interrupt Control  
0: Disable  
1: Enable
- Bit 2      **CP0E**: Comparator 0 Interrupt Control  
0: Disable  
1: Enable

- Bit 1      **MF3E**: Multi-function Interrupt 3 Control  
             0: Disable  
             1: Enable
- Bit 0      **MF2E**: Multi-function Interrupt 2 Control  
             0: Disable  
             1: Enable

**INTC3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	INT3F	INT2F	—	—	INT3E	INT2E
R/W	—	—	R/W	R/W	—	—	R/W	R/W
POR	—	—	0	0	—	—	0	0

- Bit 7~6      Unimplemented, read as "0"
- Bit 5      **INT3F**: INT3 interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 4      **INT2F**: INT2 interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 3~2      Unimplemented, read as "0"
- Bit 1      **INT3E**: INT3 interrupt control  
             0: Disable  
             1: Enable
- Bit 0      **INT2E**: INT2 interrupt control  
             0: Disable  
             1: Enable

**MF10 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	T0AF	T0PF	—	—	T0AE	T0PE
R/W	—	—	R/W	R/W	—	—	R/W	R/W
POR	—	—	0	0	—	—	0	0

- Bit 7~6      Unimplemented, read as "0"
- Bit 5      **T0AF**: TM0 Comparator A match interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 4      **T0PF**: TM0 Comparator P match interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 3~2      Unimplemented, read as "0"
- Bit 1      **T0AE**: TM0 Comparator A match interrupt control  
             0: Disable  
             1: Enable
- Bit 0      **T0PE**: TM0 Comparator P match interrupt control  
             0: Disable  
             1: Enable

**MF11 Register**

Bit	7	6	5	4	3	2	1	0
Name	UIF	SIF	DEF	LVF	UIE	SIE	DEE	LVE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7     **UIF**: UART interrupt request flag  
0: No request  
1: Interrupt request
- Bit 6     **SIF**: SIM interrupt request flag  
0: No request  
1: Interrupt request
- Bit 5     **DEF**: Data EEPROM interrupt request flag  
0: No request  
1: Interrupt request
- Bit 4     **LVF**: LVD interrupt request flag  
0: No request  
1: Interrupt request
- Bit 3     **UIE**: UART interrupt control  
0: Disable  
1: Enable
- Bit 2     **SIE**: SIM Interrupt Control  
0: Disable  
1: Enable
- Bit 1     **DEE**: Data EEPROM interrupt control  
0: Disable  
1: Enable
- Bit 0     **LVE**: LVD Interrupt Control  
0: Disable  
1: Enable

**MF12 Register**

Bit	7	6	5	4	3	2	1	0
Name	I2CTOF	—	T1AF	T1PF	I2CTOE	—	T1AE	T1PE
R/W	R/W	—	R/W	R/W	R/W	—	R/W	R/W
POR	0	—	0	0	0	—	0	0

- Bit 7     **I2CTOF**: I<sup>2</sup>C Time Out interrupt request flag  
0: No request  
1: Interrupt request
- Bit 6     Unimplemented, read as "0"
- Bit 5     **T1AF**: TM1 Comparator A match interrupt request flag  
0: No request  
1: Interrupt request
- Bit 4     **T1PF**: TM1 Comparator P match interrupt request flag  
0: No request  
1: Interrupt request
- Bit 3     **I2CTOE**: I<sup>2</sup>C Time Out interrupt control  
0: Disable  
1: Enable
- Bit 2     Unimplemented, read as "0"
- Bit 1     **T1AE**: TM1 Comparator A match interrupt control  
0: Disable  
1: Enable
- Bit 0     **T1PE**: TM1 Comparator P match interrupt control  
0: Disable  
1: Enable

**MF13 Register**

Bit	7	6	5	4	3	2	1	0
Name	T3AF	T3PF	T2AF	T2PF	T3AE	T3PE	T2AE	T2PE
R/W								
POR	0	0	0	0	0	0	0	0

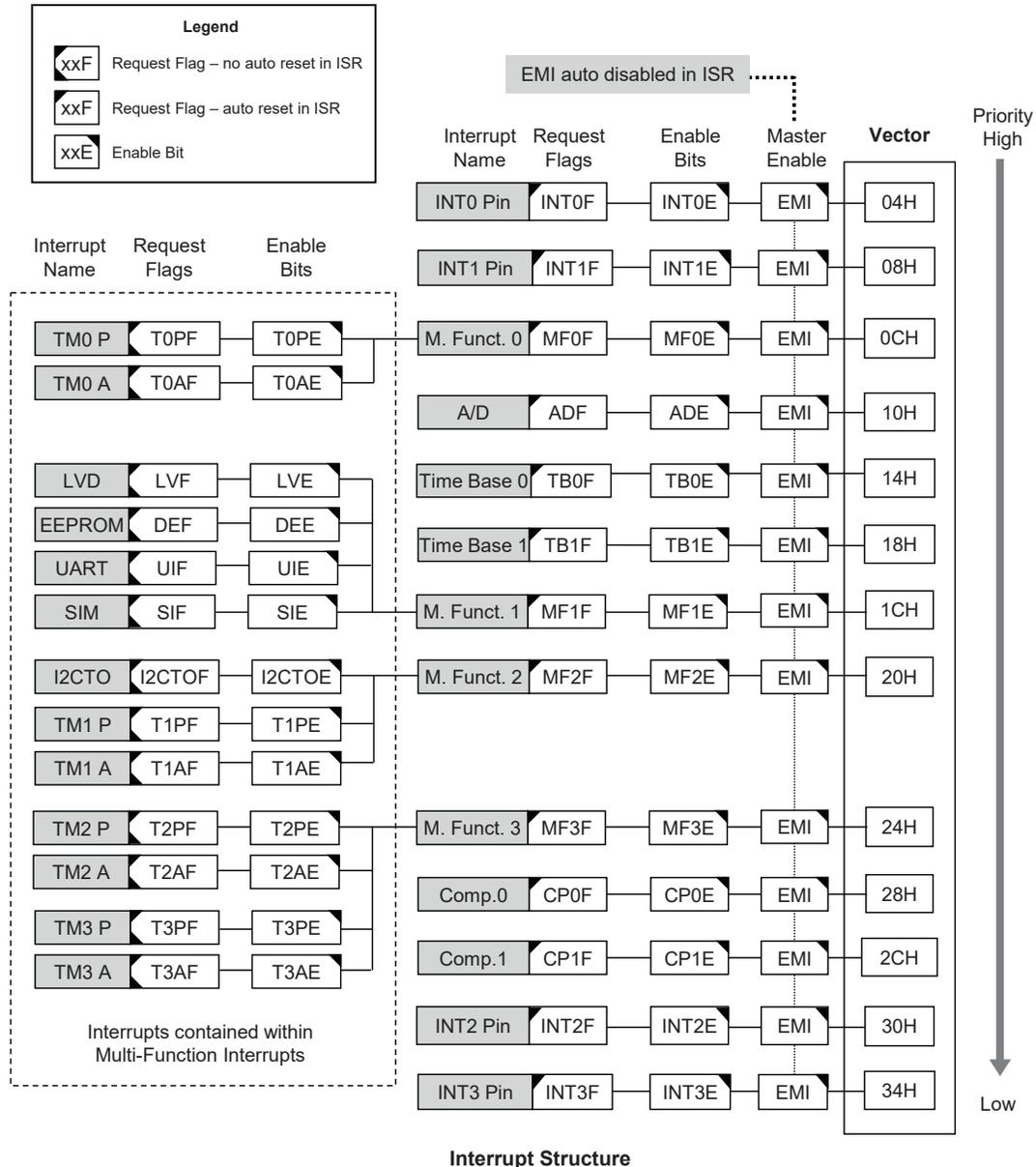
- Bit 7      **T3AF**: TM3 Comparator A match interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 6      **T3PF**: TM3 Comparator P match interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 5      **T2AF**: TM2 Comparator A match interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 4      **T2PF**: TM2 Comparator P match interrupt request flag  
             0: No request  
             1: Interrupt request
- Bit 3      **T3AE**: TM3 Comparator A match interrupt control  
             0: Disable  
             1: Enable
- Bit 2      **T3PE**: TM3 Comparator P match interrupt control  
             0: Disable  
             1: Enable
- Bit 1      **T2AE**: TM2 Comparator A match interrupt control  
             0: Disable  
             1: Enable
- Bit 0      **T2PE**: TM2 Comparator P match interrupt control  
             0: Disable  
             1: Enable

**Interrupt Operation**

When the conditions for an interrupt event occur, such as a TM Comparator P, Comparator A match or A/D conversion completion etc., the relevant interrupt request flag will be set. Whether the request flag actually generates a program jump to the relevant interrupt vector is determined by the condition of the interrupt enable bit. If the enable bit is set high then the program will jump to its relevant vector; if the enable bit is zero then although the interrupt request flag is set an actual interrupt will not be generated and the program will not jump to the relevant interrupt vector. The global interrupt enable bit, if cleared to zero, will disable all interrupts.

When an interrupt is generated, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a "JMP" which will jump to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a "RETI", which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred. The various interrupt enable bits, together with their associated request flags, are shown in the accompanying diagrams with their order of priority. Some interrupt sources have their own individual vector while others share the same multi-function interrupt vector. Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the global interrupt enable bit, EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded.

If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full. In case of simultaneous requests, the accompanying diagram shows the priority that is applied. All of the interrupt request flags when set will wake-up the devices if it is in SLEEP or IDLE Mode, however to prevent a wake-up from occurring the corresponding flag should be set before the devices are in SLEEP or IDLE Mode.



## **External Interrupt**

The external interrupts are controlled by signal transitions on the pins INT0~INT3. An external interrupt request will take place when the external interrupt request flags, INT0F~INT3F, are set, which will occur when a transition, whose type is chosen by the edge select bits, appears on the external interrupt pins. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and respective external interrupt enable bit, INT0E~INT3E, must first be set. Additionally the correct interrupt edge type must be selected using the INTEG register to enable the external interrupt function and to choose the trigger edge type. As the external interrupt pins are pin-shared with I/O pins, they can only be configured as external interrupt pins if their external interrupt enable bit in the corresponding interrupt register has been set. The pin must also be setup as an input by setting the corresponding bit in the port control register. When the interrupt is enabled, the stack is not full and the correct transition type appears on the external interrupt pin, a subroutine call to the external interrupt vector, will take place. When the interrupt is serviced, the external interrupt request flags, INT0F~INT3F, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts. Note that any pull-high resistor selections on the external interrupt pins will remain valid even if the pin is used as an external interrupt input. The INTEG register is used to select the type of active edge that will trigger the external interrupt. A choice of either rising or falling or both edge types can be chosen to trigger an external interrupt. Note that the INTEG register can also be used to disable the external interrupt function.

## **Comparator Interrupt**

The comparator interrupts are controlled by the two internal comparators. A comparator interrupt request will take place when the comparator interrupt request flags, CP0F or CP1F, are set, a situation that will occur when the comparator output CnOUT bit changes state. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and comparator interrupt enable bits, CP0E and CP1E, must first be set. When the interrupt is enabled, the stack is not full and the comparator inputs generate a comparator output transition, a subroutine call to the comparator interrupt vector, will take place. When the interrupt is serviced, the comparator interrupt request flags will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

## **A/D Converter Interrupt**

The A/D Converter Interrupt is controlled by the termination of an A/D conversion process. An A/D Converter Interrupt request will take place when the A/D Converter Interrupt request flag, ADF, is set, which occurs when the A/D conversion process finishes. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and A/D Interrupt enable bit, ADE, must first be set. When the interrupt is enabled, the stack is not full and the A/D conversion process has ended, a subroutine call to the A/D Converter Interrupt vector, will take place. When the interrupt is serviced, the A/D Converter Interrupt flag, ADF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

### **Multi-function Interrupt**

Within these devices there are up to four Multi-function interrupts. Unlike the other independent interrupts, these interrupts have no independent source, but rather are formed from other existing interrupt sources, namely the TM Interrupts, LVD interrupt, UART interrupt, SIM Interrupt, I<sup>2</sup>C time out Interrupt and EEPROM Interrupt.

A Multi-function interrupt request will take place when any of the Multi-function interrupt request flags, MFnF are set. The Multi-function interrupt flags will be set when any of their included functions generate an interrupt request flag. To allow the program to branch to its respective interrupt vector address, when the Multi-function interrupt is enabled and the stack is not full, and either one of the interrupts contained within each of Multi-function interrupt occurs, a subroutine call to one of the Multi-function interrupt vectors will take place. When the interrupt is serviced, the related Multi-Function request flag will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

However, it must be noted that, although the Multi-function Interrupt flags will be automatically reset when the interrupt is serviced, the request flags from the original source of the Multi-function interrupts, namely the TM Interrupts, LVD interrupt, UART interrupt, SIM Interrupt, I<sup>2</sup>C time out Interrupt and EEPROM Interrupt will not be automatically reset and must be manually reset by the application program.

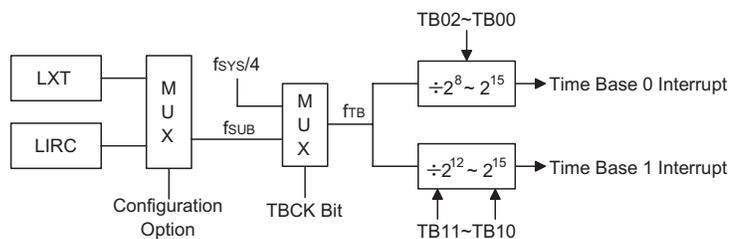
### **Serial Interface Module Interrupt**

The Serial Interface Module Interrupt, also known as the SIM interrupt, is contained within the Multi-function Interrupt. An SIM Interrupt request will take place when the SIM Interrupt request flag, SIF, is set, which occurs when a byte of data has been received or transmitted by the SIM interface or I<sup>2</sup>C address match. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and the Serial Interface Interrupt enable bit, SIE, and Muti-function interrupt enable bits, must first be set. When the interrupt is enabled, the stack is not full and a byte of data has been transmitted or received by the SIM interface or I<sup>2</sup>C address match, a subroutine call to the respective Multi-function Interrupt vector, will take place. When the Serial Interface Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the SIF flag will not be automatically cleared, it has to be cleared by the application program.

## Time Base Interrupts

The function of the Time Base Interrupts is to provide regular time signal in the form of an internal interrupt. They are controlled by the overflow signals from their respective timer functions. When these happens their respective interrupt request flags, TB0F or TB1F will be set. To allow the program to branch to their respective interrupt vector addresses, the global interrupt enable bit, EMI and Time Base enable bits, TB0E or TB1E, must first be set. When the interrupt is enabled, the stack is not full and the Time Base overflows, a subroutine call to their respective vector locations will take place. When the interrupt is serviced, the respective interrupt request flag, TB0F or TB1F, will be automatically reset and the EMI bit will be cleared to disable other interrupts.

The purpose of the Time Base Interrupt is to provide an interrupt signal at fixed time periods. Their clock sources originate from the internal clock source  $f_{TB}$ . This  $f_{TB}$  input clock passes through a divider, the division ratio of which is selected by programming the appropriate bits in the TBC register to obtain longer interrupt periods whose value ranges. The clock source that generates  $f_{TB}$ , which in turn controls the Time Base interrupt period, can originate from several different sources, as shown in the System Operating Mode section.



Time Base Interrupt

## TBC Register

Bit	7	6	5	4	3	2	1	0
Name	TBON	TBCK	TB11	TB10	LXTLP	TB02	TB01	TB00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	1	0	1	1	1

- Bit 7      **TBON**: TB0 and TB1 Control  
0: Disable  
1: Enable
- Bit 6      **TBCK**: Select  $f_{TB}$  Clock  
0:  $f_{SUB}$   
1:  $f_{SYS}/4$
- Bit 5~4    **TB11~TB10**: Select Time Base 1 Time-out Period  
00:  $2^{12}/f_{TB}$   
01:  $2^{13}/f_{TB}$   
10:  $2^{14}/f_{TB}$   
11:  $2^{15}/f_{TB}$
- Bit 3      **LXTLP**: LXT Low Power Control  
0: Disable (LXT quick start-up)  
1: Enable (LXT slow start-up)
- Bit 2~0    **TB02~TB00**: Select Time Base 0 Time-out Period  
000:  $2^8/f_{TB}$   
001:  $2^9/f_{TB}$   
010:  $2^{10}/f_{TB}$   
011:  $2^{11}/f_{TB}$   
100:  $2^{12}/f_{TB}$   
101:  $2^{13}/f_{TB}$   
110:  $2^{14}/f_{TB}$   
111:  $2^{15}/f_{TB}$

### **I<sup>2</sup>C Time Out Interrupt**

The I<sup>2</sup>C Time Out Interrupt operates is contained within the Multi-function Interrupt. An I<sup>2</sup>C Time Out Interrupt request will take place when the I<sup>2</sup>C Time Out Interrupt request flag, I2CTOF, is set, which occurs when an I<sup>2</sup>C time-out counter overflows. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, I<sup>2</sup>C time out interrupt enable bit, I2CTOE, and associated Multi-function interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and an I<sup>2</sup>C time-out counter overflow occurs, a subroutine call to the respective Multi-function Interrupt, will take place. When the I<sup>2</sup>C time out interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the I2CTOF flag will not be automatically cleared, it has to be cleared by the application program.

### **UART Interrupt**

The UART interrupt is contained within the Multi-function Interrupt. Several individual UART conditions can generate a UART interrupt. When these conditions exist, a low pulse will be generated to get the attention of the microcontroller. These conditions are a transmitter data register empty, transmitter idle, receiver data available, receiver overrun, address detect and an RX pin wake-up. To allow the program to branch to the respective interrupt vector addresses, the global interrupt enable bit, EMI, multi-function enable bit, MFnE and UART interrupt enable bit, UIE, must first be set. When the interrupt is enabled, the stack is not full and any of these conditions are created, a subroutine call to the respective Multi-function Interrupt vector, will take place. When the interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, the Multi-function interrupt request flag will be also automatically cleared. However, the USR register flags will be cleared automatically when certain actions are taken by the UART, the details of which are given in the UART section.

### **EEPROM Interrupt**

The EEPROM interrupt is contained within the Multi-function Interrupt. An EEPROM Interrupt request will take place when the EEPROM Interrupt request flag, DEF, is set, which occurs when an EEPROM Write cycle ends. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and EEPROM Interrupt enable bit, DEE, and associated Multi-function interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and an EEPROM Write cycle ends, a subroutine call to the respective EEPROM Interrupt vector will take place. When the EEPROM Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the DEF flag will not be automatically cleared, it has to be cleared by the application program.

### **LVD Interrupt**

The Low Voltage Detector Interrupt is contained within the Multi-function Interrupt. An LVD Interrupt request will take place when the LVD Interrupt request flag, LVF, is set, which occurs when the Low Voltage Detector function detects a low power supply voltage. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, Low Voltage Interrupt enable bit, LVE, and associated Multi-function interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and a low voltage condition occurs, a subroutine call to the Multi-function Interrupt vector, will take place. When the Low Voltage Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the LVF flag will not be automatically cleared, it has to be cleared by the application program.

### **TM Interrupts**

The Compact, Periodic and Standard Type TMs have two interrupts each. All of the TM interrupts are contained within the Multi-function Interrupts. For each of the Compact, Periodic and Standard Type TMs there are two interrupt request flags TnPF and TnAF and two enable bits TnPE and TnAE. A TM interrupt request will take place when any of the TM request flags are set, a situation which occurs when a TM comparator P or A match situation happens.

To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, respective TM Interrupt enable bit, and relevant Multi-function Interrupt enable bit, MFnE, must first be set. When the interrupt is enabled, the stack is not full and a TM comparator match situation occurs, a subroutine call to the relevant Multi-function Interrupt vector locations, will take place. When the TM interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the related MFnF flag will be automatically cleared. As the TM interrupt request flags will not be automatically cleared, they have to be cleared by the application program.

### **Interrupt Wake-up Function**

Each of the interrupt functions has the capability of waking up the microcontroller when in the SLEEP or IDLE Mode. A wake-up is generated when an interrupt request flag changes from low to high and is independent of whether the interrupt is enabled or not. Therefore, even though these devices are in the SLEEP or IDLE Mode and its system oscillator stopped, situations such as external edge transitions on the external interrupt pins, a low power supply voltage or comparator input change may cause their respective interrupt flag to be set high and consequently generate an interrupt. Care must therefore be taken if spurious wake-up situations are to be avoided. If an interrupt wake-up function is to be disabled then the corresponding interrupt request flag should be set high before these devices enter the SLEEP or IDLE Mode. The interrupt enable bits have no effect on the interrupt wake-up function.

## Programming Considerations

By disabling the relevant interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the interrupt register until the corresponding interrupt is serviced or until the request flag is cleared by the application program.

Where a certain interrupt is contained within a Multi-function interrupt, then when the interrupt service routine is executed, as only the Multi-function interrupt request flags, MFnF, will be automatically cleared, the individual request flag for the function needs to be cleared by the application program.

It is recommended that programs do not use the "CALL" instruction within the interrupt service subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a CALL subroutine is executed in the interrupt subroutine.

Every interrupt has the capability of waking up the microcontroller when it is in SLEEP or IDLE Mode, the wake up being generated when the interrupt request flag changes from low to high. If it is required to prevent a certain interrupt from waking up the microcontroller then its respective request flag should be first set high before enter SLEEP or IDLE Mode.

As only the Program Counter is pushed onto the stack, then when the interrupt is serviced, if the contents of the accumulator, status register or other registers are altered by the interrupt service program, their contents should be saved to the memory at the beginning of the interrupt service routine. To return from an interrupt subroutine, either a RET or RETI instruction may be executed. The RETI instruction in addition to executing a return to the main program also automatically sets the EMI bit high to allow further interrupts. The RET instruction however only executes a return to the main program leaving the EMI bit in its present zero state and therefore disabling the execution of further interrupts.

## Low Voltage Detector – LVD

Each device has a Low Voltage Detector function, also known as LVD. This enabled the device to monitor the power supply voltage,  $V_{DD}$ , and provide a warning signal should it fall below a certain level. This function may be especially useful in battery applications where the supply voltage will gradually reduce as the battery ages, as it allows an early warning battery low signal to be generated. The Low Voltage Detector also has the capability of generating an interrupt signal.

### LVD Register

The Low Voltage Detector function is controlled using a single register with the name LVDC. Three bits in this register, VLVD2~VLVD0, are used to select one of eight fixed voltages below which a low voltage condition will be determined. A low voltage condition is indicated when the LVDO bit is set. If the LVDO bit is low, this indicates that the  $V_{DD}$  voltage is above the preset low voltage value. The LVDEN bit is used to control the overall on/off function of the low voltage detector. Setting the bit high will enable the low voltage detector. Clearing the bit to zero will switch off the internal low voltage detector circuits. As the low voltage detector will consume a certain amount of power, it may be desirable to switch off the circuit when not in use, an important consideration in power sensitive battery powered applications.

### LVDC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	LVDO	LVDEN	—	VLVD2	VLVD1	VLVD0
R/W	—	—	R	R/W	—	R/W	R/W	R/W
POR	—	—	0	0	—	0	0	0

Bit 7~6 Unimplemented, read as "0"

Bit 5 **LVDO**: LVD Output Flag  
0: No Low Voltage Detect  
1: Low Voltage Detect

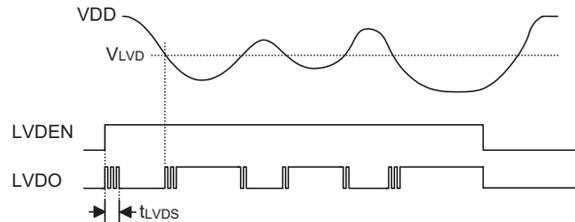
Bit 4 **LVDEN**: Low Voltage Detector Control  
0: Disable  
1: Enable

Bit 3 Unimplemented, read as "0"

Bit 2~0 **VLVD2~VLVD0**: Select LVD Voltage  
000: 2.0V  
001: 2.2V  
010: 2.4V  
011: 2.7V  
100: 3.0V  
101: 3.3V  
110: 3.6V  
111: 4.0V

### LVD Operation

The Low Voltage Detector function operates by comparing the power supply voltage,  $V_{DD}$ , with a pre-specified voltage level stored in the LVDC register. This has a range of between 2.0V and 4.0V. When the power supply voltage,  $V_{DD}$ , falls below this pre-determined value, the LVDO bit will be set high indicating a low power supply voltage condition. The Low Voltage Detector function is supplied by a reference voltage which will be automatically enabled. When these devices are powered down the low voltage detector will remain active if the LVDEN bit is high. After enabling the Low Voltage Detector, a time delay  $t_{LVDS}$  should be allowed for the circuitry to stabilise before reading the LVDO bit. Note also that as the  $V_{DD}$  voltage may rise and fall rather slowly, at the voltage nears that of  $V_{LVD}$ , there may be multiple bit LVDO transitions.



**LVD Operation**

The Low Voltage Detector also has its own interrupt which is contained within one of the Multi-function interrupts, providing an alternative means of low voltage detection, in addition to polling the LVDO bit. The interrupt will only be generated after a delay of  $t_{LVD}$  after the LVDO bit has been set high by a low voltage condition. When the devices are powered down the Low Voltage Detector will remain active if the LVDEN bit is high. In this case, the LVF interrupt request flag will be set, causing an interrupt to be generated if  $V_{DD}$  falls below the preset LVD voltage. This will cause the devices to wake-up from the SLEEP or IDLE Mode, however if the Low Voltage Detector wake up function is not required then the LVF flag should be first set high before the devices enter the SLEEP or IDLE Mode.

When LVD function is enabled, it is recommended to clear LVD flag first, and then enables interrupt function to avoid mistake action.

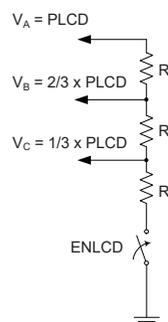
## LCD Driver

For large volume applications, which incorporate an LCD in their design, the use of a custom display rather than a more expensive character based display reduces costs significantly. However, the corresponding COM and SEG signals required, which vary in both amplitude and time, to drive such a custom display require many special considerations for proper LCD operation to occur. These devices contain an LCD Driver function, which with their internal LCD signal generating circuitry and various options will automatically generate these time and amplitude varying signals to provide a means of direct driving and easy interfacing to a range of custom LCDs.

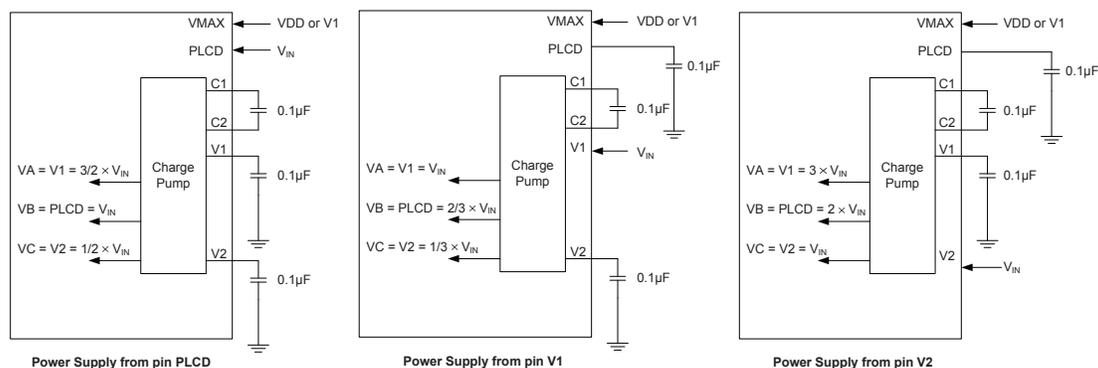
These devices include a wide range of options to enable LCD displays of various types to be driven. The table shows the range of options available across the device range.

Device	Driver No.	Bias	Duty	Bias Type	Wave Type
HT67F5650	40×4	1/3	1/4	R or C	A or B
HT67F5660	48×4	1/3	1/4	R or C	A or B

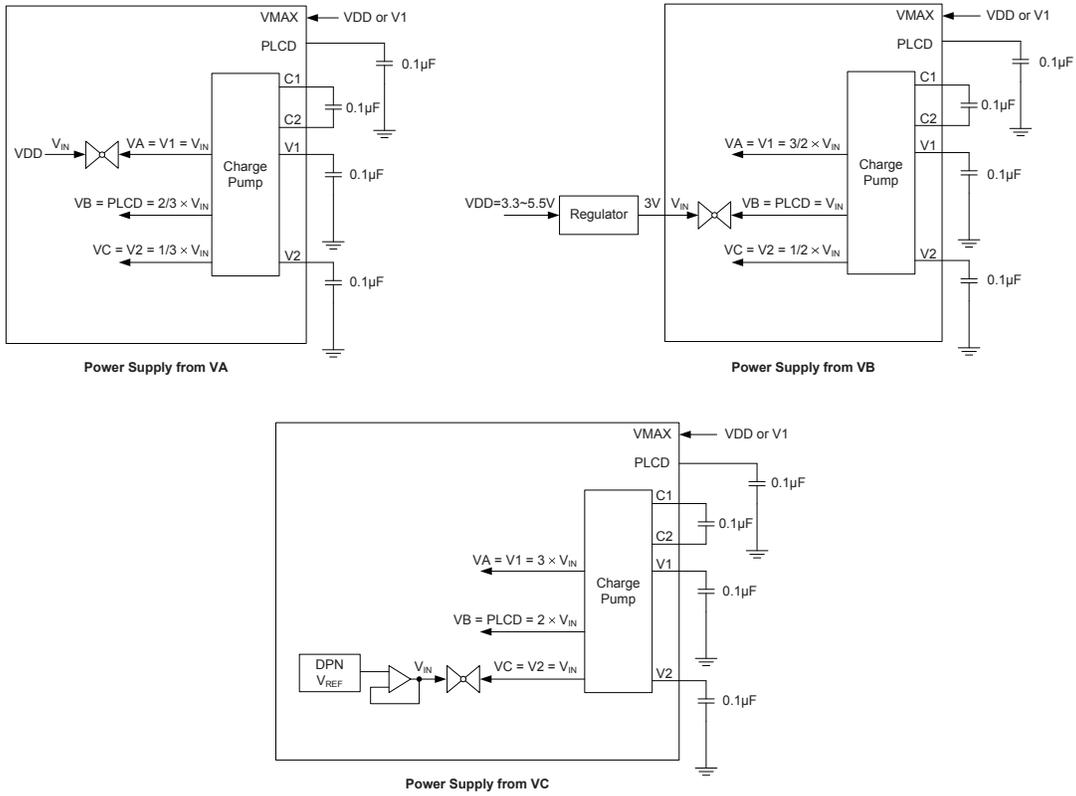
### LCD Selections



### R Type 1/3 Bias Voltage Levels



### LCD Power Source from External Pin for C1 Type



**LCD Power Source from Internal Power for C2 Type**

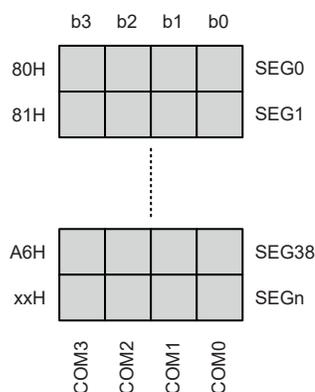
Note: The pin  $V_{MAX}$  must connect to maximum voltage to prevent pad leakage.

## LCD Display Memory

An area of Data Memory is especially reserved for use for the LCD display data. This data area is known as the LCD Memory. Any data written here will be automatically read by the internal display driver circuits, which will in turn automatically generate the necessary LCD driving signals. Therefore any data written into this Memory will be immediately reflected into the actual display connected to the microcontroller.

These devices provide an area of embedded data memory for the LCD display. This area is located at 80H to A7H in Sector 1 of the Data Memory for the HT67F5650 and 80H to AFH in Sector 1 of the Data Memory for the HT67F5660. To access the Display Memory therefore requires first that Sector 1 is selected by writing a value of 01H to MP1H or MP2H. After this, the memory can then be accessed by using indirect addressing through the use of MP1L or MP2L. With Sector 1 selected, then using MP1L/MP2L to read or write to the memory area, from 80H to A7H or 80H to AFH, will result in operations to the LCD memory. Directly addressing the Display Memory is not applicable and will result in a data access to the Sector 0 General Purpose Data Memory.

The LCD display memory can be read and written to only by indirect addressing mode using MP1L/MP1H and MP2L/MP2H. When data is written into the display data area, it is automatically read by the LCD driver which then generates the corresponding LCD driving signals. To turn the display on or off, a "1" or a "0" is written to the corresponding bit of the display memory, respectively. The figure illustrates the mapping between the display memory and LCD pattern for the devices.



Note: For HT67F5650, xxH=A7H and SEGn=SEG39;  
For HT67F5660, xxH=AFH and SEGn=SEG47.

LCD Memory Map

## LCD Clock Source

The LCD clock source is the internal clock signal,  $f_{SUB}$ , divided by 8, using an internal divider circuit. The  $f_{SUB}$  internal clock is supplied by either the LIRC or LXT oscillator, the choice of which is determined by a configuration option. For proper LCD operation, this arrangement is provided to generate an ideal LCD clock source frequency of 4kHz.

$f_{SUB}$ Clock Source	LCD Clock Frequency
LIRC	4kHz
LXT	4kHz

LCD Clock Source

## LCD Registers

Control Registers in the Data Memory, are used to control the various setup features of the LCD Driver. There are several control registers for the LCD function, LCDCP, LCDC, LCD1, LCD2 and LCD3 for the HT67F5650 device and LCDCP, LCDC, LCD1, LCD2, LCD3 and LCD4 for the HT67F5660 device.

The LCDPR bit in the LCDCP register is used to select the PLCD pin or the internal charge pump regulator to supply the power for the R type LCD COMs and SEGs pins. Bits CPVS1 and CPVS0 in the same register are used to select an appropriate charge pump output voltage level.

Various bits in the LCDC register control functions such as waveform type, power source selection and overall LCD enable/disable. The TYPE bit in the LCDC register is used to select whether Type A or Type B LCD control signals are used. The RCT bit in the LCDC register is used to select whether R type or C type LCD drive bias. Bits LCDP1 and LCDP0 in the LCDC register are used to select the power source to supply the LCD panel with the correct bias voltages. Bits LCDIS0 and LCDIS1 in the LCDC register are used to select the internal bias current to supply the LCD panel with the correct bias voltages. A choice to best match the LCD panel used in the application can be selected also to minimise bias current. The ENLCD bit in the LCDC register, which provides the overall LCD enable/disable function, will only be effective when these devices are in the Normal, Slow or Idle Mode. If these devices are in the Sleep Mode then the display will always be disabled.

Registers LCD1~LCD4 are used to determine if the output function of display pins SEG0~SEG15, SEG38~SEG39 for the HT67F5650 device and SEG0~SEG15, SEG38~SEG47 for the HT67F5660 device are used as segment drivers or I/O functions.

### LCDCP Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	LCDPR	—	CPVS1	CPVS0
R/W	—	—	—	—	R/W	—	R/W	R/W
POR	—	—	—	—	0	—	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3 **LCDPR**: LCD Power selection for R type  
0: PLCD pin  
1: Internal charge pump

Bit 2 Unimplemented, read as "0"

Bit 1~0 **CPVS1~CPVS0**: Charge pump output voltage selection  
00: 3.3V  
01: 3.0V  
10: 2.7V  
11: 4.5V

**LCDC Register**

Bit	7	6	5	4	3	2	1	0
Name	TYPE	RCT	LCDP1	LCDP0	—	LCDIS1	LCDIS0	ENLCD
R/W	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W
POR	0	0	0	0	—	0	0	0

- Bit 7     **TYPE**: LCD Waveform Type Control  
0: Type A  
1: Type B
- Bit 6     **RCT**: R/C LCD Type Control  
0: R type  
1: C type
- Bit 5~4   **LCDP1~LCDP0**: LCD power source select for C type  
00: The power source is from PLCD/V1/V2  
01: The power source is from  $V_C = \text{DPN } V_{\text{REF}} (\sim 1.08\text{V})$   
10: The power source is from  $V_B = 3\text{V}$   
11: The power source is from  $V_A = V_{\text{DD}}$
- Bit 3     Unimplemented, read as "0"
- Bit 2~1   **LCDIS1~LCDIS0**: LCD Bias Current Select  
00: 25 $\mu\text{A}$   
01: 50 $\mu\text{A}$   
10: 100 $\mu\text{A}$   
11: 200 $\mu\text{A}$
- Bit 0     **ENLCD**: LCD Enable Control  
0: Disable  
1: Enable

**LCD1 Register**

Bit	7	6	5	4	3	2	1	0
Name	LCDS7	LCDS6	LCDS5	LCDS4	LCDS3	LCDS2	LCDS1	LCDS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7     **LCDS7**: SEG7 Output Control  
0: Disable  
1: Enable
- Bit 6     **LCDS6**: SEG6 Output Control  
0: Disable  
1: Enable
- Bit 5     **LCDS5**: SEG5 Output Control  
0: Disable  
1: Enable
- Bit 4     **LCDS4**: SEG4 Output Control  
0: Disable  
1: Enable
- Bit 3     **LCDS3**: SEG3 Output Control  
0: Disable  
1: Enable
- Bit 2     **LCDS2**: SEG2 Output Control  
0: Disable  
1: Enable
- Bit 1     **LCDS1**: SEG1 Output Control  
0: Disable  
1: Enable
- Bit 0     **LCDS0**: SEG0 Output Control  
0: Disable  
1: Enable

**LCD2 Register**

Bit	7	6	5	4	3	2	1	0
Name	LCDS15	LCDS14	LCDS13	LCDS12	LCDS11	LCDS10	LCDS9	LCDS8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7      **LCDS15:** SEG15 Output Control  
0: Disable  
1: Enable
- Bit 6      **LCDS14:** SEG14 Output Control  
0: Disable  
1: Enable
- Bit 5      **LCDS13:** SEG13 Output Control  
0: Disable  
1: Enable
- Bit 4      **LCDS12:** SEG12 Output Control  
0: Disable  
1: Enable
- Bit 3      **LCDS11:** SEG11 Output Control  
0: Disable  
1: Enable
- Bit 2      **LCDS10:** SEG10 Output Control  
0: Disable  
1: Enable
- Bit 1      **LCDS9:** SEG9 Output Control  
0: Disable  
1: Enable
- Bit 0      **LCDS8:** SEG8 Output Control  
0: Disable  
1: Enable

**LCD3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	LCDS39	LCDS38
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

- Bit 7~2    Unimplemented, read as "0"
- Bit 1      **LCDS39:** SEG39 Output Control  
0: Disable  
1: Enable
- Bit 0      **LCDS38:** SEG38 Output Control  
0: Disable  
1: Enable

**LCD4 Register – HT67F5660**

Bit	7	6	5	4	3	2	1	0
Name	LCDS47	LCDS46	LCDS45	LCDS44	LCDS43	LCDS42	LCDS41	LCDS40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

- Bit 7      **LCDS47:** SEG47 Output Control  
             0: Disable  
             1: Enable
- Bit 6      **LCDS46:** SEG46 Output Control  
             0: Disable  
             1: Enable
- Bit 5      **LCDS45:** SEG45 Output Control  
             0: Disable  
             1: Enable
- Bit 4      **LCDS44:** SEG44 Output Control  
             0: Disable  
             1: Enable
- Bit 3      **LCDS43:** SEG43 Output Control  
             0: Disable  
             1: Enable
- Bit 2      **LCDS42:** SEG42 Output Control  
             0: Disable  
             1: Enable
- Bit 1      **LCDS41:** SEG41 Output Control  
             0: Disable  
             1: Enable
- Bit 0      **LCDS40:** SEG40 Output Control  
             0: Disable  
             1: Enable

**LCD Voltage Source and Biasing**

The time and amplitude varying signals generated by the LCD Driver function require the generation of several voltage levels for their operation. The devices can have either R type or C type biasing selected via a software control bit named RCT. Selecting the C type biasing will enable an internal charge pump circuitry.

**R Type Biasing**

For R type biasing the LCD voltage source, the PLCD voltage can be supplied by the PLCD pin or internal charge pump regulator, selected by the LCDPR bit in the LCDCP register, to generate the internal biasing voltages. The source on the PLCD pin could be the microcontroller power supply or some other voltage source. Note that the PLCD voltage should be equal or less than  $V_{DD}$ . There are four kinds of the internal charge pump voltage output, managed by the CPVS[1:0] bits in the LCDCP register.

For the R type 1/3 bias scheme, four voltage levels  $V_{SS}$ ,  $V_A$ ,  $V_B$  and  $V_C$  are utilised. The voltage  $V_A$  is equal to PLCD. The voltage  $V_B$  is equal to  $PLCD \times 2/3$  while the voltage  $V_C$  is equal to  $PLCD \times 1/3$ .

Different values of internal bias current can be selected using the LCDIS1~LCDIS0 bits in the LCDC register. The connection to the VMAX pin depends upon the voltage that is applied to the PLCD pin. If the VDD voltage is greater than or equal to the voltage applied to the PLCD pin then the VMAX pin should be connected to VDD. Note that for R type biasing the voltage on the PLCD pin should not be greater than the VDD pin voltage. Note that no external capacitors or resistors are required to be connected if R type biasing is used.

Condition	VMAX Connection
$V_{DD} \geq PLCD$	Connect VMAX to VDD
$V_{DD} < PLCD$	Forbidden condition

**R Type Bias VMAX Pin Connection**

### C Type Biasing

For C type biasing the devices can have either external pin or internal power source selected via by register bits LCDP1~LCDP0, LCD voltage source is supplied on external pin PLCD, V1, V2 (LCDP[1:0]=00) or internal power (LCDP[1:0]=01, 10 or 11) to generate the internal biasing voltages.

When power source is from pin PLCD, The C type biasing scheme uses an internal charge pump circuit, which can generate voltages higher than what is supplied on PLCD. This feature is useful in applications where the microcontroller supply voltage is less than the supply voltage required by the LCD. An additional charge pump capacitor must also be connected between pins C1 and C2 to generate the necessary voltage levels.

Four voltage levels  $V_{SS}$ ,  $V_A$ ,  $V_B$  and  $V_C$  are utilized.

These devices have an integrated depletion circuit for LCD voltage source. This could be the DPN  $V_{REF}$  (~1.08V), a fixed 3V voltage generated by an additional regulator or internal power  $V_{DD}$  to generate biasing voltage when bits LCDP1~LCDP0 are configured 01, 10 or 11.

When power source is from pin V1 or  $V_A$  ( $V_A=V_{DD}$ ), which is maximum bias. The pin PLCD must connect a 0.1 $\mu$ F to ground. The voltage  $V_A$  will have a value equal to V1 or  $V_{DD}$ .  $V_B$  will have a value equal to  $V_A \times 2/3$  and  $V_C$  will have a value equal to  $V_A \times 1/3$ .

When power source is from pin PLCD or  $V_B$  ( $V_B=$ Regulator Output 3V), the voltage  $V_A$  is generated internally and has a value of  $PLCD \times 1.5$  or  $3V \times 3/2$ .  $V_B$  will have a value equal to  $V_A \times 2/3$  and  $V_C$  will have a value equal to  $V_A \times 1/3$ .

When power source is from pin V2 or  $V_C$  ( $V_C=$ DPN  $V_{REF}$ ), the voltage  $V_A$  is generated internally and has a value of  $V2 \times 3$  or  $DPN V_{REF} \times 3$ .  $V_B$  will have a value equal to  $V_A \times 2/3$  and  $V_C$  will have a value equal to  $V_A \times 1/3$ .

The connection to the VMAX pin depends upon the bias and the voltage that is applied to the PLCD pin, the details are shown in the table. It is extremely important to ensure that these charge pump generated internal voltages do not exceed the maximum  $V_{DD}$  voltage of 5.5V.

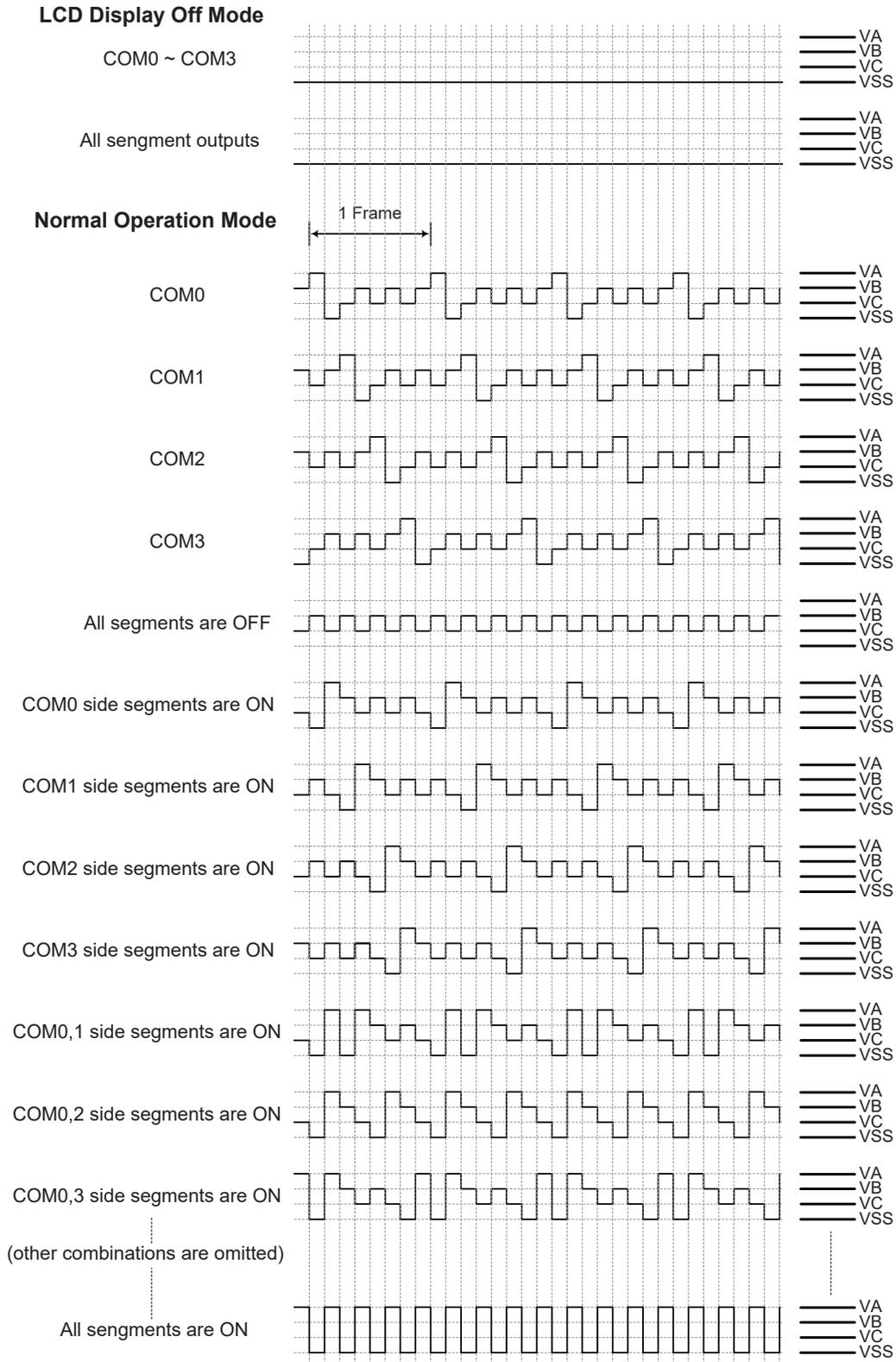
Condition	VMAX Connection
$V_{DD} > PLCD \times 1.5$	Connect VMAX to VDD
Otherwise	Connect VMAX to V1

## **LCD Driver Output**

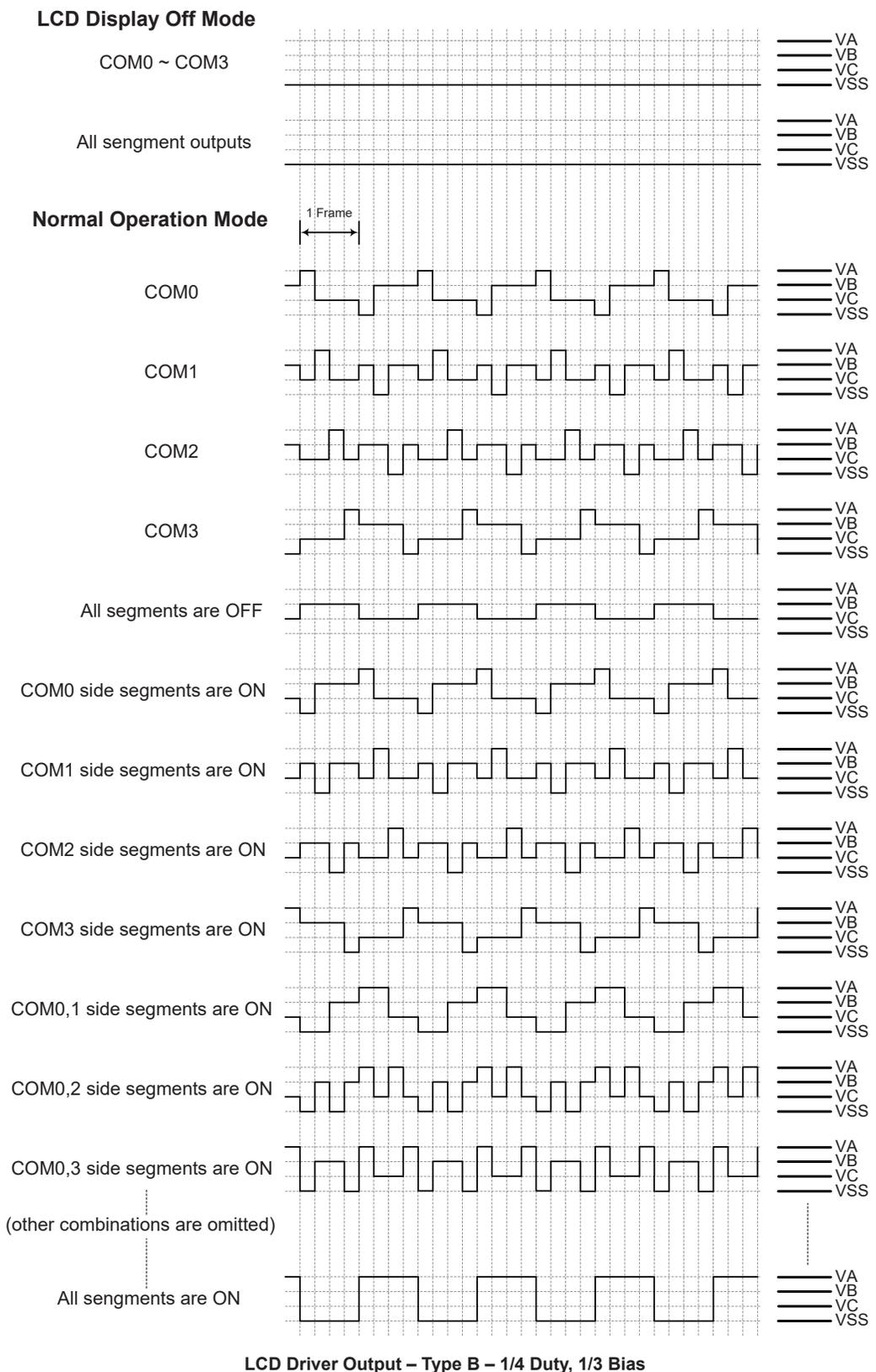
The number of COM and SEG outputs supplied by the LCD driver, as well as its biasing and wave type selections, are dependent upon how the LCD control bits are programmed. The Bias Type, whether C or R type is also selected by a software control bit.

The nature of Liquid Crystal Displays require that only AC voltages can be applied to their pixels as the application of DC voltages to LCD pixels may cause permanent damage. For this reason the relative contrast of an LCD display is controlled by the actual RMS voltage applied to each pixel, which is equal to the RMS value of the voltage on the COM pin minus the voltage applied to the SEG pin. This differential RMS voltage must be greater than the LCD saturation voltage for the pixel to be on and less than the threshold voltage for the pixel to be off.

The requirement to limit the DC voltage to zero and to control as many pixels as possible with a minimum number of connections requires that both a time and amplitude signal is generated and applied to the application LCD. These time and amplitude varying signals are automatically generated by the LCD driver circuits in the microcontroller. What is known as the duty determines the number of common lines used, which are also known as backplanes or COMs. The duty is 1/4 and equates to a COM number of 4, therefore defines the number of time divisions within each LCD signal frame. Two types of signal generation are also provided, known as Type A and Type B, the required type is selected via the TYPE bit in the LCDC register. Type B offers lower frequency signals, however lower frequencies may introduce flickering and influence display clarity.



**LCD Driver Output – Type A – 1/4 Duty, 1/3 Bias**



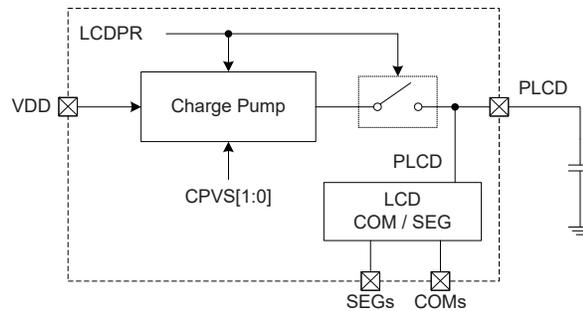
**LCD Driver Output – Type B – 1/4 Duty, 1/3 Bias**

### LCD Charge Pump

The COMs and SEGs pins can be powered up by the external PLCD pin or internal charge pump circuit which is determined by the LCDPR bit in the LCDCP register. When the LCDPR bit is set low, the LCD driver power is supplied by the external PLCD pin. The PLCD pin voltage should be equal to or less than  $V_{DD}$  if the PLCD pin is selected to be used. If the LCDPR bit is set high, the LCD driver power is supplied by the internal charge pump circuit. There are four charge pump output voltage levels which are selected by the CPVS1~CPVS0 bits in the LCDCP register. If the internal charge pump circuit is used, an external 4.7 $\mu$ F capacitor should be connected to the external PLCD pin for output voltage stability. Note that there is also a relationship between the selected charge pump output voltage and  $V_{DD}$  when the internal charge pump circuit is used. In addition, for C type the LCDPR bit should be fixed at low.

LCDPR	LCD Driver Power Supply	Relationship
0	PLCD pin	$PLCD \leq V_{DD}$
1	Charge Pump Circuit	$PLCD \leq V_{DD} + 0.7V$

**LCD Driver Power Supply Relationship**



**LCD Driver Charge Pump Circuit**

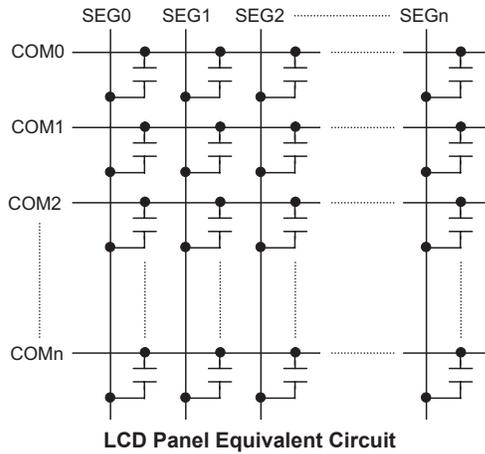
## Programming Considerations

Certain precautions must be taken when programming the LCD. One of these is to ensure that the LCD Memory is properly initialised after the microcontroller is powered on. Like the General Purpose Data Memory, the contents of the LCD Memory are in an unknown condition after power-on. As the contents of the LCD Memory will be mapped into the actual display, it is important to initialise this memory area into a known condition soon after applying power to obtain a proper display pattern.

Consideration must also be given to the capacitive load of the actual LCD used in the application. As the load presented to the microcontroller by LCD pixels can be generally modeled as mainly capacitive in nature, it is important that this is not excessive, a point that is particularly true in the case of the COM lines which may be connected to many LCD pixels. The accompanying diagram depicts the equivalent circuit of the LCD.

One additional consideration that must be taken into account is what happens when the microcontroller enters the Idle or Slow Mode. The ENLCD control bit in the LCDC register permits the display to be powered off to reduce power consumption. If this bit is zero, the driving signals to the display will cease, producing a blank display pattern but reducing any power consumption associated with the LCD.

After Power-on, note that as the ENLCD bit will be cleared to zero, the display function will be disabled.

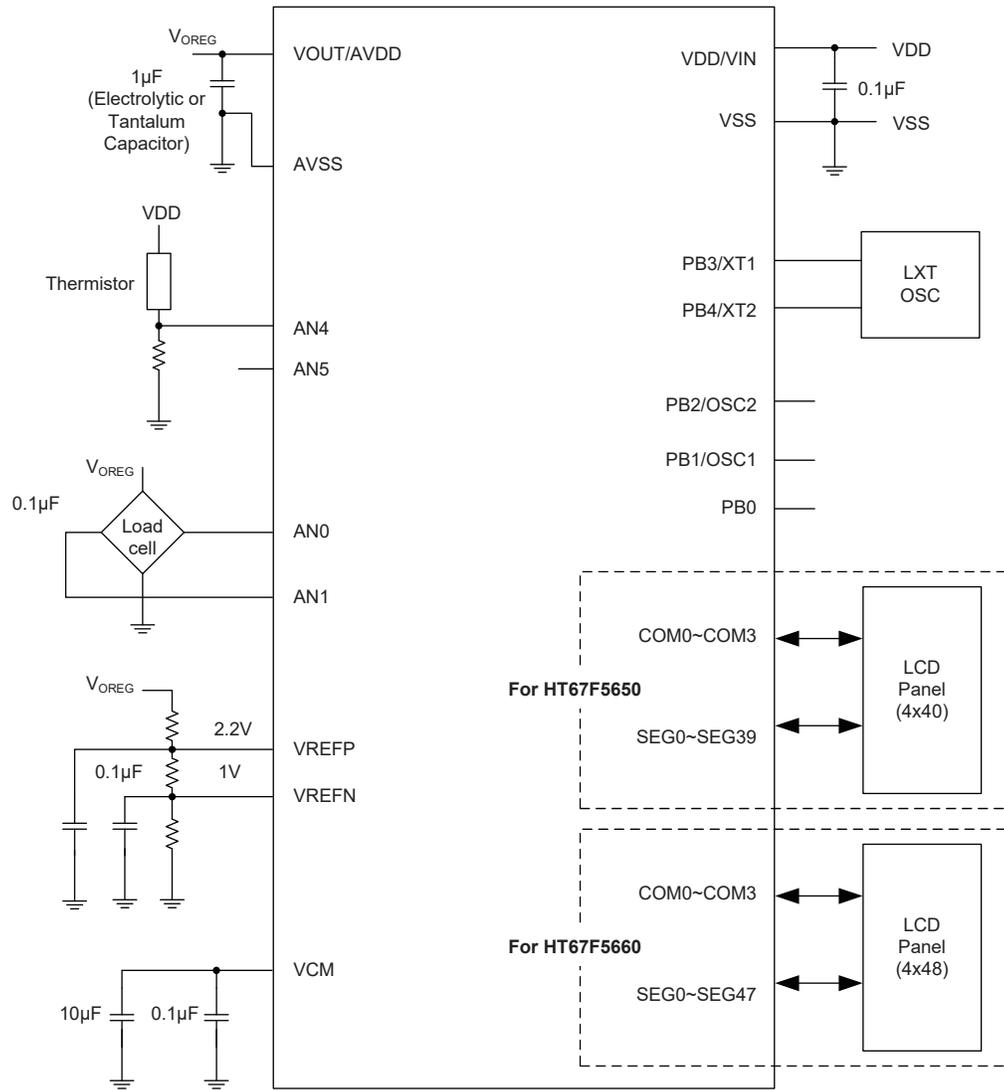


## Configuration Option

Configuration options refer to certain options within the MCU that are programmed into the devices during the programming process. During the development process, these options are selected using the HT-IDE software development tools. As these options are programmed into the devices using the hardware programming tools, once they are selected they cannot be changed later using the application program. All options must be defined for proper system function, the details of which are shown in the table.

No.	Options
<b>Oscillator Options</b>	
1	High Speed System Oscillator Selection – $f_H$ : 1. HXT 2. HIRC
2	HIRC Frequency Selection: 1. 4.9152MHz 2. 9.8304MHz 3. 14.7456MHz
3	Low Speed System Oscillator Selection – $f_{SUB}$ : 1. LXT 2. LIRC
<b>Watchdog Timer Options</b>	
4	WDT function: 1. Always enable 2. Controlled by WDT Control Register
5	WDT Clock Selection – $f_s$ : 1. $f_{SUB}$ 2. $f_{SYS}/4$

**Application Circuits**



## Instruction Set

### Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontroller, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

### Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5 $\mu$ s and branch or call instructions would be implemented within 1 $\mu$ s. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be "CLR PCL" or "MOV PCL, A". For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

### Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

### Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

## Logical and Rotate Operation

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one Bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry Bit from where it can be examined and the necessary serial Bit set high or low. Another application which rotate data operations are used is to implement multiplication and division calculations.

## Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction "RET" in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual Bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data Bits.

## Bit Operations

The ability to provide single Bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port Bit programming where individual Bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-Bit output port, manipulate the input data to ensure that other Bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these Bit operation instructions are used.

## Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be set as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

## Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

## Instruction Set Summary

The instructions related to the data memory access in the following table can be used when the desired data memory is located in Data Memory sector 0.

### Table Conventions

x: Bits immediate data  
 m: Data Memory address  
 A: Accumulator  
 i: 0~7 number of bits  
 addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
<b>Arithmetic</b>			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV, SC
ADDM A,[m]	Add ACC to Data Memory	1 <sup>Note</sup>	Z, C, AC, OV, SC
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV, SC
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV, SC
ADCM A,[m]	Add ACC to Data memory with Carry	1 <sup>Note</sup>	Z, C, AC, OV, SC
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV, SC, CZ
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV, SC, CZ
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	1 <sup>Note</sup>	Z, C, AC, OV, SC, CZ
SBC A,x	Subtract immediate data from ACC with Carry	1	Z, C, AC, OV, SC, CZ
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV, SC, CZ
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	1 <sup>Note</sup>	Z, C, AC, OV, SC, CZ
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	1 <sup>Note</sup>	C
<b>Logic Operation</b>			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	1 <sup>Note</sup>	Z
ORM A,[m]	Logical OR ACC to Data Memory	1 <sup>Note</sup>	Z
XORM A,[m]	Logical XOR ACC to Data Memory	1 <sup>Note</sup>	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	1 <sup>Note</sup>	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
<b>Increment &amp; Decrement</b>			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	1 <sup>Note</sup>	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	1 <sup>Note</sup>	Z
<b>Rotate</b>			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	1 <sup>Note</sup>	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	1 <sup>Note</sup>	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	1 <sup>Note</sup>	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	1 <sup>Note</sup>	C

Mnemonic	Description	Cycles	Flag Affected
<b>Data Move</b>			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	1 <sup>Note</sup>	None
MOV A,x	Move immediate data to ACC	1	None
<b>Bit Operation</b>			
CLR [m].i	Clear bit of Data Memory	1 <sup>Note</sup>	None
SET [m].i	Set bit of Data Memory	1 <sup>Note</sup>	None
<b>Branch Operation</b>			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	1 <sup>Note</sup>	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	1 <sup>Note</sup>	None
SZ [m].i	Skip if bit i of Data Memory is zero	1 <sup>Note</sup>	None
SNZ [m]	Skip if Data Memory is not zero	1 <sup>Note</sup>	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	1 <sup>Note</sup>	None
SIZ [m]	Skip if increment Data Memory is zero	1 <sup>Note</sup>	None
SDZ [m]	Skip if decrement Data Memory is zero	1 <sup>Note</sup>	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	1 <sup>Note</sup>	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	1 <sup>Note</sup>	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
<b>Table Read Operation</b>			
TABRD [m]	Read table (specific page) to TBLH and Data Memory	2 <sup>Note</sup>	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2 <sup>Note</sup>	None
ITABRD [m]	Increment table pointer TBLP first and Read table to TBLH and Data Memory	2 <sup>Note</sup>	None
ITABRDL [m]	Increment table pointer TBLP first and Read table (last page) to TBLH and Data Memory	2 <sup>Note</sup>	None
<b>Miscellaneous</b>			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	1 <sup>Note</sup>	None
SET [m]	Set Data Memory	1 <sup>Note</sup>	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	1 <sup>Note</sup>	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then up to three cycles are required, if no skip takes place only one cycle is required.

2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.

3. For the "CLR WDT" instruction the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after the "CLR WDT" instructions is executed. Otherwise the TO and PDF flags remain unchanged.

### Extended Instruction Set

The extended instructions are used to support the full range address access for the data memory. When the accessed data memory is located in any data memory sections except sector 0, the extended instruction can be used to access the data memory instead of using the indirect addressing access to improve the CPU firmware performance.

Mnemonic	Description	Cycles	Flag Affected
<b>Arithmetic</b>			
LADD A,[m]	Add Data Memory to ACC	2	Z, C, AC, OV, SC
LADDM A,[m]	Add ACC to Data Memory	2 <sup>Note</sup>	Z, C, AC, OV, SC
LADC A,[m]	Add Data Memory to ACC with Carry	2	Z, C, AC, OV, SC
LADCM A,[m]	Add ACC to Data memory with Carry	2 <sup>Note</sup>	Z, C, AC, OV, SC
LSUB A,[m]	Subtract Data Memory from ACC	2	Z, C, AC, OV, SC, CZ
LSUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	2 <sup>Note</sup>	Z, C, AC, OV, SC, CZ
LSBC A,[m]	Subtract Data Memory from ACC with Carry	2	Z, C, AC, OV, SC, CZ
LSBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	2 <sup>Note</sup>	Z, C, AC, OV, SC, CZ
LDAA [m]	Decimal adjust ACC for Addition with result in Data Memory	2 <sup>Note</sup>	C
<b>Logic Operation</b>			
LAND A,[m]	Logical AND Data Memory to ACC	2	Z
LOR A,[m]	Logical OR Data Memory to ACC	2	Z
LXOR A,[m]	Logical XOR Data Memory to ACC	2	Z
LANDM A,[m]	Logical AND ACC to Data Memory	2 <sup>Note</sup>	Z
LORM A,[m]	Logical OR ACC to Data Memory	2 <sup>Note</sup>	Z
LXORM A,[m]	Logical XOR ACC to Data Memory	2 <sup>Note</sup>	Z
LCPL [m]	Complement Data Memory	2 <sup>Note</sup>	Z
LCPLA [m]	Complement Data Memory with result in ACC	2	Z
<b>Increment &amp; Decrement</b>			
LINCA [m]	Increment Data Memory with result in ACC	2	Z
LINC [m]	Increment Data Memory	2 <sup>Note</sup>	Z
LDECA [m]	Decrement Data Memory with result in ACC	2	Z
LDEC [m]	Decrement Data Memory	2 <sup>Note</sup>	Z
<b>Rotate</b>			
LRR A,[m]	Rotate Data Memory right with result in ACC	2	None
LRR [m]	Rotate Data Memory right	2 <sup>Note</sup>	None
LRRCA [m]	Rotate Data Memory right through Carry with result in ACC	2	C
LRRC [m]	Rotate Data Memory right through Carry	2 <sup>Note</sup>	C
LRL A,[m]	Rotate Data Memory left with result in ACC	2	None
LRL [m]	Rotate Data Memory left	2 <sup>Note</sup>	None
LRLCA [m]	Rotate Data Memory left through Carry with result in ACC	2	C
LRLC [m]	Rotate Data Memory left through Carry	2 <sup>Note</sup>	C
<b>Data Move</b>			
LMOV A,[m]	Move Data Memory to ACC	2	None
LMOV [m],A	Move ACC to Data Memory	2 <sup>Note</sup>	None
<b>Bit Operation</b>			
LCLR [m].i	Clear bit of Data Memory	2 <sup>Note</sup>	None
LSET [m].i	Set bit of Data Memory	2 <sup>Note</sup>	None

Mnemonic	Description	Cycles	Flag Affected
<b>Branch</b>			
LSZ [m]	Skip if Data Memory is zero	2 <sup>Note</sup>	None
LSZA [m]	Skip if Data Memory is zero with data movement to ACC	2 <sup>Note</sup>	None
LSNZ [m]	Skip if Data Memory is not zero	2 <sup>Note</sup>	None
LSZ [m].i	Skip if bit i of Data Memory is zero	2 <sup>Note</sup>	None
LSNZ [m].i	Skip if bit i of Data Memory is not zero	2 <sup>Note</sup>	None
LSIZ [m]	Skip if increment Data Memory is zero	2 <sup>Note</sup>	None
LSDZ [m]	Skip if decrement Data Memory is zero	2 <sup>Note</sup>	None
LSIZA [m]	Skip if increment Data Memory is zero with result in ACC	2 <sup>Note</sup>	None
LSDZA [m]	Skip if decrement Data Memory is zero with result in ACC	2 <sup>Note</sup>	None
<b>Table Read</b>			
LTABRD [m]	Read table to TBLH and Data Memory	3 <sup>Note</sup>	None
LTABRDL [m]	Read table (last page) to TBLH and Data Memory	3 <sup>Note</sup>	None
LITABRD [m]	Increment table pointer TBLP first and Read table to TBLH and Data Memory	3 <sup>Note</sup>	None
LITABRDL [m]	Increment table pointer TBLP first and Read table (last page) to TBLH and Data Memory	3 <sup>Note</sup>	None
<b>Miscellaneous</b>			
LCLR [m]	Clear Data Memory	2 <sup>Note</sup>	None
LSET [m]	Set Data Memory	2 <sup>Note</sup>	None
LSWAP [m]	Swap nibbles of Data Memory	2 <sup>Note</sup>	None
LSWAPA [m]	Swap nibbles of Data Memory with result in ACC	2	None

Note: 1. For these extended skip instructions, if the result of the comparison involves a skip then up to four cycles are required, if no skip takes place two cycles is required.

2. Any extended instruction which changes the contents of the PCL register will also require three cycles for execution.

## Instruction Definition

<b>ADC A,[m]</b>	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC
<b>ADCM A,[m]</b>	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC
<b>ADD A,[m]</b>	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC
<b>ADD A,x</b>	Add immediate data to ACC
Description	The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + x$
Affected flag(s)	OV, Z, AC, C, SC
<b>ADDM A,[m]</b>	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC
<b>AND A,[m]</b>	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "AND" } [m]$
Affected flag(s)	Z
<b>AND A,x</b>	Logical AND immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bit wise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "AND" } x$
Affected flag(s)	Z
<b>ANDM A,[m]</b>	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \text{ "AND" } [m]$
Affected flag(s)	Z

<b>CALL addr</b>	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack ← Program Counter + 1 Program Counter ← addr
Affected flag(s)	None
<b>CLR [m]</b>	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] ← 00H
Affected flag(s)	None
<b>CLR [m].i</b>	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i ← 0
Affected flag(s)	None
<b>CLR WDT</b>	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF
<b>CPL [m]</b>	Complement Data Memory
Description	Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa.
Operation	[m] ← $\overline{[m]}$
Affected flag(s)	Z
<b>CPLA [m]</b>	Complement Data Memory with result in ACC
Description	Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC ← $\overline{[m]}$
Affected flag(s)	Z
<b>DAA [m]</b>	Decimal-Adjust ACC for addition with result in Data Memory
Description	Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.
Operation	[m] ← ACC + 00H or [m] ← ACC + 06H or [m] ← ACC + 60H or [m] ← ACC + 66H
Affected flag(s)	C

<b>DEC [m]</b>	Decrement Data Memory
Description	Data in the specified Data Memory is decremented by 1.
Operation	$[m] \leftarrow [m] - 1$
Affected flag(s)	Z
<b>DECA [m]</b>	Decrement Data Memory with result in ACC
Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] - 1$
Affected flag(s)	Z
<b>HALT</b>	Enter power down mode
Description	This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.
Operation	$TO \leftarrow 0$ $PDF \leftarrow 1$
Affected flag(s)	TO, PDF
<b>INC [m]</b>	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	$[m] \leftarrow [m] + 1$
Affected flag(s)	Z
<b>INCA [m]</b>	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] + 1$
Affected flag(s)	Z
<b>JMP addr</b>	Jump unconditionally
Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	Program Counter $\leftarrow$ addr
Affected flag(s)	None
<b>MOV A,[m]</b>	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	$ACC \leftarrow [m]$
Affected flag(s)	None
<b>MOV A,x</b>	Move immediate data to ACC
Description	The immediate data specified is loaded into the Accumulator.
Operation	$ACC \leftarrow x$
Affected flag(s)	None
<b>MOV [m],A</b>	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	$[m] \leftarrow ACC$
Affected flag(s)	None

<b>NOP</b>	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None
<b>OR A,[m]</b>	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "OR" [m]
Affected flag(s)	Z
<b>OR A,x</b>	Logical OR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "OR" x
Affected flag(s)	Z
<b>ORM A,[m]</b>	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "OR" [m]
Affected flag(s)	Z
<b>RET</b>	Return from subroutine
Description	The Program Counter is restored from the stack. Program execution continues at the restored address.
Operation	Program Counter ← Stack
Affected flag(s)	None
<b>RET A,x</b>	Return from subroutine and load immediate data to ACC
Description	The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.
Operation	Program Counter ← Stack ACC ← x
Affected flag(s)	None
<b>RETI</b>	Return from interrupt
Description	The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.
Operation	Program Counter ← Stack EMI ← 1
Affected flag(s)	None
<b>RL [m]</b>	Rotate Data Memory left
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i=0~6) [m].0 ← [m].7
Affected flag(s)	None

<b>RLA [m]</b>	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.(i+1) \leftarrow [m].i; (i=0\sim6)$ $ACC.0 \leftarrow [m].7$
Affected flag(s)	None
<b>RLC [m]</b>	Rotate Data Memory left through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.
Operation	$[m].(i+1) \leftarrow [m].i; (i=0\sim6)$ $[m].0 \leftarrow C$ $C \leftarrow [m].7$
Affected flag(s)	C
<b>RLCA [m]</b>	Rotate Data Memory left through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.(i+1) \leftarrow [m].i; (i=0\sim6)$ $ACC.0 \leftarrow C$ $C \leftarrow [m].7$
Affected flag(s)	C
<b>RR [m]</b>	Rotate Data Memory right
Description	The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.
Operation	$[m].i \leftarrow [m].(i+1); (i=0\sim6)$ $[m].7 \leftarrow [m].0$
Affected flag(s)	None
<b>RRA [m]</b>	Rotate Data Memory right with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.i \leftarrow [m].(i+1); (i=0\sim6)$ $ACC.7 \leftarrow [m].0$
Affected flag(s)	None
<b>RRC [m]</b>	Rotate Data Memory right through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.
Operation	$[m].i \leftarrow [m].(i+1); (i=0\sim6)$ $[m].7 \leftarrow C$ $C \leftarrow [m].0$
Affected flag(s)	C

<b>RRCA [m]</b>	Rotate Data Memory right through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.i ← [m].(i+1); (i=0~6) ACC.7 ← C C ← [m].0
Affected flag(s)	C
<b>SBC A,[m]</b>	Subtract Data Memory from ACC with Carry
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC - [m] - C
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>SBC A, x</b>	Subtract immediate data from ACC with Carry
Description	The immediate data and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC - [m] - $\bar{C}$
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>SBCM A,[m]</b>	Subtract Data Memory from ACC with Carry and result in Data Memory
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	[m] ← ACC - [m] - C
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>SDZ [m]</b>	Skip if decrement Data Memory is 0
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	[m] ← [m] - 1 Skip if [m]=0
Affected flag(s)	None
<b>SDZA [m]</b>	Skip if decrement Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	ACC ← [m] - 1 Skip if ACC=0
Affected flag(s)	None

<b>SET [m]</b>	Set Data Memory
Description	Each bit of the specified Data Memory is set to 1.
Operation	$[m] \leftarrow FFH$
Affected flag(s)	None
<b>SET [m].i</b>	Set bit of Data Memory
Description	Bit i of the specified Data Memory is set to 1.
Operation	$[m].i \leftarrow 1$
Affected flag(s)	None
<b>SIZ [m]</b>	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] + 1$ Skip if $[m]=0$
Affected flag(s)	None
<b>SIZA [m]</b>	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] + 1$ Skip if $ACC=0$
Affected flag(s)	None
<b>SNZ [m].i</b>	Skip if Data Memory is not 0
Description	If the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m].i \neq 0$
Affected flag(s)	None
<b>SNZ [m]</b>	Skip if Data Memory is not 0
Description	If the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m] \neq 0$
Affected flag(s)	None
<b>SUB A,[m]</b>	Subtract Data Memory from ACC
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C, SC, CZ

<b>SUBM A,[m]</b>	Subtract Data Memory from ACC with result in Data Memory
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>SUB A,x</b>	Subtract immediate data from ACC
Description	The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - x$
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>SWAP [m]</b>	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	$[m].3 \sim [m].0 \leftrightarrow [m].7 \sim [m].4$
Affected flag(s)	None
<b>SWAPA [m]</b>	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC.3 \sim ACC.0 \leftarrow [m].7 \sim [m].4$ $ACC.7 \sim ACC.4 \leftarrow [m].3 \sim [m].0$
Affected flag(s)	None
<b>SZ [m]</b>	Skip if Data Memory is 0
Description	If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if $[m]=0$
Affected flag(s)	None
<b>SZA [m]</b>	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m]$ Skip if $[m]=0$
Affected flag(s)	None
<b>SZ [m].i</b>	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if $[m].i=0$
Affected flag(s)	None

<b>TABRD [m]</b>	Read table (specific page) to TBLH and Data Memory
Description	The low byte of the program code (specific page) addressed by the table pointer pair (TBLP and TBHP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>TABRDL [m]</b>	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>ITABRD [m]</b>	Increment table pointer low byte first and read table to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the program code addressed by the table pointer (TBHP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>ITABRDL [m]</b>	Increment table pointer low byte first and read table (last page) to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>XOR A,[m]</b>	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "XOR" [m]
Affected flag(s)	Z
<b>XORM A,[m]</b>	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "XOR" [m]
Affected flag(s)	Z
<b>XOR A,x</b>	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "XOR" x
Affected flag(s)	Z

### Extended Instruction Definition

The extended instructions are used to directly access the data stored in any data memory sections.

<b>LADC A,[m]</b>	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC
<b>LADCM A,[m]</b>	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC
<b>LADD A,[m]</b>	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC
<b>LADDM A,[m]</b>	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC
<b>LAND A,[m]</b>	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "AND" } [m]$
Affected flag(s)	Z
<b>LANDM A,[m]</b>	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \text{ "AND" } [m]$
Affected flag(s)	Z
<b>LCLR [m]</b>	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	$[m] \leftarrow 00H$
Affected flag(s)	None
<b>LCLR [m].i</b>	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	$[m].i \leftarrow 0$
Affected flag(s)	None

<b>LCPL [m]</b>	Complement Data Memory
Description	Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa.
Operation	$[m] \leftarrow \overline{[m]}$
Affected flag(s)	Z
<b>LCPLA [m]</b>	Complement Data Memory with result in ACC
Description	Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow \overline{[m]}$
Affected flag(s)	Z
<b>LDAA [m]</b>	Decimal-Adjust ACC for addition with result in Data Memory
Description	Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.
Operation	$[m] \leftarrow ACC + 00H$ or $[m] \leftarrow ACC + 06H$ or $[m] \leftarrow ACC + 60H$ or $[m] \leftarrow ACC + 66H$
Affected flag(s)	C
<b>LDEC [m]</b>	Decrement Data Memory
Description	Data in the specified Data Memory is decremented by 1.
Operation	$[m] \leftarrow [m] - 1$
Affected flag(s)	Z
<b>LDECA [m]</b>	Decrement Data Memory with result in ACC
Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] - 1$
Affected flag(s)	Z
<b>LINC [m]</b>	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	$[m] \leftarrow [m] + 1$
Affected flag(s)	Z
<b>LINCA [m]</b>	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] + 1$
Affected flag(s)	Z

<b>LMOV A,[m]</b>	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	$ACC \leftarrow [m]$
Affected flag(s)	None
<b>LMOV [m],A</b>	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	$[m] \leftarrow ACC$
Affected flag(s)	None
<b>LOR A,[m]</b>	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "OR" } [m]$
Affected flag(s)	Z
<b>LORM A,[m]</b>	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \text{ "OR" } [m]$
Affected flag(s)	Z
<b>LRL [m]</b>	Rotate Data Memory left
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
Operation	$[m].(i+1) \leftarrow [m].i; (i=0\sim 6)$ $[m].0 \leftarrow [m].7$
Affected flag(s)	None
<b>LRLA [m]</b>	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.(i+1) \leftarrow [m].i; (i=0\sim 6)$ $ACC.0 \leftarrow [m].7$
Affected flag(s)	None
<b>LRLC [m]</b>	Rotate Data Memory left through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.
Operation	$[m].(i+1) \leftarrow [m].i; (i=0\sim 6)$ $[m].0 \leftarrow C$ $C \leftarrow [m].7$
Affected flag(s)	C
<b>LRLCA [m]</b>	Rotate Data Memory left through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.(i+1) \leftarrow [m].i; (i=0\sim 6)$ $ACC.0 \leftarrow C$ $C \leftarrow [m].7$
Affected flag(s)	C

<b>LRR [m]</b>	Rotate Data Memory right
Description	The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.
Operation	$[m].i \leftarrow [m].(i+1); (i=0\sim 6)$ $[m].7 \leftarrow [m].0$
Affected flag(s)	None
<b>LRRRA [m]</b>	Rotate Data Memory right with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.i \leftarrow [m].(i+1); (i=0\sim 6)$ $ACC.7 \leftarrow [m].0$
Affected flag(s)	None
<b>LRRC [m]</b>	Rotate Data Memory right through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.
Operation	$[m].i \leftarrow [m].(i+1); (i=0\sim 6)$ $[m].7 \leftarrow C$ $C \leftarrow [m].0$
Affected flag(s)	C
<b>LRRCA [m]</b>	Rotate Data Memory right through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.i \leftarrow [m].(i+1); (i=0\sim 6)$ $ACC.7 \leftarrow C$ $C \leftarrow [m].0$
Affected flag(s)	C
<b>LSBC A,[m]</b>	Subtract Data Memory from ACC with Carry
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - [m] - C$
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>LSBCM A,[m]</b>	Subtract Data Memory from ACC with Carry and result in Data Memory
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m] - C$
Affected flag(s)	OV, Z, AC, C, SC, CZ

<b>LSDZ [m]</b>	Skip if decrement Data Memory is 0
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] - 1$ Skip if $[m]=0$
Affected flag(s)	None
<b>LSDZA [m]</b>	Skip if decrement Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] - 1$ Skip if $ACC=0$
Affected flag(s)	None
<b>LSET [m]</b>	Set Data Memory
Description	Each bit of the specified Data Memory is set to 1.
Operation	$[m] \leftarrow FFH$
Affected flag(s)	None
<b>LSET [m].i</b>	Set bit of Data Memory
Description	Bit i of the specified Data Memory is set to 1.
Operation	$[m].i \leftarrow 1$
Affected flag(s)	None
<b>LSIZ [m]</b>	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] + 1$ Skip if $[m]=0$
Affected flag(s)	None
<b>LSIZA [m]</b>	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] + 1$ Skip if $ACC=0$
Affected flag(s)	None
<b>LSNZ [m].i</b>	Skip if Data Memory is not 0
Description	If the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m].i \neq 0$
Affected flag(s)	None

<b>LSNZ [m]</b>	Skip if Data Memory is not 0
Description	If the content of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if [m] ≠ 0
Affected flag(s)	None
<b>LSUB A,[m]</b>	Subtract Data Memory from ACC
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC – [m]
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>LSUBM A,[m]</b>	Subtract Data Memory from ACC with result in Data Memory
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	[m] ← ACC – [m]
Affected flag(s)	OV, Z, AC, C, SC, CZ
<b>LSWAP [m]</b>	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	[m].3~[m].0 ↔ [m].7~[m].4
Affected flag(s)	None
<b>LSWAPA [m]</b>	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC.3~ACC.0 ← [m].7~[m].4 ACC.7~ACC.4 ← [m].3~[m].0
Affected flag(s)	None
<b>LSZ [m]</b>	Skip if Data Memory is 0
Description	If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if [m]=0
Affected flag(s)	None
<b>LSZA [m]</b>	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	ACC ← [m] Skip if [m]=0
Affected flag(s)	None

<b>LSZ [m].i</b>	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i=0
Affected flag(s)	None
<b>LTABRD [m]</b>	Read table (current page) to TBLH and Data Memory
Description	The low byte of the program code (current page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>LTABRDL [m]</b>	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>LITABRD [m]</b>	Increment table pointer low byte first and read table to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the program code addressed by the table pointer (TBLP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>LITABRDL [m]</b>	Increment table pointer low byte first and read table (last page) to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
<b>LXOR A,[m]</b>	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "XOR" [m]
Affected flag(s)	Z
<b>LXORM A,[m]</b>	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "XOR" [m]
Affected flag(s)	Z

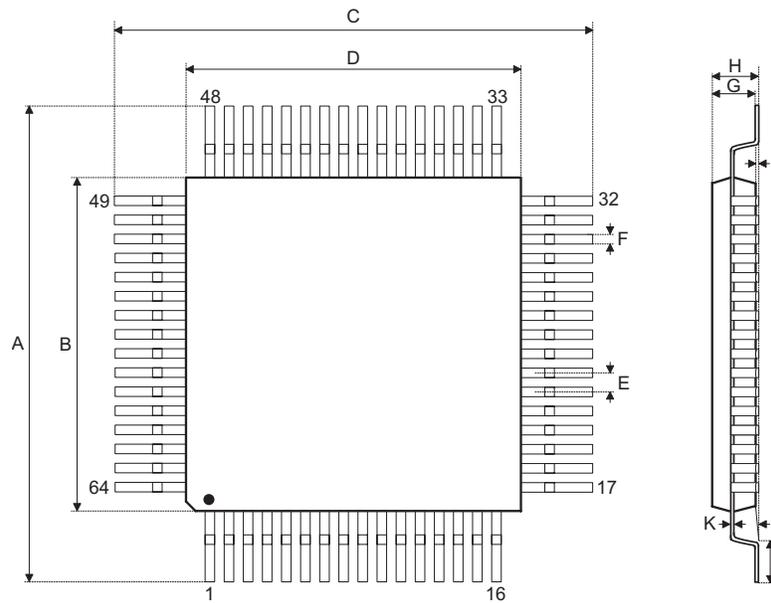
## Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package/Carton Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- [Further Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [Packing Materials Information](#)
- [Carton information](#)

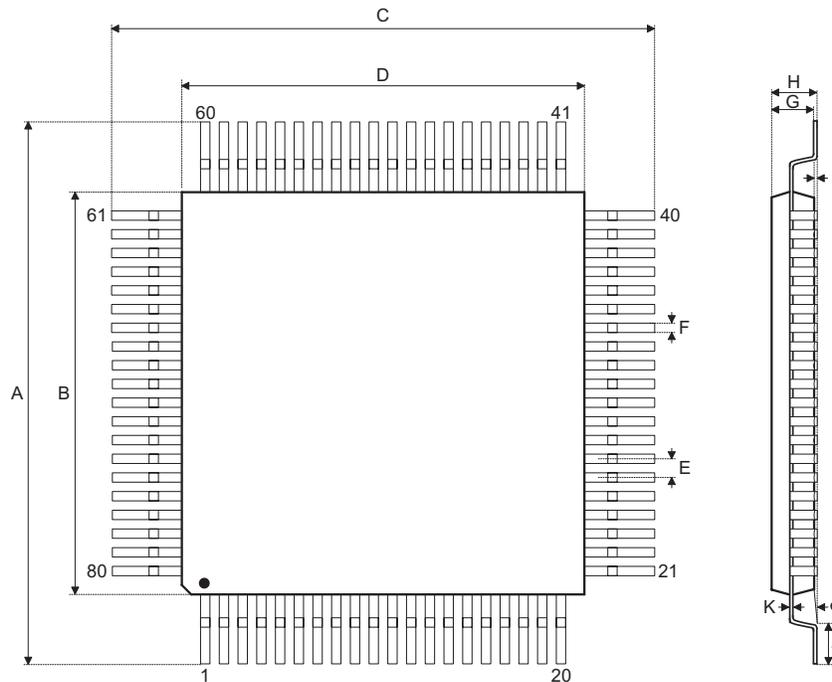
64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

**80-pin LQFP (10mm×10mm) Outline Dimensions**



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12.00 BSC	—
B	—	10.00 BSC	—
C	—	12.00 BSC	—
D	—	10.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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