FAIRCHILD SEMICONDUCTOR TM

April 1998

# FDS4410

## Single N-Channel Logic Level PWM Optimized PowerTrenchTM MOSFET

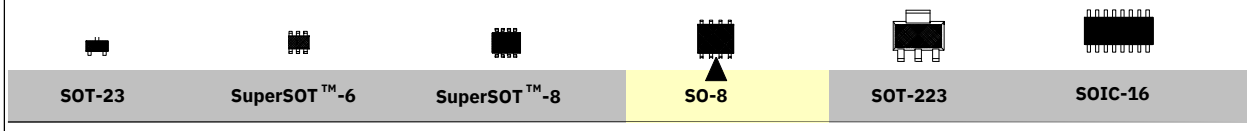
### General Description Features

This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

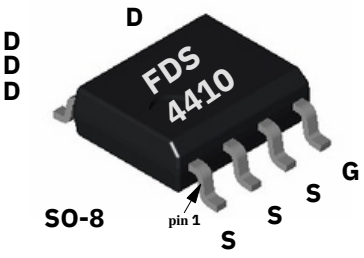
The MOSFET features faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

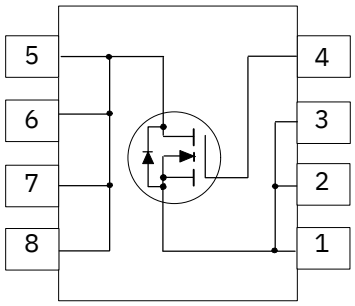
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

- 10 A, 30 V. $R_{DS(ON)}$ = 0.0135 Ω @ VGS = 10 V
  RDS(ON) = 0.0200 Ω @ VGS = 4.5 V.
- Optimized for use in switching DC/DC converters with PWM controllers.
- Very fast switching .
- Low gate charge (typical 22 nC).



SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16




### Absolute Maximum Ratings $T_A$= 25C unless other wise noted

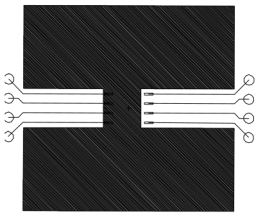
| Symbol | Parameter | FDS4410 | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$ | Drain Current - Continuous (Note 1a) | 10 | A |
| | - Pulsed | 50 | |
| $P_D$ | Power Dissipation for Single Operation (Note 1a) | 2.5 | W |
| | (Note 1b) | 1.2 | |
| | (Note 1c) | 1 | |
| $T_J, T_{STG}$ | Operating and Storage Temperature Range | -55 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to- (Note 1a) | 5 | °C/ |
| $R_{\theta JC}$ | Ambient Thermal Resistance, | 0 | W |
| | Junction-to-Case (Note 1) | 2 | °C/ |
| | | 5 | W |

## Electrical Characteristics (TA = 25°C unless otherwise noted)

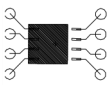
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| BVDSS | Drain-Source Breakdown Voltage | VGS = 0 V, I D = 250 µA | 30 | | | V |
| $\Delta BV_{DSS}/\Delta T_j$ | Breakdown Voltage Temp. Coefficient | I50 µA, Referenced to 25 o D = 2C | | 21 | | mV /oC |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | V | | | 1 | µA |
| | | DS = 24 V, VGS = 0 V | | | 10 | µA |
| | | TJ = 55°C | | | | |
| $I_{GSSF}$ | Gate - Body Leakage, | V GS = 20 V, VDS = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Forward Gate - Body | VGS = -20 V, VDS= 0 V | | | -10 | nA |
| **ON CHARACTERISTICS** | Leakage, Reverse | | | | 0 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | V DS = VGS, ID = 250 µA | 1 | 2 | 3 | V |
| $\Delta V_{GS(th)}/\Delta T_j$ | Gate Threshold Voltage Temp. Coefficient | I50 µA, Ro | | -4.5 | | mV /oC |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | D = 2eferenced to 25 C | | 0.011 | 0.0135 Ω | |
| | | V | | 0.018 | 0.023 | |
| | | GS = 10 V, I D = 10 A | | | | |
| | | V GS = 4.5 V, I D = 9 A TJ =125°C | | 0.017 | 0.02 | |
| $I_{D(ON)}$ | On-State Drain Current | VGS = 10 V, VDS = 5 V | 50 | | A | |
| $g_{FS}$ | Forward Transconductance | VDS = 10 V, I D= 10 A | | 27 | S | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | VDS = 15 V, VGS = 0 V, f = 1.0 MHz | | 134 | | pF |
| $C_{os}$ | Output Capacitance | | | 0 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 340 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | 125 | | |
| $t_{D(on)}$ | Turn - On Delay | V DS= 15 V, I D= 1 A | | 1 | 2 | ns |
| t | Time Turn - On | V 6 Ω | | 2 | 2 | ns |
| $t_r$ | Rise Time | GS = 10 V , RGEN = | | 1 | 2 | ns |
| $t_{D(off)}$ | Turn - Off Delay | | | 3 | 4 | ns |
| t | Time | V DS = 15 V, I D = 10 A, | | 3 | 6 | nC |
| $t_f$ | Turn - Off Fall Time | V | | 8 | 0 | nC |
| $Q_g$ | Total Gate Charge | GS = 10 V | | 1 | 1 | nC |
| $Q_{gs}$ | Gate-Source | | | 0 | 8 | |
| | Charge | | | 2 | 2. | |
| $Q_{gd}$ | Gate-Drain Charge | | | 4 | 2 | |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.3 | A |
| $V_{SD}$ (Note 2) | Drain-Source Diode Forward Voltage | VGS = 0 V, IS = 2.1 A | | 0.73 | 1.2 | V |

Notes:

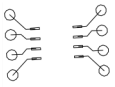
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50OC/W on a 1 in2 pad of 2oz copper.



b. 105OC/W on a 0.04 in2 pad of 2oz copper.



c. 125OC/W on a 0.006 in2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

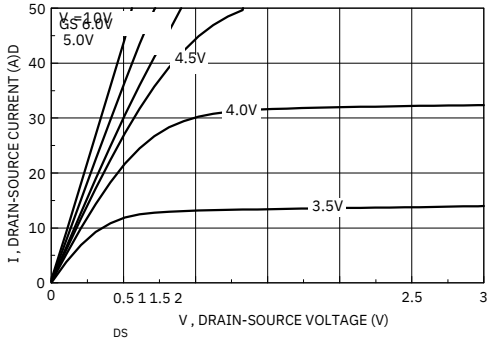



**Figure 1. On-Region Characteristics**.

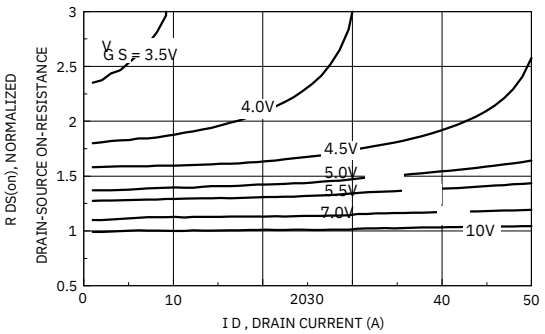



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage**.

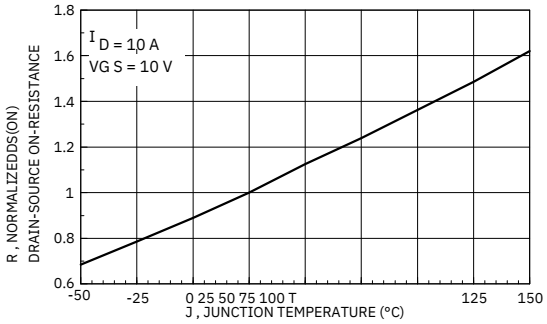



**Figure 3. On-Resistance Variation with Temperature**.

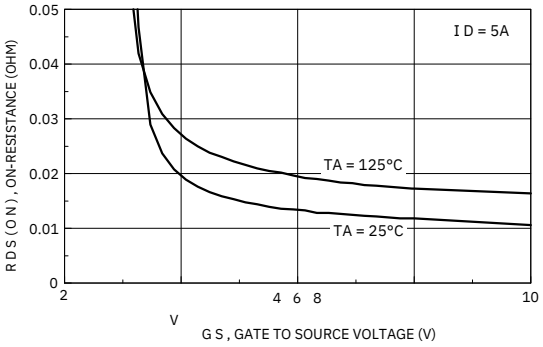



**Figure 4 . On-Resistance Variation with Gate-to-Source Voltage.**

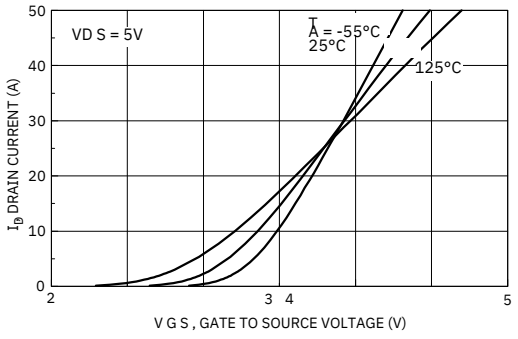



**Figure 5 . Transfer Characteristics.**

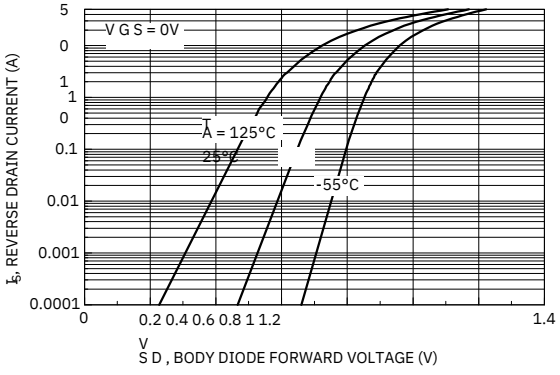



**Figure 6 . Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Electrical And Thermal Characteristics

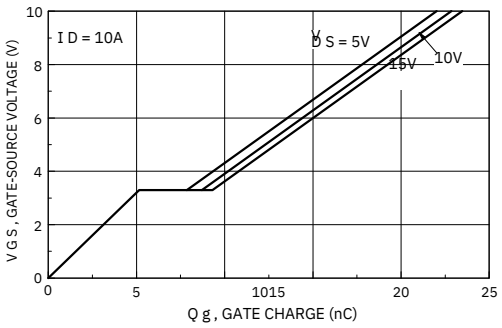



**Figure 7. Gate Charge Characteristics.**

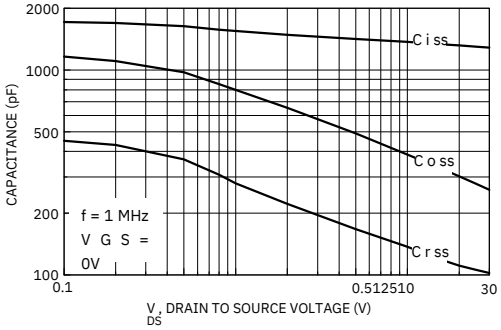



**Figure 8. Capacitance Characteristics.**

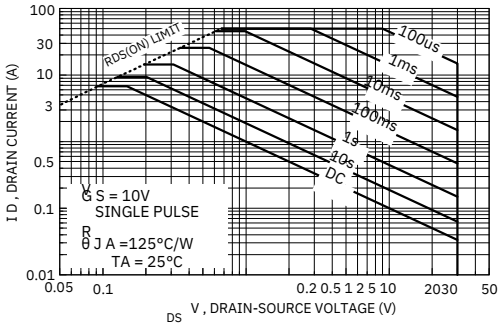



**Figure 9. Maximum Safe Operating Area.**

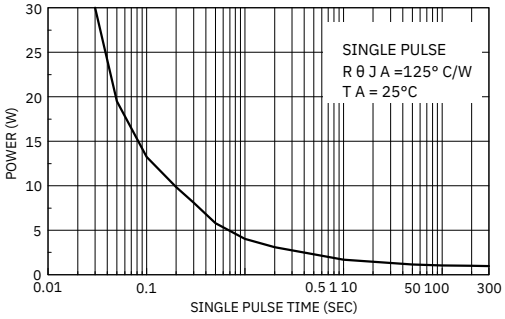



**Figure 10. Single Pulse Maximum Power Dissipation.**

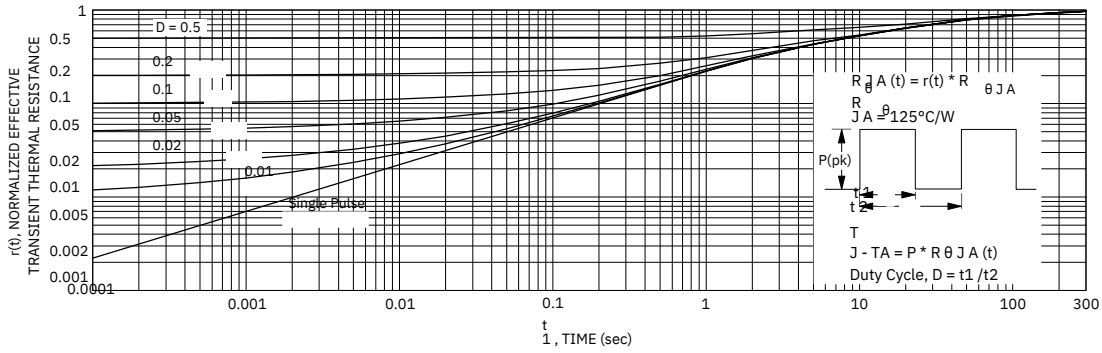



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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