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FQB4N80 / FQI4N80

N-Channel QFETMOSFET

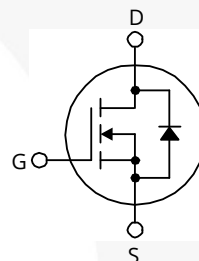
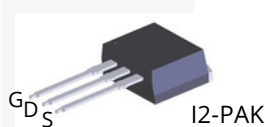
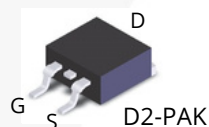
800 V, 3.9 A, 3.6 Ω

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 3.9 A, 800 V, $R_{DS(on)} = 3.6 \Omega$ (Max.) @ $V_{GS} = 10$ V, $I_D = 1.95$ A
- Low Gate Charge (Typ. 19 nC)
- Low C_{rss} (Typ. 8.6 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQB4N80TM / FQI4N80TU	Unit
V_{DS}	Drain-Source Voltage	800	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	3.9	A
	- Continuous ($T_C = 100^\circ\text{C}$)	2.47	A
I_{DM}	Drain Current - Pulsed (Note 1)	15.6	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	460	mJ
I_{AR}	Avalanche Current	3.9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13	mJ
dv/dt	Peak Diode Recovery dv/dt	4.0	V/ns
PD	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	130	W
	- Derate above 25°C (Note 3)	1.04	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQB4N80TM / FQI4N80TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.96	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in2 pad of 2 oz copper), Max.	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB4N80TM	FQB4N80	D2-PAK	Tape and Reel	330 mm	24 mm	800 units
FQI4N80TU	FQI4N80	I2-PAK	Tube	N/A	N/A	50 units

Electrical Characteristics $T = 25^{\circ}\text{C}$ unless otherwise noted.

Sym bol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	800	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to	--	0.95	--	$^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$25^{\circ}\text{C } V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 640\text{ V}, T_C = 125^{\circ}\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.	--	5.	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.95\text{ A}$	0 -	2.	0	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 1.95\text{ A}$	- -	8	3.	S
			-	3.	6 -	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	88	88	pF
C_{oss}	Output Capacitance		-	0	0	pF
C_{rss}	Reverse Transfer Capacitance		-	75	10	pF
			-	8.6	0	
			-		12	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 3.9\text{ A}, I_{RG} = 25\text{ }\Omega$	-	16	40	ns
t_{r}	Turn-On Rise Time		-	45	10	ns
$t_{d(off)}$	Turn-Off Delay Time		-	35	0	ns
t_{f}	Turn-Off Fall Time	(Note 4)	-	35	80	ns
Q_g	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 3.9\text{ A}, V_{GS} = 10\text{ V}$	-	19	80	nC
Q_{gs}	Gate-Source Charge		-	4.	25	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	-	2	--	nC
			-	9.	--	
			-	1		

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		-	--	3.9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	--	15.	A
V_D	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.9\text{ A}$	-	--	6	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 3.9\text{ A}$, Reverse	-	575	1.4	ns
Q_{rr}	Recovery Charged	$IF / dt = 100\text{ A}/\mu\text{s}$	-	3.65	--	μC
			-		--	

1. Repetitive Rating : Pulse width limited by maximum junction temperature
 2. $L = 57\text{ mH}, I = 3.9\text{ A}, V_{DS} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^{\circ}\text{C}$
 3. $I_S, V \leq BV$, Starting $T = 25^{\circ}\text{C}, di/dt \leq 200\text{ A}/\mu\text{s}$
 4. Essentially independent of operating temperature

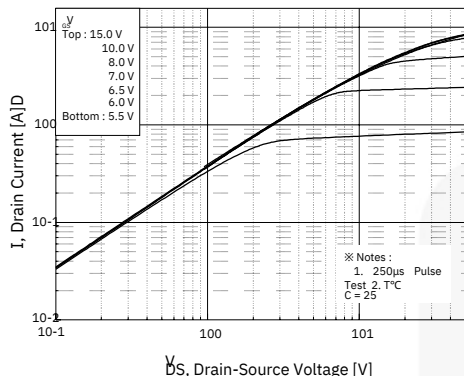


Figure 1. On-Region Characteristics

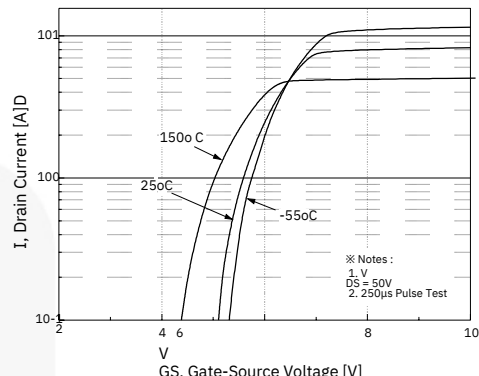


Figure 2. Transfer Characteristics

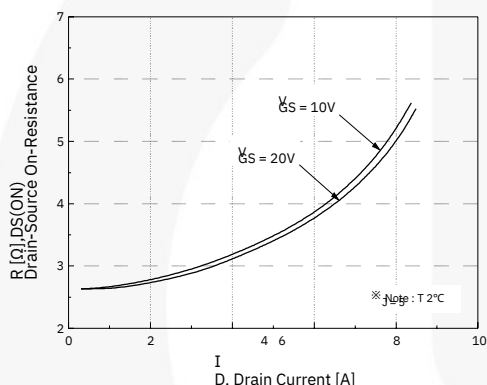


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

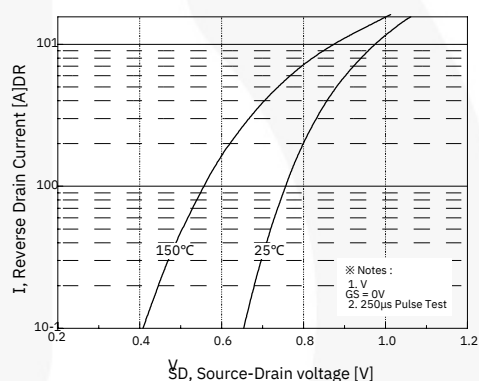


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

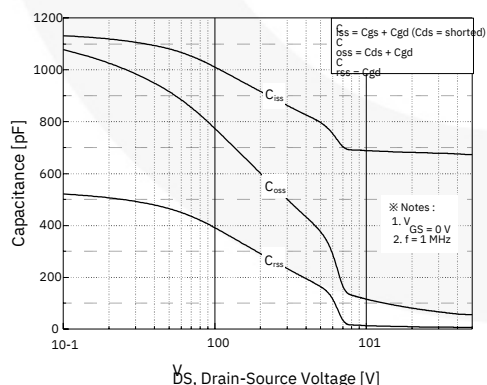


Figure 5. Capacitance Characteristics

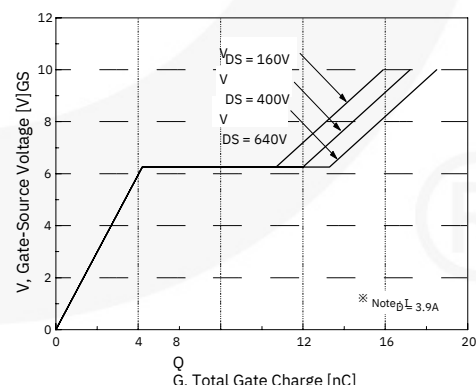


Figure 6. Gate Charge Characteristics

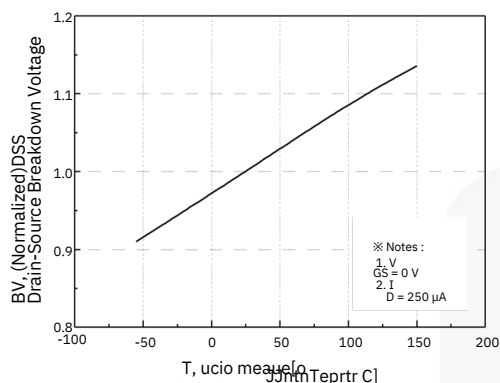


Figure 7. Breakdown Voltage Variation vs. Temperature

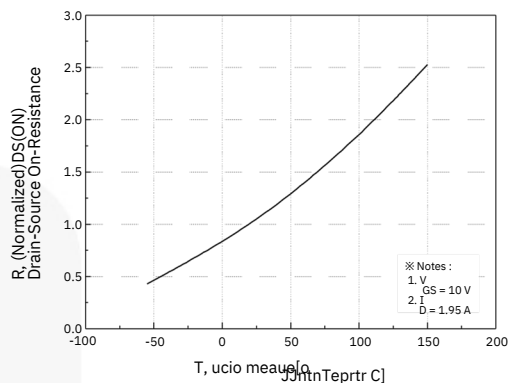


Figure 8. On-Resistance Variation vs. Temperature

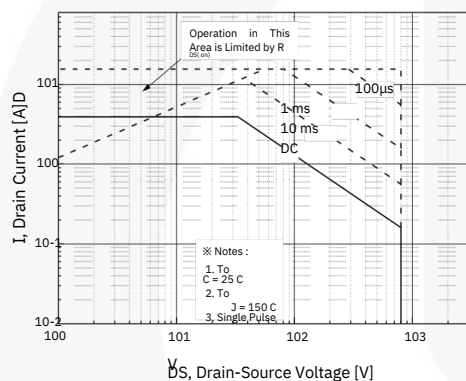


Figure 9. Maximum Safe Operating Area

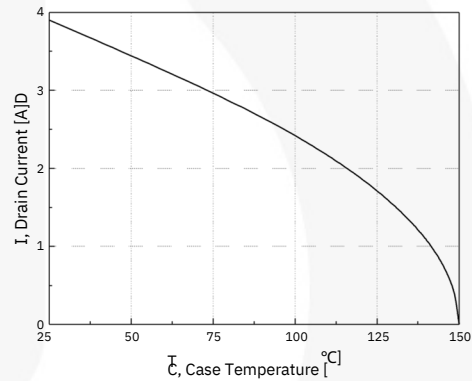


Figure 10. Maximum Drain Current vs. Case Temperature

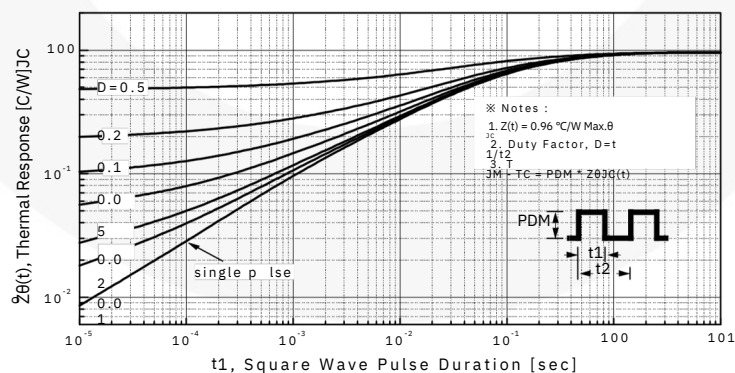


Figure 11. Transient Thermal Response Curve

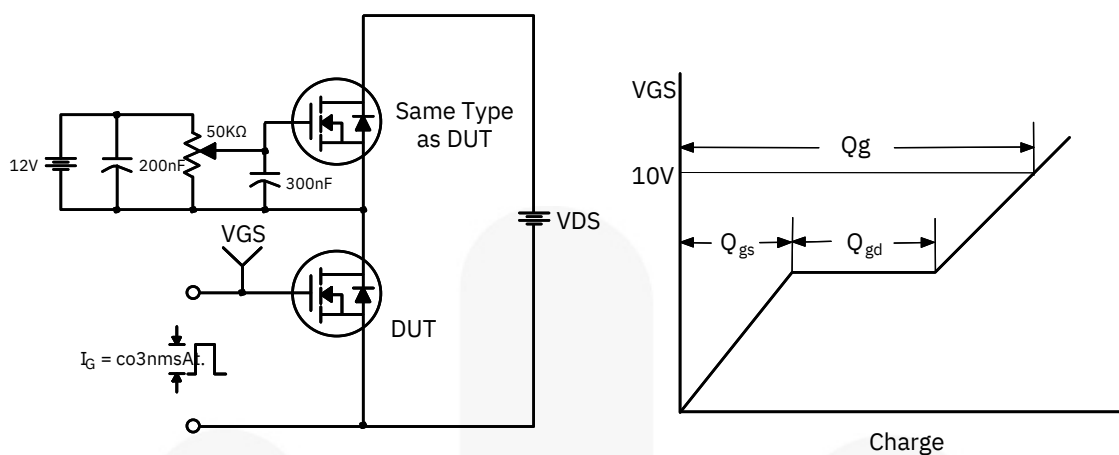


Figure 12. Gate Charge Test Circuit & Waveform

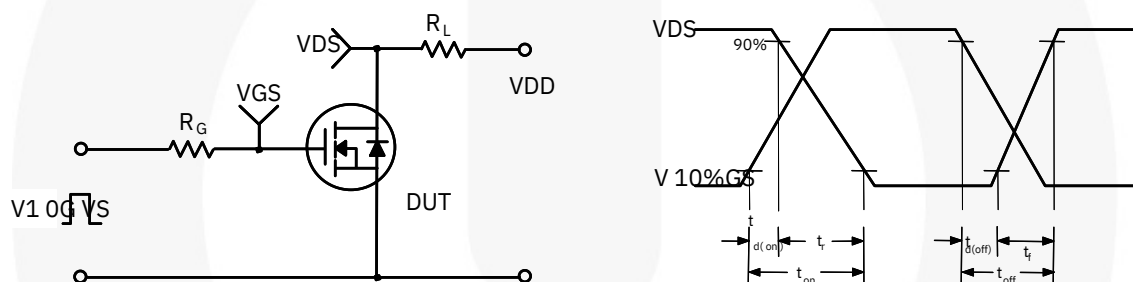


Figure 13. Resistive Switching Test Circuit & Waveforms

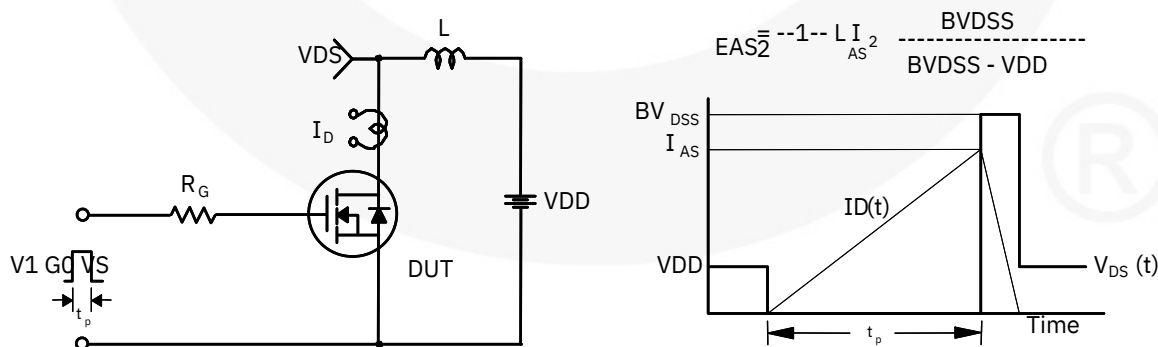


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

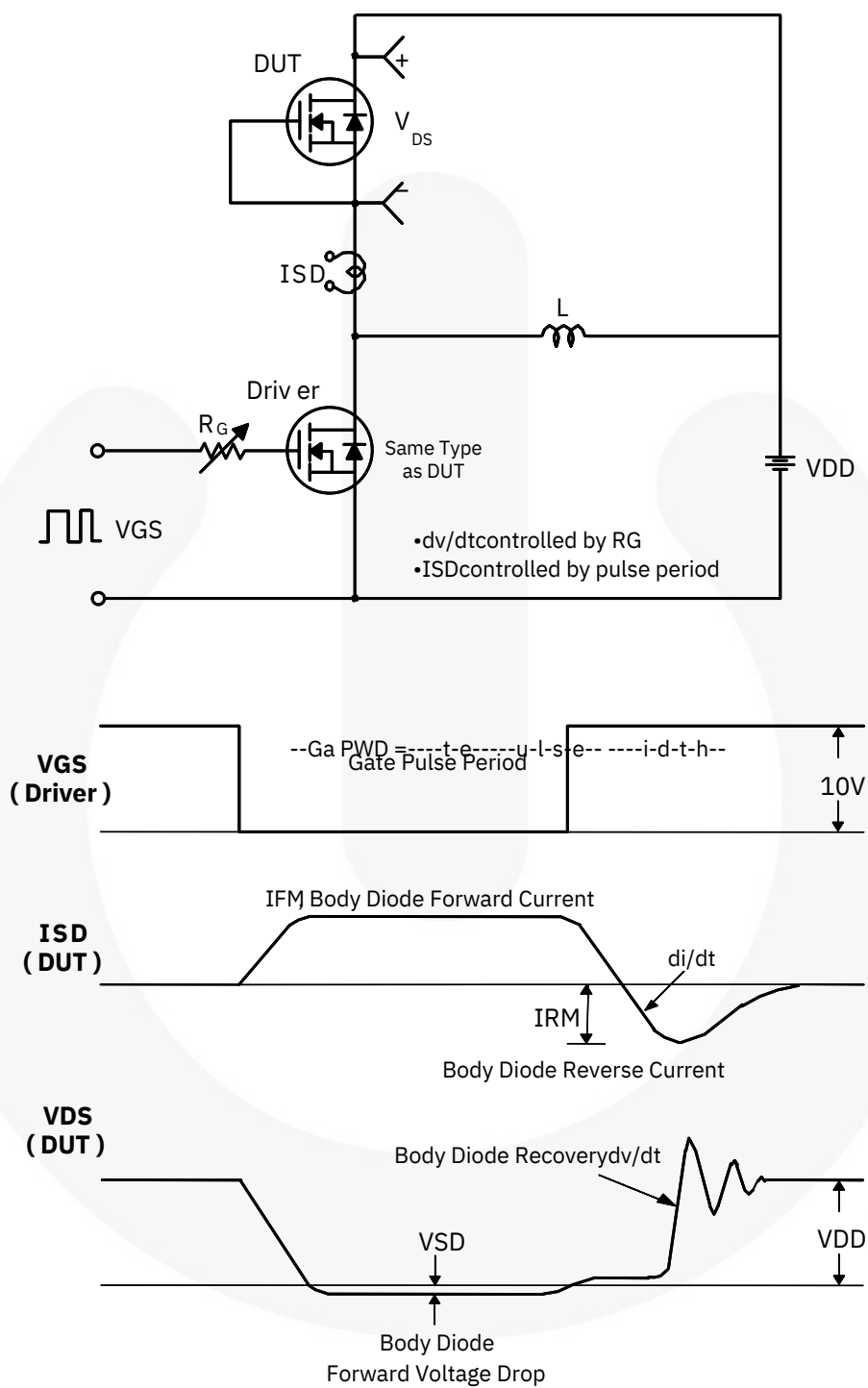


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

TO-263 2L (D2PAK)

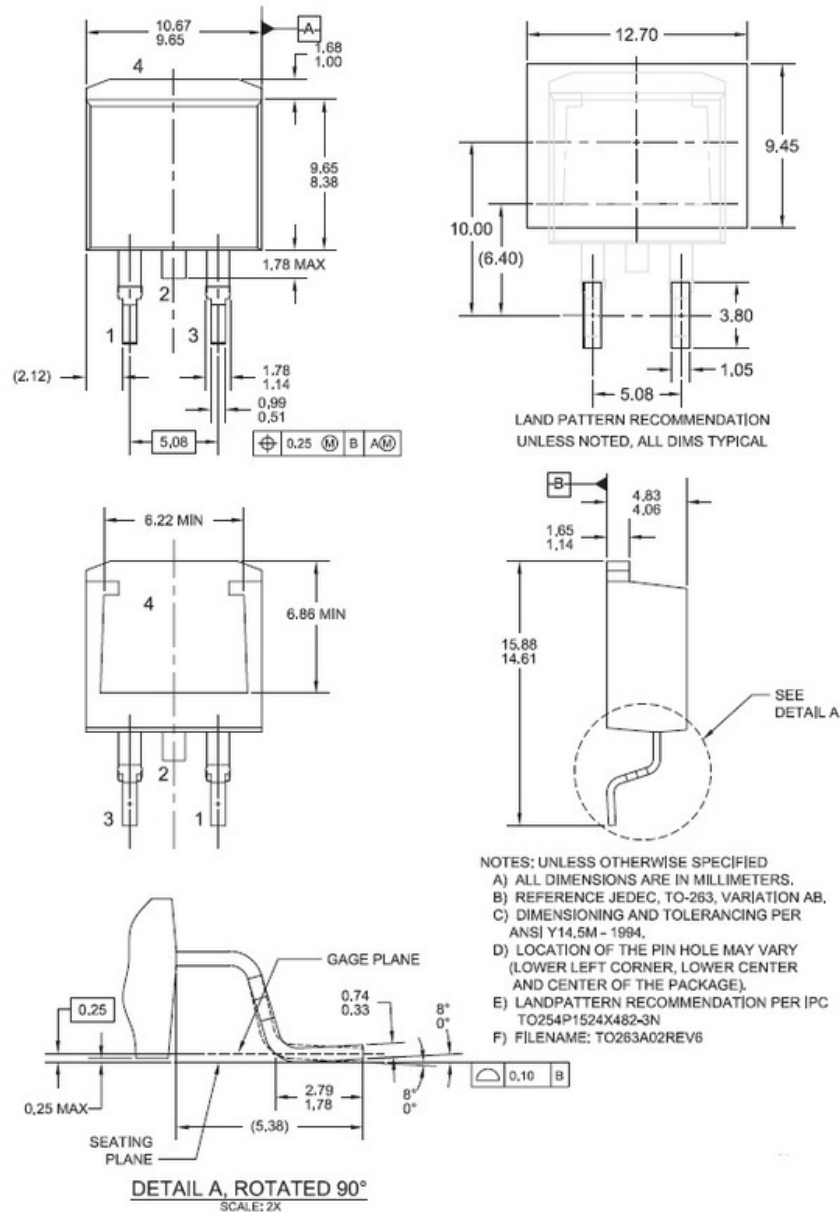


Figure 16. 2LD,TO263, Surface Mount

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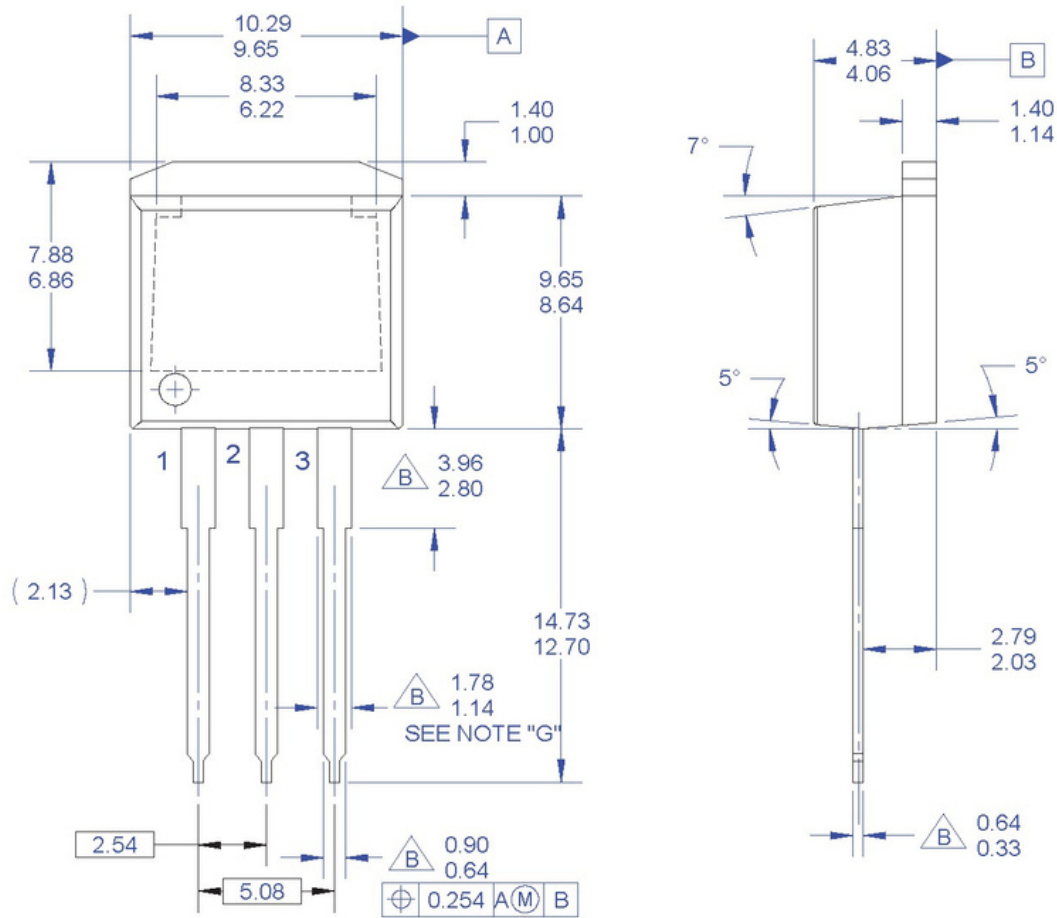
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Dimension in Millimeters

Mechanical Dimensions

TO-262 3L (I2PAK)



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

Figure 17. 3LD, TO262, Jedec Variation AA (I2PAK)

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Dimension in Millimeters



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Definition of Terms

Datasheet Identification Product Status Definition

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Datasheet contains preliminary data;	supplementary data will be published at a later	
Preliminary	First Production date	Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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