

**AO4468**
**N-Channel Enhancement Mode Field Effect Transistor**

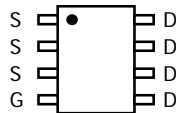
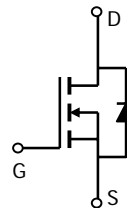
**General Description**

The AO4468 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. This device is suitable for use as a load switch or in PWM applications. The source leads are separated to allow a Kelvin connection to the source, which may be used to bypass the source inductance.

Standard Product AO4468 is Pb-free (meets ROHS & Sony 259 specifications). AO4468L is a Green Product ordering option. AO4468 and AO4468L are electrically identical.

**Features**

$V_{DS}$  (V) = 30V  
 $I_D$  = 11.6A ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 14m\Omega$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 22m\Omega$  ( $V_{GS} = 4.5V$ )


**SOIC-8**

**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>A</sup>	$I_D$	$T_A=25^\circ\text{C}$	11.6
		$T_A=70^\circ\text{C}$	9.2
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	50	A
Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	31	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	59	75
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C		0.003	1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =10mA	1.5	2	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	50			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =11.6A T <sub>J</sub> =125°C		11 17	14 21	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		17.4	22	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =11.6A		19		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.73	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		955	1200	pF
C <sub>oss</sub>	Output Capacitance		145		pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		112		pF	
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		0.5	0.85	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =11.6A		17	24	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge		9	12	nC	
Q <sub>gs</sub>	Gate Source Charge		3.4		nC	
Q <sub>gd</sub>	Gate Drain Charge		4.7		nC	
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =1.30Ω, R <sub>GEN</sub> =3Ω		5	6.5	ns
t <sub>r</sub>	Turn-On Rise Time		6	7.5	ns	
t <sub>D(off)</sub>	Turn-Off DelayTime		19	25	ns	
t <sub>f</sub>	Turn-Off Fall Time		4.5	6	ns	
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =11.6A, dI/dt=100A/μs		19	21	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =11.6A, dI/dt=100A/μs		9	12	nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t<sub>θ</sub> ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

Rev 0 : Apr 2006

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

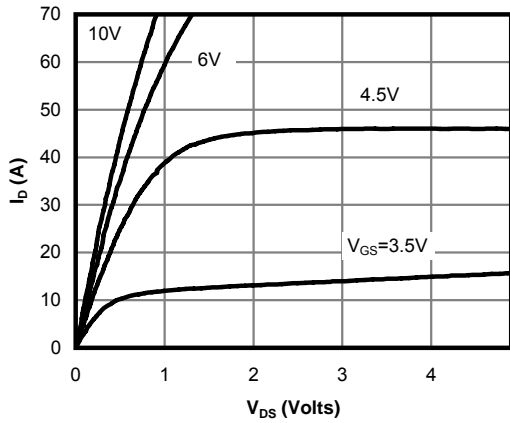


Fig 1: On-Region Characteristics

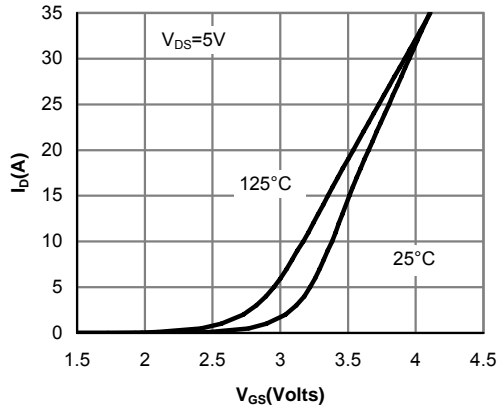


Figure 2: Transfer Characteristics

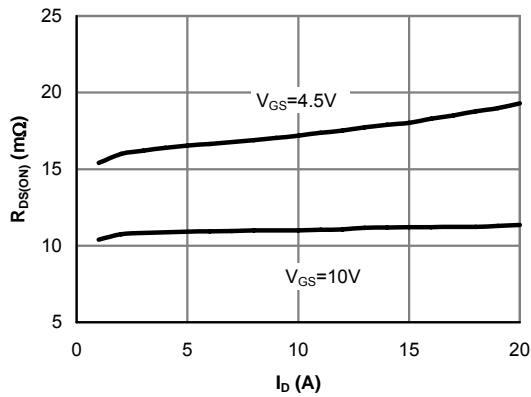


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

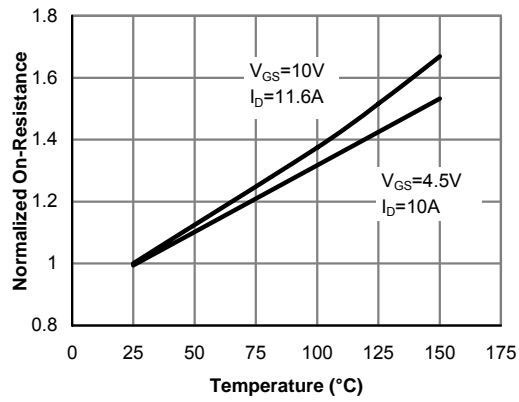


Figure 4: On-Resistance vs. Junction Temperature

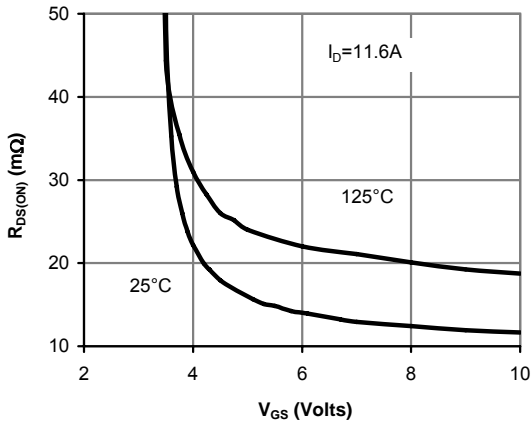


Figure 5: On-Resistance vs. Gate-Source Voltage

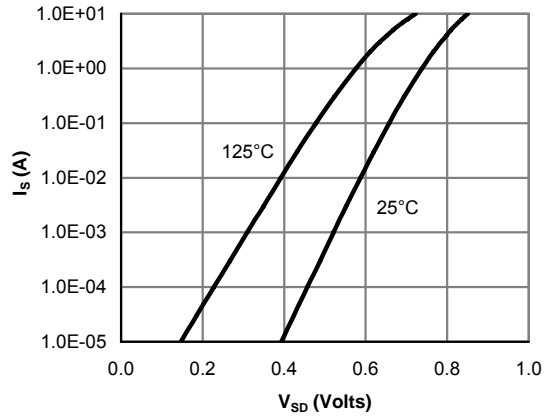


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

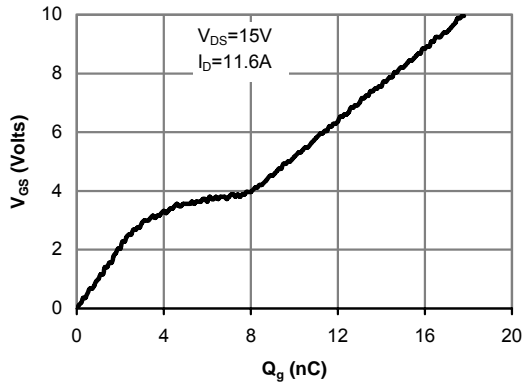


Figure 7: Gate-Charge Characteristics

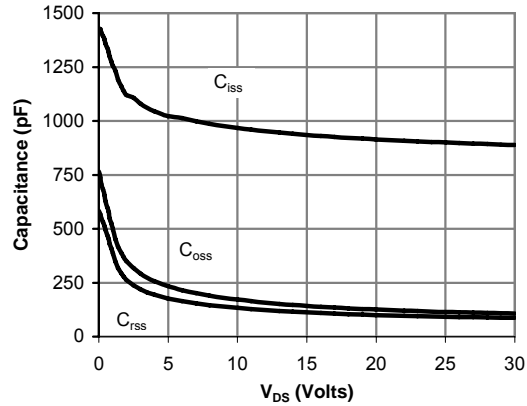


Figure 8: Capacitance Characteristics

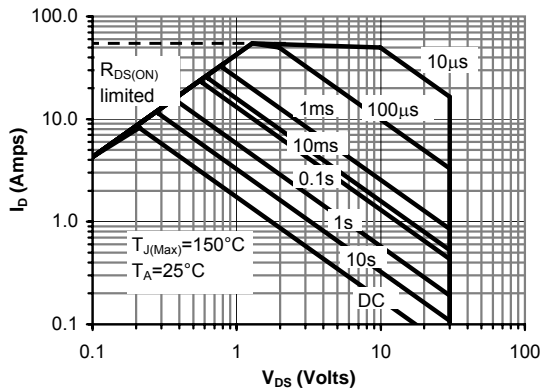


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

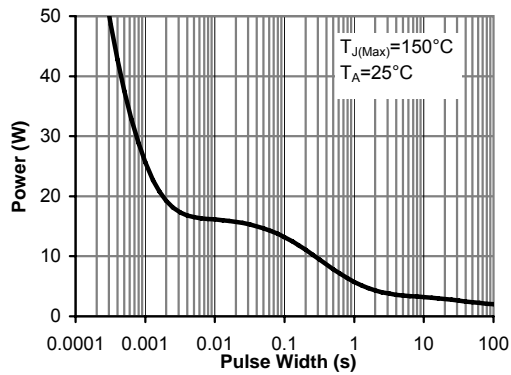


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

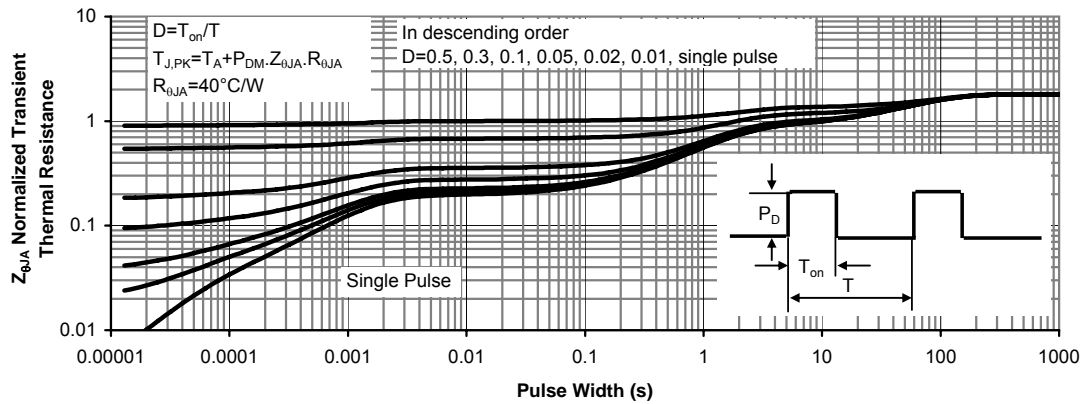


Figure 11: Normalized Maximum Transient Thermal Impedance