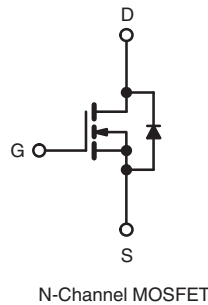
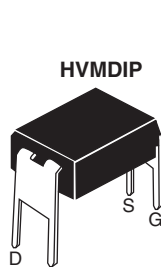


## Power MOSFET

| PRODUCT SUMMARY           |                               |
|---------------------------|-------------------------------|
| $V_{DS}$ (V)              | 100                           |
| $R_{DS(on)}$ ( $\Omega$ ) | $V_{GS} = 10\text{ V}$   0.27 |
| $Q_g$ (Max.) (nC)         | 16                            |
| $Q_{gs}$ (nC)             | 4.4                           |
| $Q_{gd}$ (nC)             | 7.7                           |
| Configuration             | Single                        |



### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

| ORDERING INFORMATION |                           |
|----------------------|---------------------------|
| Package              | HVMDIP                    |
| Lead (Pb)-free       | IRFD120PbF<br>SiHFD120-E3 |
| SnPb                 | IRFD120<br>SiHFD120       |

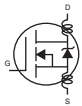

| ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |                                  |                |                                   |                     |
|---|----------------------------------|----------------|-----------------------------------|---------------------|
| PARAMETER   |                                  | SYMBOL         | LIMIT                             | UNIT                |
| Drain-Source Voltage  |                                  | $V_{DS}$       | 100                               | V                   |
| Gate-Source Voltage   |                                  | $V_{GS}$       | $\pm 20$                          |                     |
| Continuous Drain Current  | $V_{GS}$ at 10 V                 | $I_D$          | $T_A = 25\text{ }^\circ\text{C}$  | A                   |
|   |                                  |                | $T_A = 100\text{ }^\circ\text{C}$ |                     |
| Pulsed Drain Current <sup>a</sup>   |                                  | $I_{DM}$       | 10                                |                     |
| Linear Derating Factor  |                                  |                | 0.0083                            | W/ $^\circ\text{C}$ |
| Single Pulse Avalanche Energy <sup>b</sup>  |                                  | $E_{AS}$       | 100                               | mJ                  |
| Repetitive Avalanche Current <sup>a</sup>   |                                  | $I_{AR}$       | 1.3                               | A                   |
| Repetitive Avalanche Energy <sup>a</sup>  |                                  | $E_{AR}$       | 0.13                              | mJ                  |
| Maximum Power Dissipation   | $T_A = 25\text{ }^\circ\text{C}$ | $P_D$          | 1.3                               | W                   |
| Peak Diode Recovery dV/dt <sup>c</sup>  |                                  | dV/dt          | 5.5                               | V/ns                |
| Operating Junction and Storage Temperature Range                                      |                                  | $T_J, T_{stg}$ | - 55 to + 175                     | $^\circ\text{C}$    |
| Soldering Recommendations (Peak Temperature)  | for 10 s                         |                | 300 <sup>d</sup>                  |                     |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 22\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 2.6\text{ A}$  (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$ ,  $dI/dt \leq 110\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS  |            |      |      |      |
|-----------------------------|------------|------|------|------|
| PARAMETER                   | SYMBOL     | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | $R_{thJA}$ | -    | 120  | °C/W |

| SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |                     |   |  |      |      |           |               |
|---|---------------------|---|--|------|------|-----------|---------------|
| PARAMETER   | SYMBOL              | TEST CONDITIONS   |  | MIN. | TYP. | MAX.      | UNIT          |
| <b>Static</b>   |                     |   |  |      |      |           |               |
| Drain-Source Breakdown Voltage  | $V_{DS}$            | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$   |  | 100  | -    | -         | V             |
| $V_{DS}$ Temperature Coefficient  | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$   |  | -    | 0.13 | -         | V/°C          |
| Gate-Source Threshold Voltage   | $V_{GS(th)}$        | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$   |  | 2.0  | -    | 4.0       | V             |
| Gate-Source Leakage   | $I_{GSS}$           | $V_{GS} = \pm 20\text{ V}$  |  | -    | -    | $\pm 100$ | nA            |
| Zero Gate Voltage Drain Current   | $I_{DSS}$           | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$  |  | -    | -    | 25        | $\mu\text{A}$ |
|   |                     | $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$  |  | -    | -    | 250       |               |
| Drain-Source On-State Resistance  | $R_{DS(on)}$        | $V_{GS} = 10\text{ V}$  | $I_D = 0.78\text{ A}^b$  | -    | -    | 0.27      | $\Omega$      |
| Forward Transconductance  | $g_{fs}$            | $V_{DS} = 50\text{ V}, I_D = 0.78\text{ A}^b$   |  | 0.80 | -    | -         | S             |
| <b>Dynamic</b>  |                     |   |  |      |      |           |               |
| Input Capacitance   | $C_{iss}$           | $V_{GS} = 0\text{ V}$<br>$V_{DS} = 25\text{ V}$<br>$f = 1.0\text{ MHz}$ , see fig. 5  |  | -    | 360  | -         | pF            |
| Output Capacitance  | $C_{oss}$           |   |  | -    | 150  | -         |               |
| Reverse Transfer Capacitance  | $C_{rss}$           |   |  | -    | 34   | -         |               |
| Total Gate Charge   | $Q_g$               | $V_{GS} = 10\text{ V}$  | $I_D = 9.2\text{ A}, V_{DS} = 80\text{ V}$<br>see fig. 6 and 13 <sup>b</sup> | -    | -    | 16        | nC            |
| Gate-Source Charge  | $Q_{gs}$            |   |  | -    | -    | 4.4       |               |
| Gate-Drain Charge   | $Q_{gd}$            |   |  | -    | -    | 7.7       |               |
| Turn-On Delay Time  | $t_{d(on)}$         | $V_{DD} = 50\text{ V}, I_D = 9.2\text{ A}$<br>$R_g = 18\text{ }\Omega, R_D = 5.2\text{ }\Omega$ , see fig. 10 <sup>b</sup>                                      |  | -    | 6.8  | -         | ns            |
| Rise Time   | $t_r$               |   |  | -    | 27   | -         |               |
| Turn-Off Delay Time   | $t_{d(off)}$        |   |  | -    | 18   | -         |               |
| Fall Time   | $t_f$               |   |  | -    | 17   | -         |               |
| Internal Drain Inductance   | $L_D$               | Between lead,<br>6 mm (0.25") from<br>package and center of<br>die contact  |  | -    | 4.0  | -         | nH            |
| Internal Source Inductance  | $L_S$               |   |  | -    | 6.0  | -         |               |
| <b>Drain-Source Body Diode Characteristics</b>                              |                     |   |  |      |      |           |               |
| Continuous Source-Drain Diode Current                                       | $I_S$               | MOSFET symbol<br>showing the<br>integral reverse<br>p - n junction diode    |  | -    | -    | 1.3       | A             |
| Pulsed Diode Forward Current <sup>a</sup>                                   | $I_{SM}$            |   |  | -    | -    | 10        |               |
| Body Diode Voltage  | $V_{SD}$            | $T_J = 25\text{ }^\circ\text{C}, I_S = 1.3\text{ A}, V_{GS} = 0\text{ V}^b$   |  | -    | -    | 2.5       | V             |
| Body Diode Reverse Recovery Time  | $t_{rr}$            | $T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$  |  | -    | 130  | 260       | ns            |
| Body Diode Reverse Recovery Charge  | $Q_{rr}$            |   |  | -    | 0.65 | 1.3       | $\mu\text{C}$ |
| Forward Turn-On Time  | $t_{on}$            | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )   |  |      |      |           |               |

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\text{ }\%$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Fig. 1 - Typical Output Characteristics,  $T_A = 25\text{ }^\circ\text{C}$



Fig. 3 - Typical Transfer Characteristics

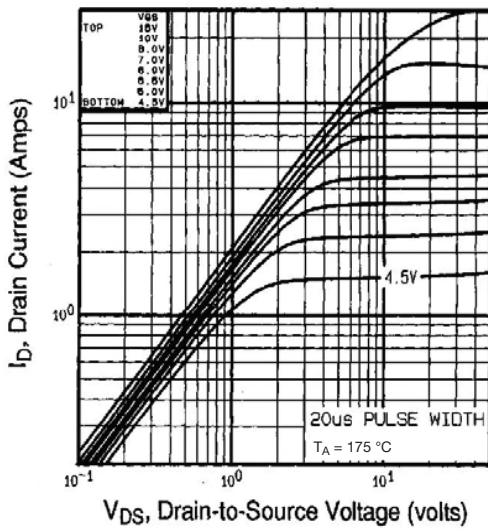


Fig. 2 - Typical Output Characteristics,  $T_A = 175\text{ }^\circ\text{C}$

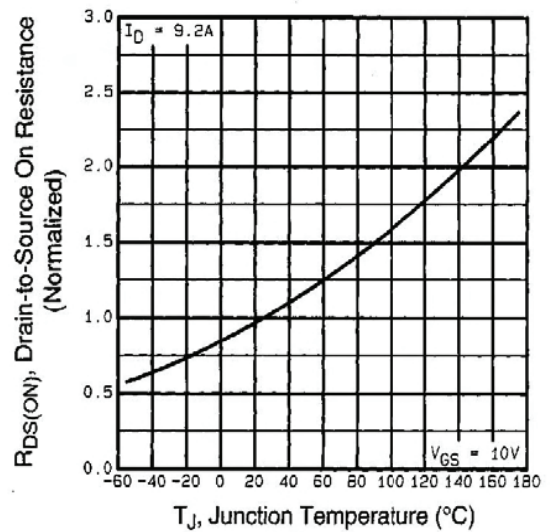


Fig. 4 - Normalized On-Resistance vs. Temperature

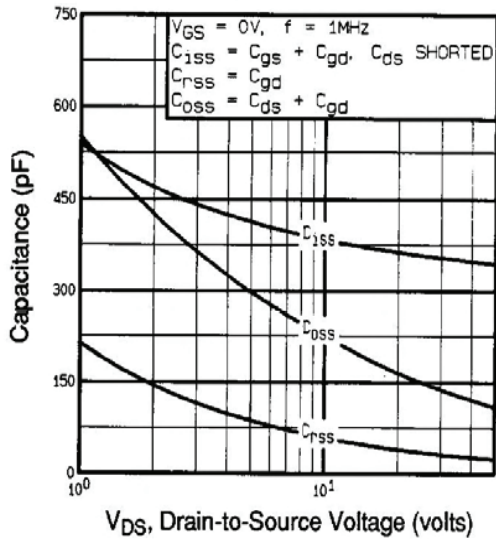


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area

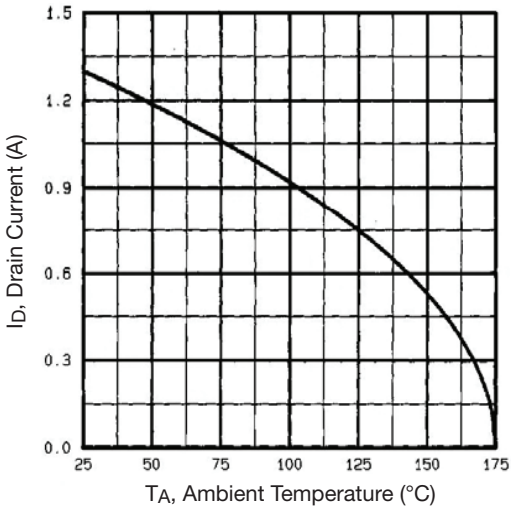


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

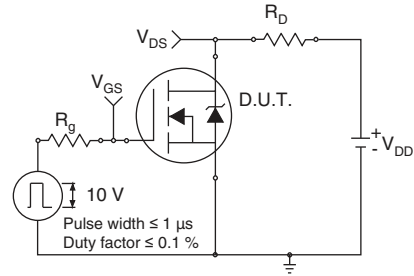


Fig. 10a - Switching Time Test Circuit

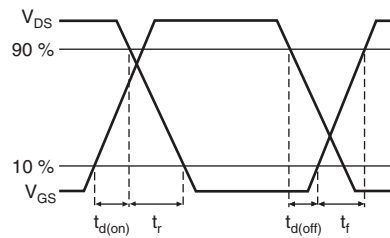


Fig. 10b - Switching Time Waveforms

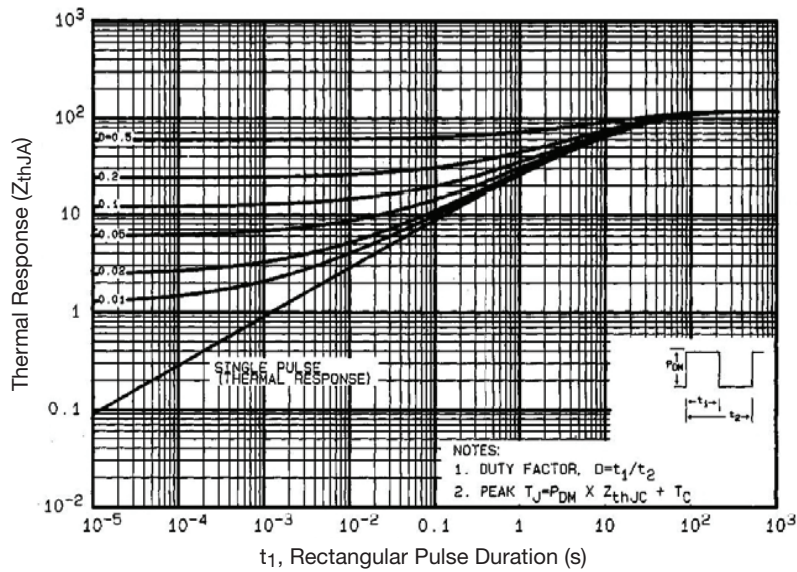


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

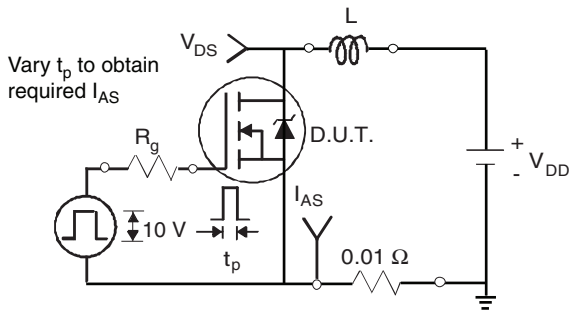


Fig. 12a - Unclamped Inductive Test Circuit

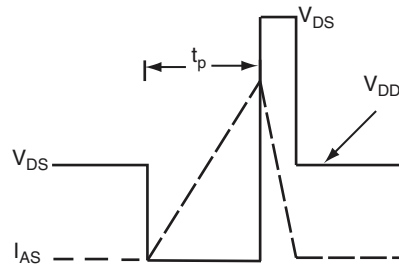


Fig. 12b - Unclamped Inductive Waveforms

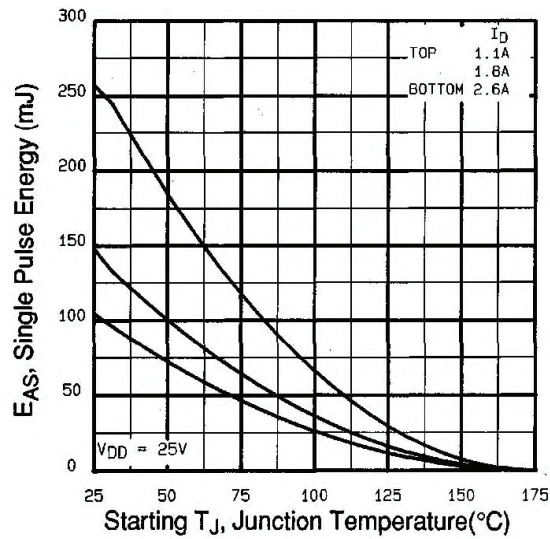


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

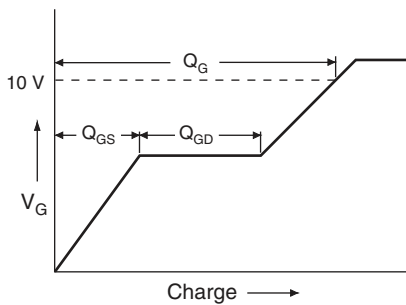


Fig. 13a - Basic Gate Charge Waveform

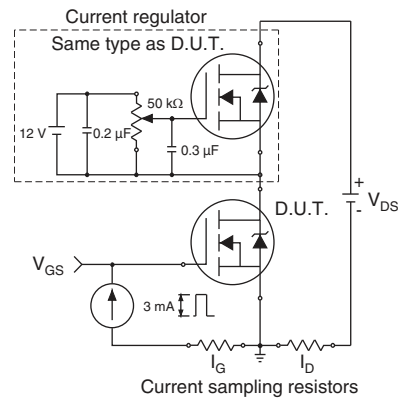


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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## HVM DIP (High voltage)



| DIM. | INCHES |       | MILLIMETERS |       |
|------|--------|-------|-------------|-------|
|      | MIN.   | MAX.  | MIN.        | MAX.  |
| A    | 0.310  | 0.330 | 7.87        | 8.38  |
| E    | 0.300  | 0.425 | 7.62        | 10.79 |
| L    | 0.270  | 0.290 | 6.86        | 7.36  |

ECN: X10-0386-Rev. B, 06-Sep-10  
DWG: 5974

### Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.





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