20-Bit Analog-to-Digital Converter For Bridge Sensors

Check for Samples: ADS1230

FEATURES

- **Complete Front-End for Bridge Sensor**
- **Onboard PGA with Gain of 64 or 128**
- **Onboard Oscillator**
- **RMS Noise:**
  40nV at 10SPS (G = 128)
  88nV at 80SPS (G = 128)
- **18-Bit Noise-Free Resolution**
- **Selectable 10SPS or 80SPS Data Rates**
- **Simultaneous 50Hz and 60Hz Rejection at 10SPS**
- **External Voltage Reference up to 5V for Ratiometric Measurements**
- **Simple, Pin-Driven Control**
- **Two-Wire Serial Digital Interface**
- **Tiny 16-pin TSSOP Package**
- **Supply Range: 2.7V to 5.3V**
- **–40°C to +85°C Temperature Range**

APPLICATIONS

- **Weigh Scales**
- **Strain Gauges**
- **Pressure Sensors**
- **Industrial Process Control**

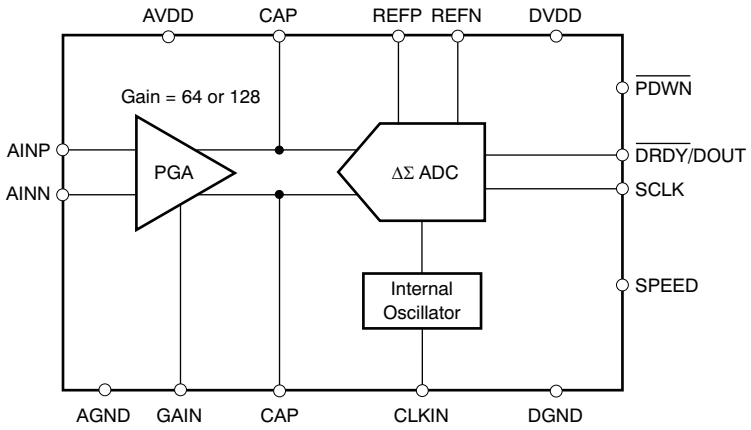
DESCRIPTION

The ADS1230 is a precision 20-bit analog-to-digital converter (ADC). With an onboard low-noise programmable gain amplifier (PGA), onboard oscillator, and precision 20-bit delta-sigma ADC, the ADS1230 provides a complete front-end solution for bridge sensor applications including weigh scales, strain gauges, and pressure sensors.

The low-noise PGA has a gain of 64 or 128, supporting a full-scale differential input of ±39mV or ±19.5mV, respectively. The delta-sigma ADC has 20-bit effective resolution and is comprised of a 3rd-order modulator and 4th-order digital filter. Two data rates are supported: 10SPS (with both 50Hz and 60Hz rejection) and 80SPS. The ADS1230 can be clocked by the internal oscillator or an external clock source. Offset calibration is performed on-demand, and the ADS1230 can be put in a low-power standby mode or shut off completely in power-down mode.

All of the features of the ADS1230 are controlled by dedicated pins; there are no digital registers to program. Data are output over an easily-isolated serial interface that connects directly to the MSP430 and other microcontrollers.

The ADS1230 is available in a TSSOP-16 package and is specified from –40°C to +85°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	ADS1230	UNIT
AVDD to AGND	–0.3 to +6	V
DVDD to DGND	–0.3 to +6	V
AGND to DGND	–0.3 to +0.3	V
Input Current	100, Momentary	mA
	10, Continuous	mA
Analog Input Voltage to AGND	–0.3 to AVDD + 0.3	V
Digital Input Voltage to DGND	–0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–60 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = –40°C to +85°C, AVDD = DVDD = REFP = +5V, REFN = AGND, and Gain = 64, unless otherwise noted.

PARAMETER		CONDITIONS		ADS1230 MIN	ADS1230 TYP	ADS1230 MAX	UNIT
Analog Inputs							
Full-Scale Input Voltage (AINP – AINN)					±0.5V_{REF}/PGA		V
Common-Mode Input Range				AGND + 1.5V		AVDD – 1.5V	V
Differential Input Current					±2		nA
System Performance							
Resolution		No Missing Codes		20			Bits
Data Rate		Internal Oscillator, SPEED = High			80		SPS
		Internal Oscillator, SPEED = Low			10		SPS
		External Oscillator, SPEED = High			f_{CLK}/61,440		SPS
		External Oscillator, SPEED = Low			f_{CLK}/491,520		SPS
Digital Filter Settling Time		Full Settling			4		Conversions
Integral Nonlinearity (INL)		Differential Input, End-Point Fit, G = 64			±10		ppm
		Differential Input, End-Point Fit, G = 128			±6		ppm
Input Offset Error(1)					±3		ppm of FS
Input Offset Drift					±10		nV/°C
Gain Error					±0.8		%
Gain Drift					±4		ppm/°C
Normal-Mode Rejection(2)		f_{IN} = 50Hz or 60Hz ±1Hz, f_{DATA} = 10SPS	Internal Oscillator	80	90		dB
			External Oscillator(3)	90	100		dB
Common-Mode Rejection		at DC, AVDD = 0.1V			110		dB
Input-Referred Noise		f_{DATA} = 10SPS			53		nV, rms
		f_{DATA} = 80SPS			100		nV, rms
Power-Supply Rejection		at DC, AVDD = 0.1V		90	100		dB
Voltage Reference Input							
Voltage Reference Input (V_{REF})		V_{REF} = REFP – REFN		1.5	AVDD	AVDD + 0.1V	V
Negative Reference Input (REFN)				AGND – 0.1		REFP – 1.5	V
Positive Reference Input (REFP)				REFN + 1.5		AVDD + 0.1	V
Voltage Reference Input Current					10		nA
Digital							
Logic Levels	V_{IH}	All digital inputs except CLKIN		0.7 DVDD		DVDD + 0.1	V
	V_{IH}	CLKIN		0.7 DVDD		5.1	V
	V_{IL}			DGND		0.2 DVDD	V
	V_{OH}	I_{OH} = 1mA		DVDD – 0.4			V
	V_{OL}	I_{OL} = 1mA				0.2 DVDD	V
Input Leakage		0 < V_{IN} < DVDD				±10	µA
External Clock Input Frequency (f_{CLKIN})				0.2	4.9152	6	MHz
Serial Clock Input Frequency (f_{SCLK})						5	MHz

(1) Offset calibration can minimize these errors to the level of noise at any temperature.
(2) Specification is assured by the combination of design and final production test.
(3) External oscillator = 4.9152MHz.

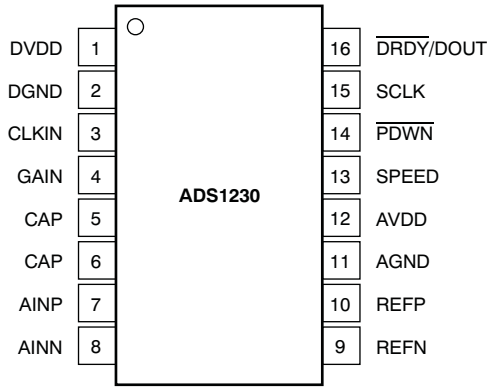
ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –40°C to +85°C, AVDD = DVDD = REFP = +5V, REFN = AGND, and Gain = 64, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1230			UNIT
		MIN	TYP	MAX	
Power Supply					
Power-Supply Voltage (AVDD, DVDD)		2.7		5.3	V
Analog Supply Current	Normal Mode, AVDD = 3V		900	1400	µA
	Normal Mode, AVDD = 5V		900	1400	µA
	Standby Mode		0.1	1	µA
	Power-Down		0.1	1	µA
Digital Supply Current	Normal Mode, DVDD = 3V		60	100	µA
	Normal mode, DVDD = 5V		95	140	µA
	Standby Mode, SCLK = High, DVDD = 3V		45	65	µA
	Standby Mode, SCLK = High, DVDD = 5V		65	80	µA
	Power-Down		0.2		µA
Power Dissipation, Total	Normal Mode, AVDD = DVDD = 3V		2.9	4.5	mW
	Normal Mode, AVDD = DVDD = 5V		5.0	7.7	mW
	Standby Mode, AVDD = DVDD = 5V		0.3	0.4	mW

PIN CONFIGURATION

PW PACKAGE
TSSOP-16
(Top View)



PIN DESCRIPTIONS

NAME	TERMINAL	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
DVDD	1	Digital	Digital Power Supply: 2.7V to 5.3V
DGND	2	Digital	Digital Ground
CLKIN	3	Digital/Digital Input	External Clock Input: typically 4.9152MHz. Tie low to activate internal oscillator.
GAIN	4	Digital Input	PGA Gain Select **GAIN** / **PGA** 0 / 64 1 / 128
CAP	5	Analog	Gain Amp Bypass Capacitor Connection
CAP	6	Analog	Gain Amp Bypass Capacitor Connection
AINP	7	Analog Input	Positive Analog Input
AINN	8	Analog Input	Negative Analog Input
REFN	9	Analog Input	Negative Reference Input
REFP	10	Analog Input	Positive Reference Input
AGND	11	Analog	Analog Ground
AVDD	12	Analog	Analog Power Supply, 2.7V to 5.3V
SPEED	13	Digital Input	Data Rate Select: **SPEED** / **DATA RATE** 0 / 10SPS 1 / 80SPS
$\overline{\text{PDWN}}$	14	Digital Input	Power-Down: Holding this pin low powers down the entire converter and resets the ADC.
SCLK	15	Digital Input	Serial Clock: Clock out data on the rising edge. Also used to initiate Offset Calibration and Sleep modes. See the Offset Calibration, Standby Mode, and Standby Mode with Offset Calibration sections for more details.
$\overline{\text{DRDY}}$/DOUT	16	Digital Output	Dual-Purpose Output: Data Ready: Indicates valid data by going low. Data Output: Outputs data, MSB first, on the first rising edge of SCLK.

NOISE PERFORMANCE

The ADS1230 offers outstanding noise performance. Table 1 summarizes the typical noise performance with inputs shorted externally for different data rates and voltage reference values.

The RMS and Peak-to-Peak noise are referred to the input. The effective number of bits (ENOB) is defined as:

ENOB = ln (FSR/RMS noise)/ln(2)

The Noise-Free Bits are defined as:

Noise-Free Bits = ln (FSR/Peak-to-Peak Noise)/ln(2)

Where:

FSR (Full-Scale Range) = V_{REF}/Gain.

Table 1. Noise Performance for AV_{DD} = 5V and V_{REF} = 5V

DATA RATE	GAIN	RMS NOISE (nV)	PEAK-TO-PEAK NOISE(1) (nV)	ENOB (RMS)	NOISE-FREE BITS
10	64	53	290	20.5	18
	128	40	198	19.8	17.5
80	64	100	480	19.5	17.3
	128	88	480	18.7	16.3

(1) Peak-to-peak data are based on direct measurement.

Table 2. Noise Performance for AV_{DD} = 3V and V_{REF} = 3V

DATA RATE	GAIN	RMS NOISE (nV)	PEAK-TO-PEAK NOISE(1) (nV)	ENOB (RMS)	NOISE-FREE BITS
10	64	46	290	20.6	18
	128	49	259	19.6	17.2
80	64	100	576	19.5	17
	128	102	461	18.5	16.3

(1) Peak-to-peak data are based on direct measurement.

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = DVDD = REFP = 5V, and REFN = AGND, unless otherwise noted.

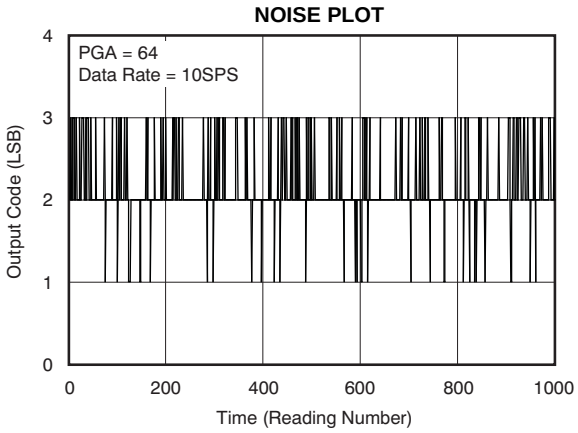


Figure 1.

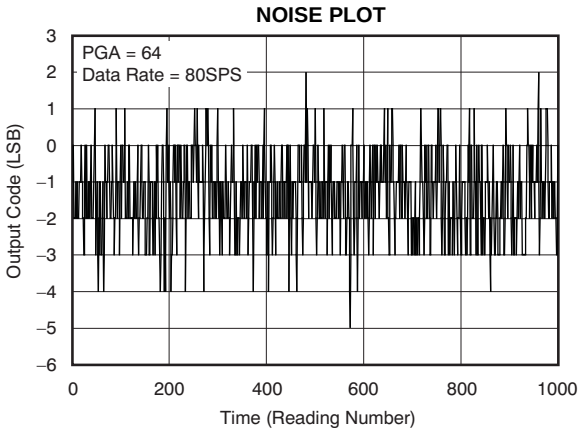


Figure 2.

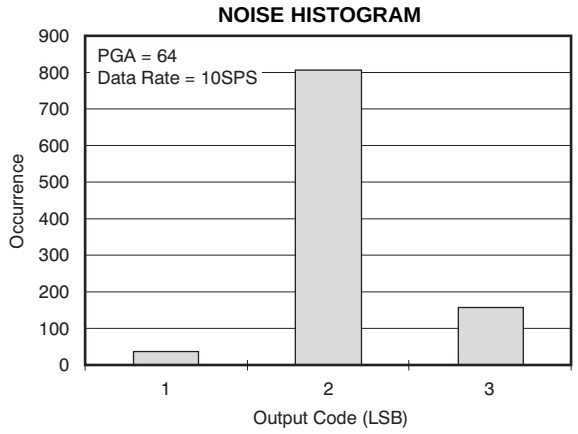


Figure 3.

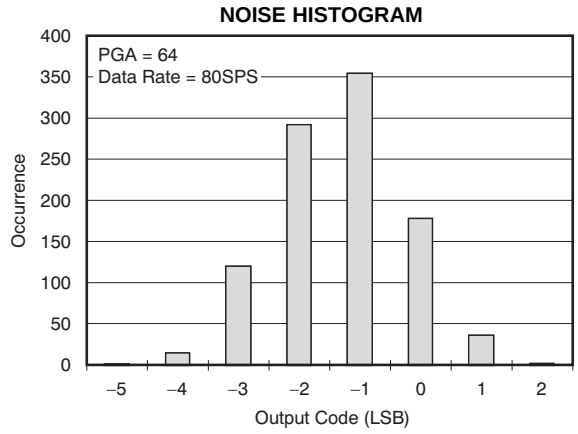


Figure 4.

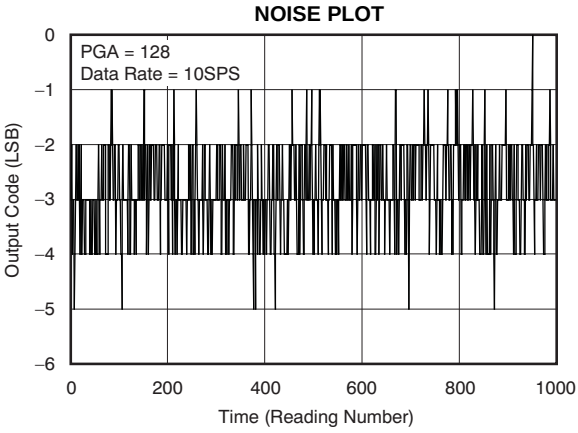


Figure 5.

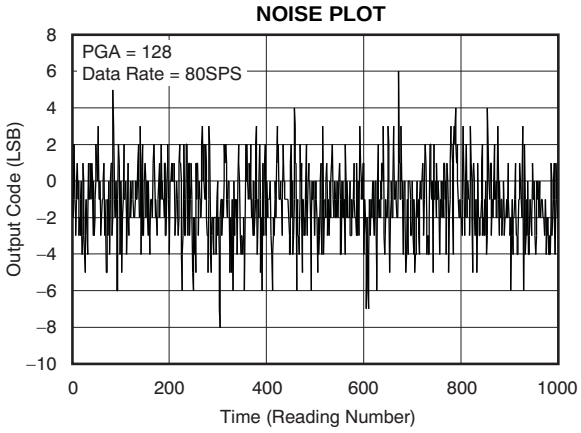


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = DVDD = REFP = 5V, and REFN = AGND, unless otherwise noted.

NOISE HISTOGRAM

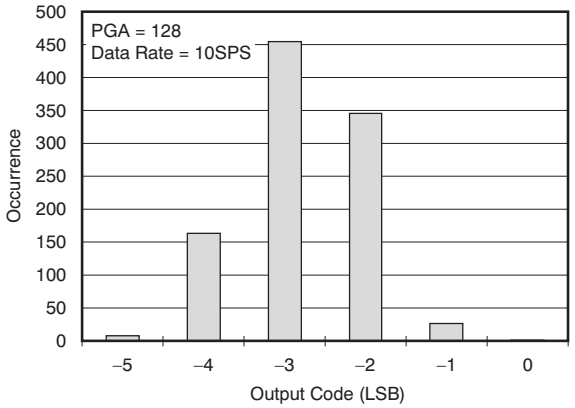


Figure 7.

NOISE HISTOGRAM

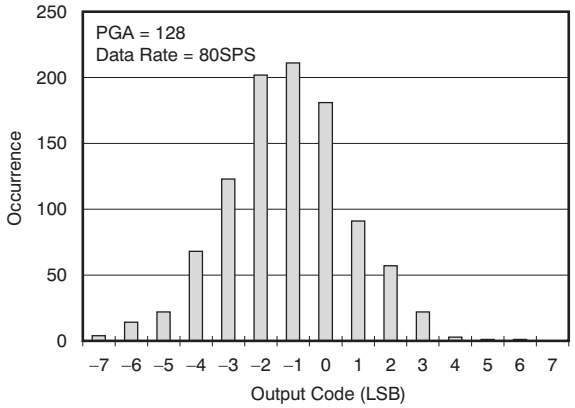


Figure 8.

OFFSET vs TEMPERATURE

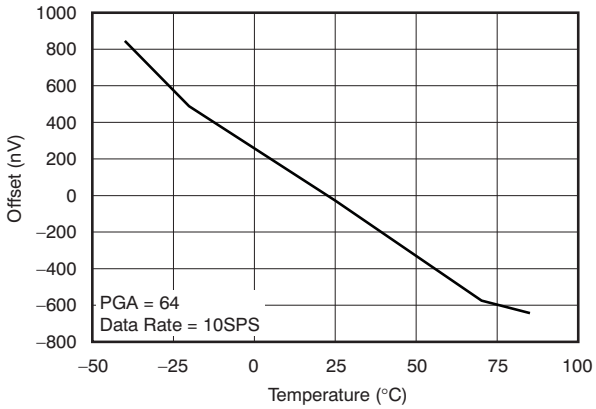


Figure 9.

GAIN ERROR vs TEMPERATURE

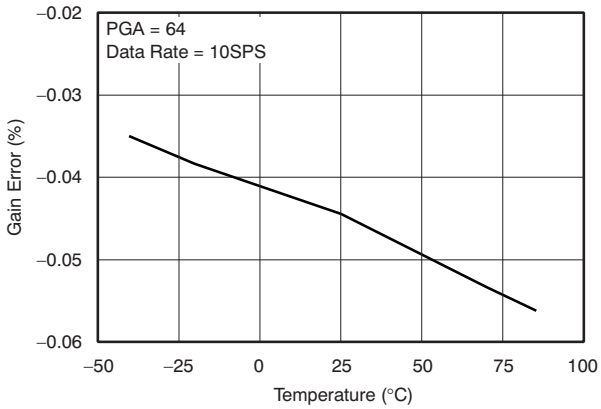


Figure 10.

NOISE vs INPUT SIGNAL

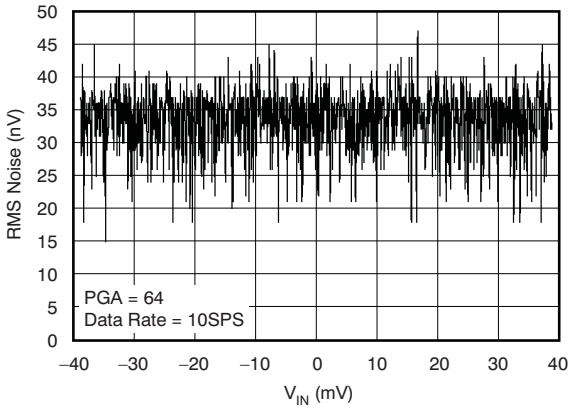


Figure 11.

NOISE vs INPUT SIGNAL

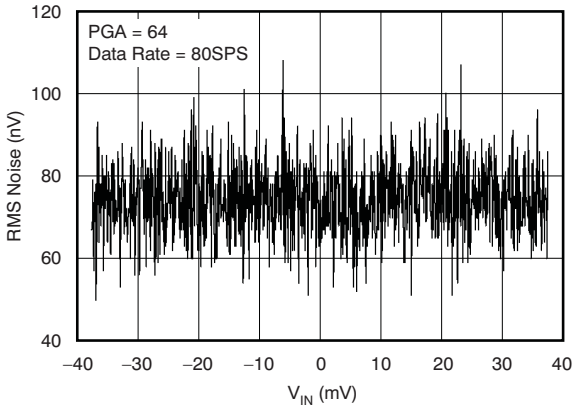


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = DVDD = REFP = 5V, and REFN = AGND, unless otherwise noted.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

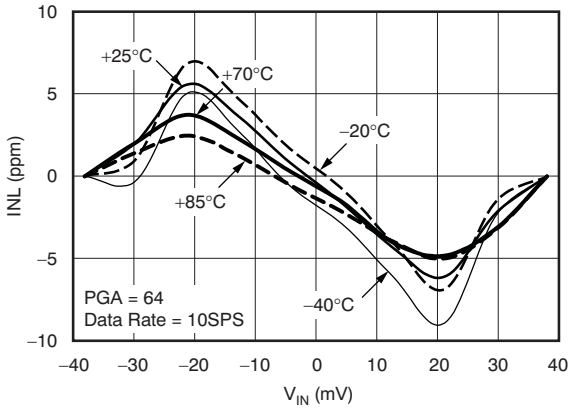


Figure 13.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

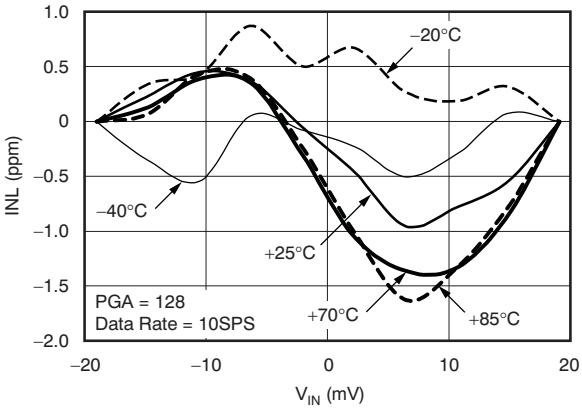


Figure 14.

ANALOG CURRENT vs TEMPERATURE (Normal Mode)

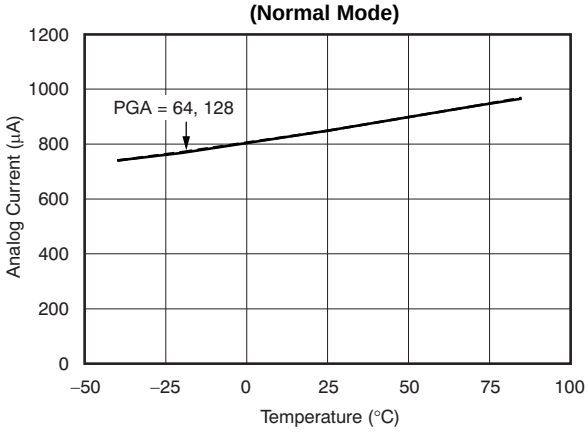


Figure 15.

DIGITAL CURRENT vs TEMPERATURE (Normal Mode)

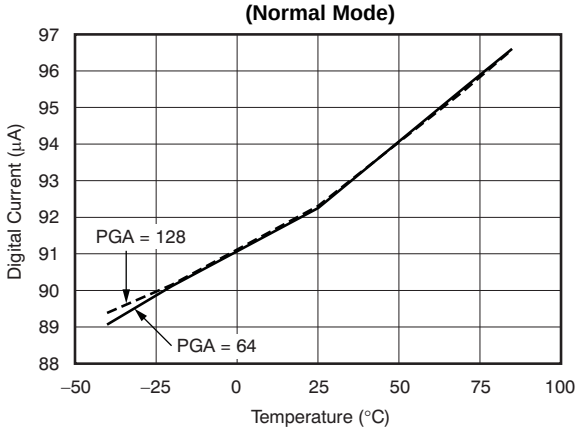


Figure 16.

DATA RATE vs TEMPERATURE

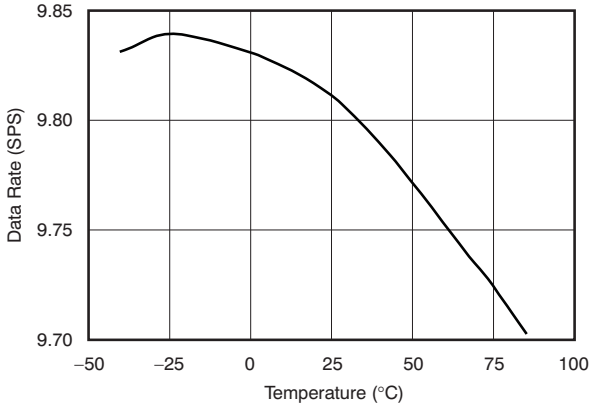


Figure 17.

OVERVIEW

The ADS1230 is a precision, 20-bit ADC that includes a low-noise PGA, internal oscillator, third-order delta-sigma (ΔΣ) modulator, and fourth-order digital filter. The ADS1230 provides a complete front-end solution for bridge sensor applications such as weigh scales, strain guages, and pressure sensors.

Clocking can be supplied by an external clock or by a precision internal oscillator. Data can be output at 10SPS for excellent 50Hz and 60Hz rejection, or at 80SPS when higher speeds are needed. The ADS1230 is easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1230 accepts differential input signals, but can also measure unipolar signals. When measuring unipolar (or single-ended signals) with respect to ground, connect the negative input (AINN) to ground and connect the input signal to the positive input (AINP). Note that when the ADS1230 is configured this way, only half of the converter full-scale range is used, since only positive digital output codes are produced.

LOW-NOISE PGA

The ADS1230 features a low-drift, low-noise PGA that provides a complete front-end solution for bridge sensors. A simplified diagram of the PGA is shown in Figure 18. It consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately-matched resistors (R_1, R_{F1}, and R_{F2}), which construct a differential front-end stage with a gain of 64, followed by gain stage A3 (Gain = 1 or 2). The PGA inputs are equipped with an EMI filter, as shown in Figure 18. The cutoff frequency of the EMI filter is 19.6MHz. By using AVDD as the reference input, the bipolar input ranges from –39mV to +39mV (Gain = 64) or –19.5mV to +19.5mV (Gain = 128), and the unipolar input ranges from 0mV to +39mV (Gain = 64) or 0mV to +19.5mV (Gain = 128). The inputs of the ADS1230 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry.

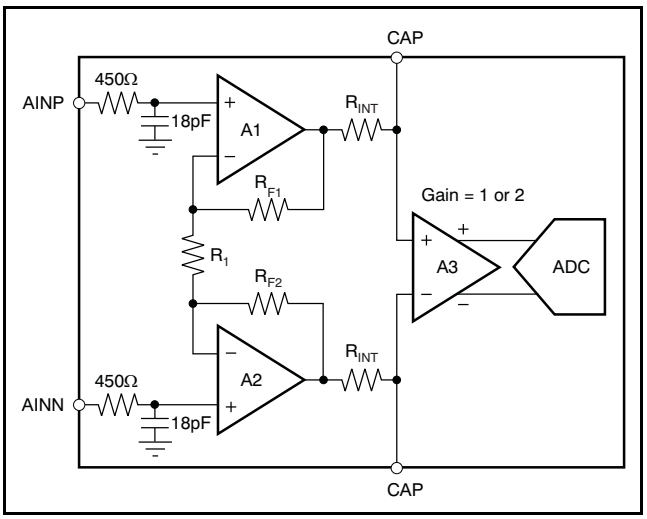


Figure 18. Simplified Diagram of the PGA

Bypass Capacitor

By applying a 0.1μF external capacitor (C_{EXT}) across two capacitor pins combined with the internal 2kΩ resistor R_{INT} (on-chip), a low-pass filter with a corner frequency of 720Hz is created to bandlimit the signal path before the modulator input. This low-pass filter serves two purposes. First, the input signal is bandlimited to prevent aliasing as well as to filter out the high-frequency noise. Second, it attenuates the chopping residue from the amplifier to improve temperature drift performance. It is not required to use high-quality capacitors (such as ceramic or tantalum capacitors) for a general application. However, high-quality capacitors such as poly are recommended for high-linearity applications.

VOLTAGE REFERENCE INPUTS (REFP, REFN)

The voltage reference used by the modulator is generated from the voltage difference between REFP and REFN: V_{REF} = REFP – REFN. The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, a switching buffer circuitry is used to reduce the input equivalent capacitance. The reference drift and noise impact ADC performance. In order to achieve best results, pay close attention to the reference noise and drift specifications. A simplified diagram of the circuitry on the reference inputs is shown in Figure 19. The switches and capacitors can be modeled approximately using an effective impedance of:

$$Z_{EFF} = \frac{1}{2f_{MOD}C_{BUF}}$$

Where:

f_{MOD} = modulator sampling frequency (76.8kHz)
C_{BUF} = input capacitance of the buffer

For the ADS1230:

$$Z_{EFF} = \frac{1}{(2)(76.8kHz)(13fF)} = 500M\Omega$$

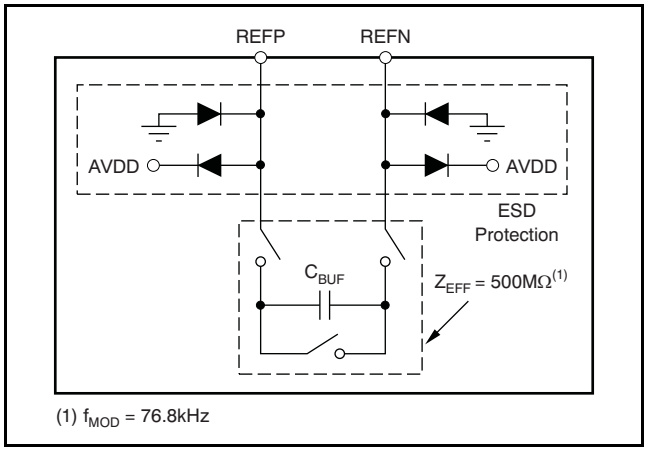


Figure 19. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

GND – 100mV < (REFP or REFN) < AVDD + 100mV

CLOCK SOURCES

The ADS1230 can use an external clock source or internal oscillator to accommodate a wide variety of applications. Figure 20 shows the equivalent circuitry of the clock source. The CLK_DETECT block determines whether the crystal oscillator/external clock signal is applied to the CLKIN pin so that the internal oscillator is bypassed or activated. When the CLKIN pin frequency is above ~200kHz, the CLK_DETECT output goes low and shuts down the internal oscillator. When the CLKIN pin frequency is below ~200kHz, the CLK_DETECT output goes high and activates the internal oscillator. It is highly recommended to hard-wire the CLKIN pin to ground when the internal oscillator is chosen.

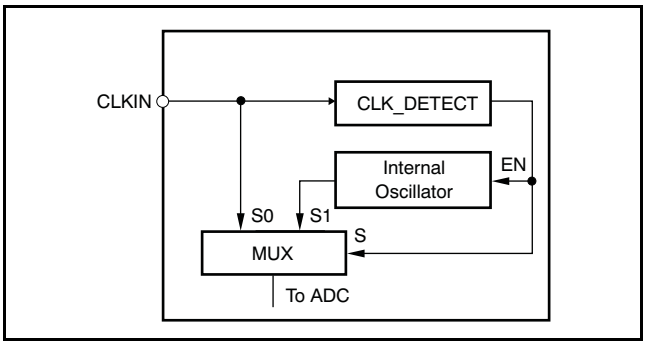


Figure 20. Equivalent Circuitry of the Clock Source

An external clock may be used by driving the CLKIN pin directly. The Electrical Characteristics table shows the allowable frequency range. The clock input may be driven with 5V logic, regardless of the DVDD or AVDD voltage.

FREQUENCY RESPONSE

The ADS1230 uses a sinc^4 digital filter with the frequency response (f_{CLK} = 4.9152MHz) shown in Figure 21. The frequency response repeats at multiples of the modulator sampling frequency of 76.8kHz. The overall response is that of a low-pass filter with a –3dB cutoff frequency of 3.32Hz with the SPEED pin tied low (10SPS data rate) and 11.64Hz with the SPEED pin tied high (80SPS data rate).

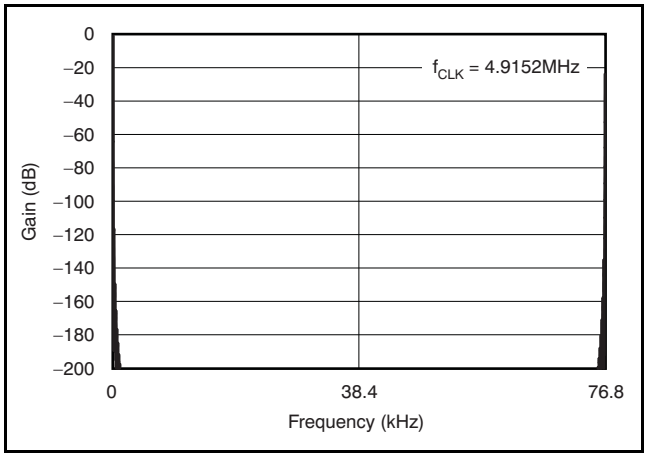


Figure 21. Frequency Response

To help see the response at lower frequencies, Figure 22(a) illustrates the response out to 100Hz, when the data rate = 10SPS. Notice that signals at multiples of 10Hz are rejected, and therefore simultaneous rejection of 50Hz and 60Hz is achieved.

The benefit of using a sinc^4 filter is that every frequency notch has four zeros on the same location. This response, combined with the low drift internal oscillator, provides an excellent normal-mode rejection of line-cycle interference.

Figure 22(b) shows the same plot, but zooms in on the 50Hz and 60Hz notches with the SPEED pin tied low (10SPS data rate). With only a ±3% variation of the internal oscillator, over 100dB of normal-mode rejection is achieved.

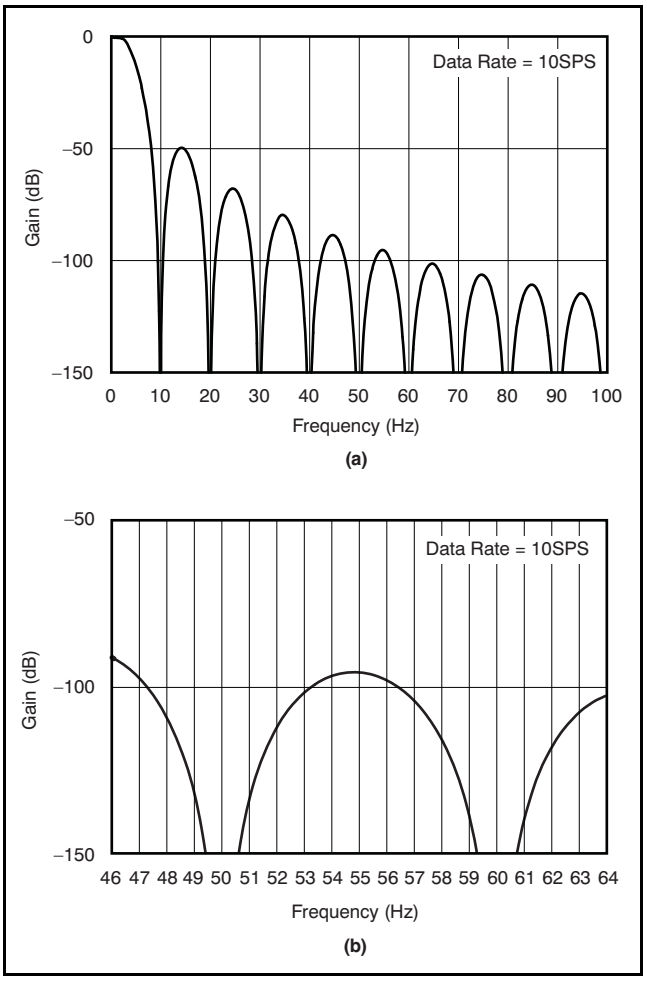


Figure 22. Frequency Response Out To 100Hz

The ADS1230 data rate and frequency response scale directly with clock frequency. For example, if f_{CLK} increases from 4.9152MHz to 6.144MHz when the SPEED pin is tied high, the data rate increases from 80SPS to 100SPS, while notches also increase from 80Hz to 100Hz. Note that these changes are only possible when the external clock source is applied.

SETTLING TIME

In certain instances, large changes in input will require settling time. For example, an external multiplexer in front of the ADS1230 can put large changes in input voltage by simply switching the multiplexer input channels. Abrupt changes in the input will require four data conversion cycles to settle. When continuously converting, five readings may be necessary in order to settle the data. If the change in input occurs in the middle of the first conversion, four more full conversions of the fully-settled input are required to get fully-settled data. Discard the first four readings because they contain only partially-settled data. Figure 23 illustrates the settling time for the ADS1230 in Continuous Conversion mode.

DATA RATE

The ADS1230 data rate is set by the SPEED pin, as shown in Table 3. When SPEED is low, the data rate is nominally 10SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of nominally 80SPS.

Table 3. Data Rate Settings

SPEED PIN	DATA RATE	
	Internal Oscillator or 4.9152MHz Crystal	External Oscillator
0	10SPS	f_{CLKIN} / 491,520
1	80SPS	f_{CLKIN} / 61,440

DATA FORMAT

The ADS1230 outputs 20 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of $0.5V_{REF}/(2^{19} - 1)$. The positive full-scale input produces an output code of 7FFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 4 summarizes the ideal output codes for different input signals.

The ADS1230 is a 20-bit ADC. After data conversion is completed, applying 20 SCLKs retrieves 20 bits of data (MSB first). However, if the SCLKs continue to be applied after 20 bits of data are retrieved, the DOUT pin outputs four 1s for the 21st through the 24th SCLK, as shown in Figure 24.

Table 4. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT
≥ $+0.5V_{REF}$/Gain	7FFFFh
$(+0.5V_{REF}/Gain)/(2^{19} - 1)$	00001h
0	00000h
$(-0.5V_{REF}/Gain)/(2^{19} - 1)$	FFFFFh
≤ $-0.5V_{REF}$/Gain	80000h

(1) Excludes effects of noise, INL, offset, and gain errors.

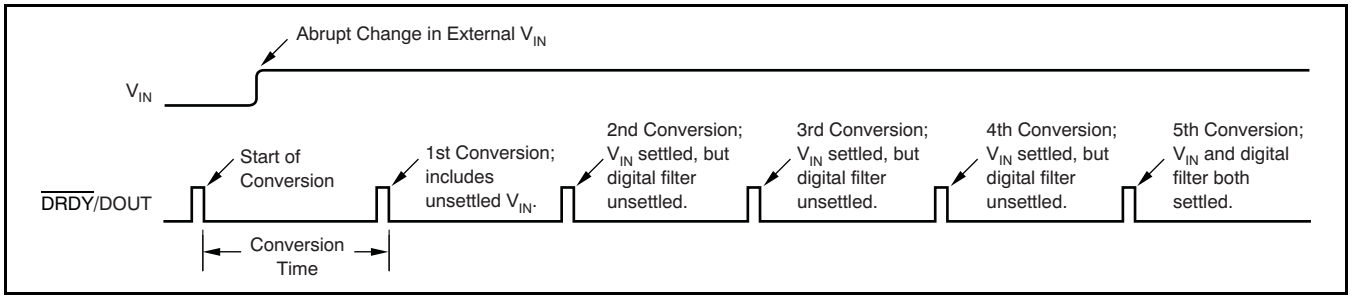


Figure 23. Settling Time in Continuous Conversion Mode

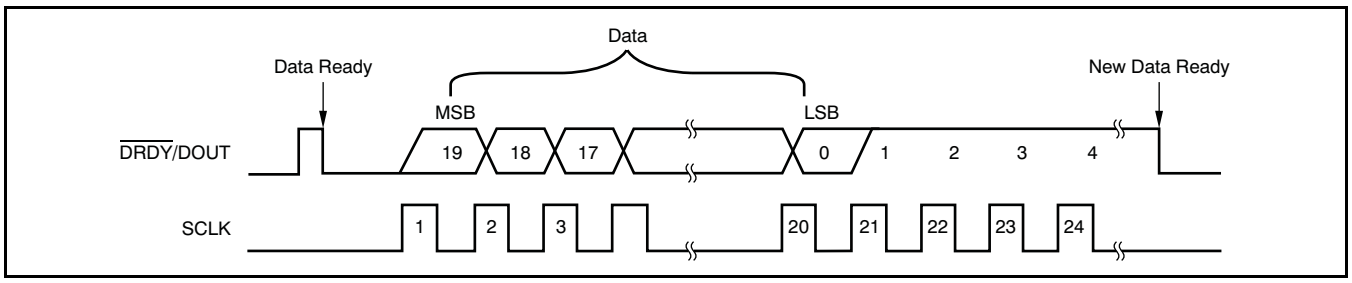


Figure 24. Data Retrieval Format

DATA READY/DATA OUTPUT (DRDY/DOUT)

This digital output pin serves two purposes. First, it indicates when new data are ready by going low. Afterwards, on the first rising edge of SCLK, the DRDY/DOUT pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all 20 bits have been retrieved, the pin can be forced high with an additional SCLK. It then stays high until new data are ready. This configuration is useful when polling on the status of DRDY/DOUT to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise and fall times of SCLK are both less than 50ns.

DATA RETRIEVAL

The ADS1230 continuously converts the analog input signal. To retrieve data, wait until DRDY/DOUT goes low, as shown in Figure 25. After DRDY/DOUT goes low, begin shifting out the data by applying SCLKs. Data are shifted out MSB first. It is not required to shift out all 20 bits of data, but the data must be retrieved before new data are updated (within t_{CONV}) or else the data will be overwritten. Avoid data retrieval during the update period (t_{UPDATE}). If 24 SCLKs have been applied, DRDY/DOUT will be high since the last four bits have been appended by '1'. However, if only 20 SCLKs have been applied, DRDY/DOUT remains at the state of the last bit shifted out until it is taken high (see t_{UPDATE}), indicating that new data are being updated. To avoid having DRDY/DOUT remain in the state of the last bit, the 21st SCLK can be applied to force DRDY/DOUT high, as shown in Figure 26. This technique is useful when a host controlling the device is polling DRDY/DOUT to determine when data are ready.

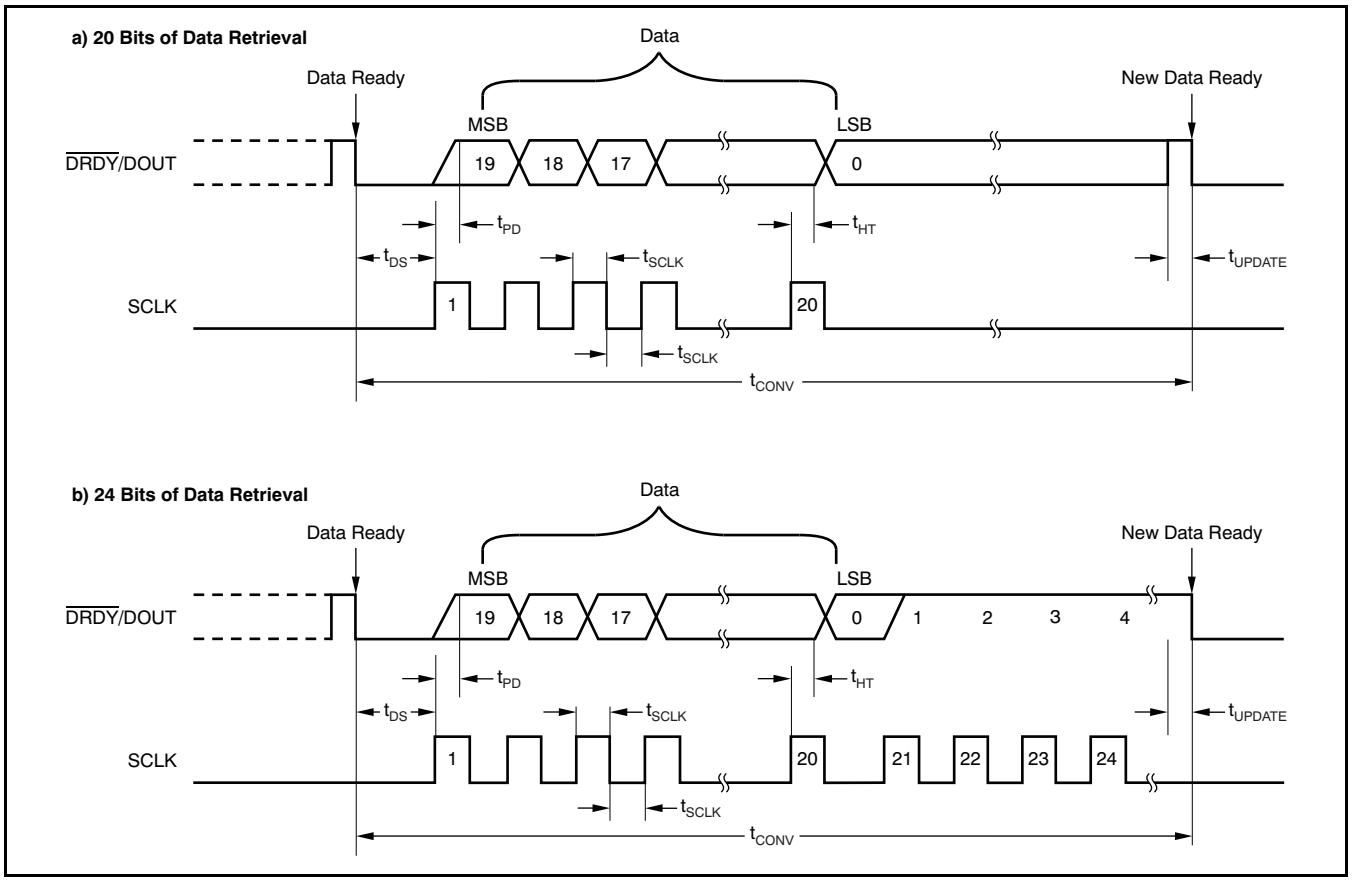


Figure 25. Data Retrieval Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t_{DS}	$\overline{DRDY}$/DOUT low to first SCLK rising edge		0			ns
t_{SCLK}	SCLK positive or negative pulse width		100			ns
t_{PD}	SCLK rising edge to new data bit valid: propagation delay				50	ns
t_{HT}	SCLK rising edge to old data bit valid: hold time		0			ns
t_{UPDATE}	Data updating: no readback allowed		39			µs
t_{CONV}	Conversion time (1/data rate)	SPEED = 1		12.5		ms
		SPEED = 0		100		ms

(1) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

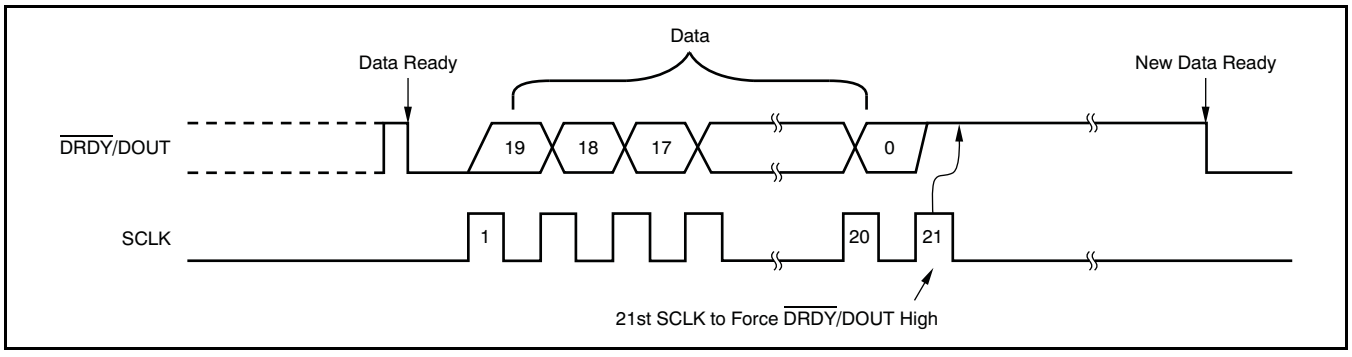


Figure 26. Data Retrieval with $\overline{DRDY}$/DOUT Forced High Afterwards

OFFSET CALIBRATION

Offset calibration can be initiated at any time to remove the ADS1230 inherited offset error. To initiate offset calibration, apply at least two additional SCLKs after retrieving 20 bits of data plus four bits of '1'. Figure 27 shows the timing pattern. The 25th SCLK keeps DRDY/DOUT high. The falling edge of the 26th SCLK begins the calibration cycle. Additional SCLK pulses may be sent after the 26th SCLK; however, activity on SCLK should be minimized during offset calibration for best results.

During this time, the analog input pins are disconnected within the ADC and the appropriate signal is applied internally to perform the calibration. When the calibration is completed, DRDY/DOUT goes low, indicating that new data are ready. The first conversion after a calibration is fully settled and valid for use. The offset calibration takes exactly the same time as specified in (t_{CAL}) immediately after the falling edge of the 26th SCLK.

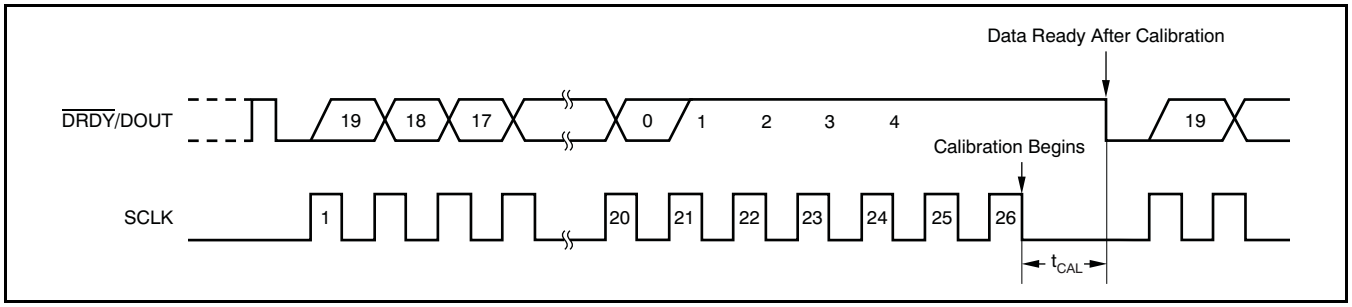


Figure 27. Offset-Calibration Timing

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
t_{CAL} (1)	First data ready after calibration	SPEED = 1	101.28	101.29	ms
		SPEED = 0	801.02	801.03	ms

(1) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

STANDBY MODE

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. In Standby mode, the entire analog circuitry is powered down and only the clock source circuitry is awake to reduce the wake-up time from the Standby mode. To enter Standby mode, simply hold SCLK high after DRDY/DOUT goes low; see Figure 28. Standby mode can be initiated at any time during readback; it is not necessary to retrieve all 20 bits of data beforehand.

When $t_{STANDBY}$ has passed with SCLK held high, Standby mode activates. DRDY/DOUT stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wakeup), set SCLK low. The first data after exiting Standby mode is valid.

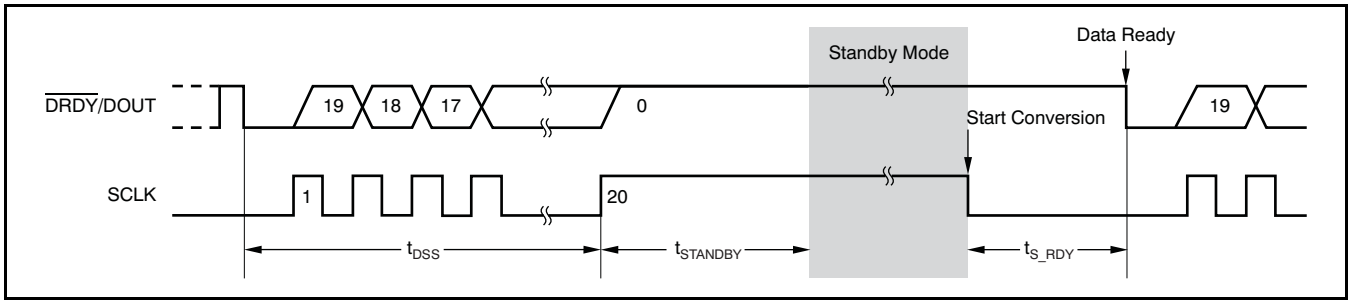


Figure 28. Standby Mode Timing (can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
t_{DSS} (1)	SCLK high after DRDY/DOUT goes low to activate Standby mode	SPEED = 1	0	12.44	ms
		SPEED = 0	0	99.94	ms
$t_{STANDBY}$ (1)	Standby mode activation time	SPEED = 1	20		µs
		SPEED = 0	20		µs
t_{S_RDY} (1)	Data ready after exiting Standby mode	SPEED = 1	52.51	52.51	ms
		SPEED = 0	401.8	401.8	ms

(1) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

STANDBY MODE WITH OFFSET-CALIBRATION

Offset-calibration can be set to run immediately after exiting Standby mode. This option is useful when the ADS1230 is put in Standby mode for long periods of time, and offset-calibration is desired afterwards to compensate for temperature or supply voltage changes.

To force an offset-calibration with Standby mode, shift 25 SCLKs and bring the SCLK pin high to enter Standby mode. Offset-calibration then begins after wake-up; Figure 29 shows the appropriate timing. Note the extra time needed after wake-up for calibration before data are ready. The first data after Standby mode with offset-calibration is fully settled and can be used right away.

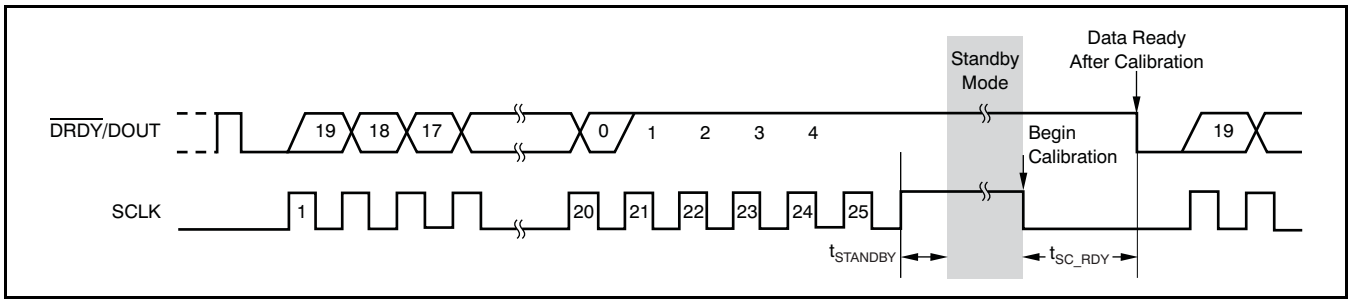


Figure 29. Standby Mode with Offset-Calibration Timing (can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
t_{SC_RDY} (1)	Data ready after exiting Standby mode and calibration	SPEED = 1	103	103	ms
		SPEED = 0	803	803	ms

(1) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

POWER-UP SEQUENCE

When powering up the ADS1230, AVDD and DVDD must be powered up before the PDWN pin goes high, as shown in Figure 30. If PDWN is not controlled by a microprocessor, a simple RC delay circuit must be implemented, as shown in Figure 31.

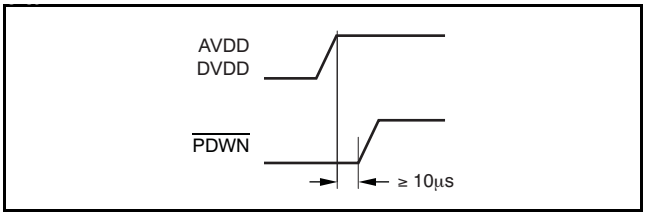


Figure 30. Power-Up Timing Sequence

POWER-DOWN MODE

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter Power-Down mode, simply hold the PDWN pin low. Power-Down mode also resets the entire circuitry to free the ADC circuitry from locking up to an unknown state. Power-Down mode can be initiated at any time during readback; it is not necessary to retrieve all 20 bits of data beforehand. Figure 32 shows the wake-up timing from Power-Down mode.

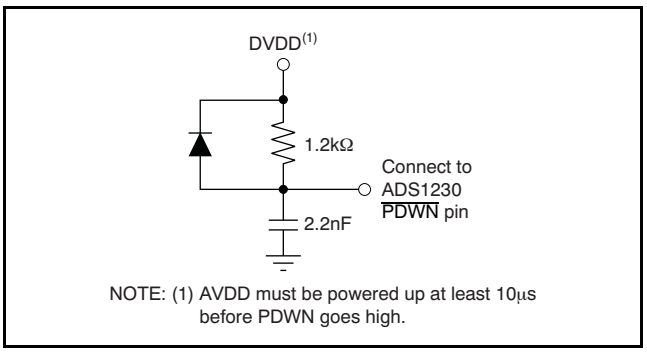


Figure 31. RC Delay Circuit

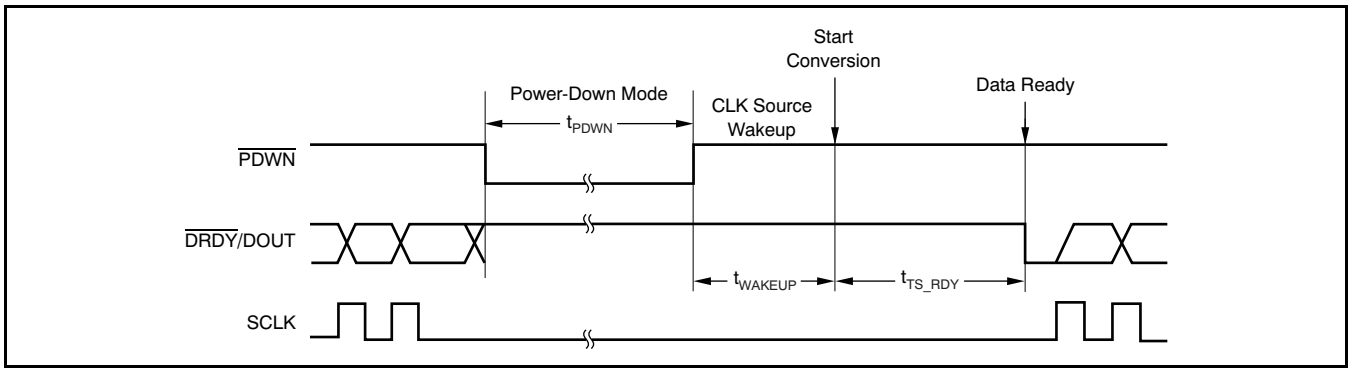


Figure 32. Wake-Up Timing from Power-Down Mode

SYMBOL	DESCRIPTION		MIN	TYP	UNITS
t_{WAKEUP}	Wake-up time after Power-Down mode	Internal clock		7.95	µs
		External clock		0.16	µs
t_{PDWN} (1)	PDWN pulse width		26		µs

(1) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

APPLICATION EXAMPLES

Weigh Scale System

Figure 33 shows a typical ADS1230 hook-up as part of a weigh scale system. In this setup, the ADS1230 is configured at a 10SPS data rate. Note that the internal oscillator is used by grounding the CLKIN pin. The user can also apply a 4.9152MHz clock to the CLKIN pin. For a typical 2mV/V load cell, the maximum output signal is approximately 10mV for a single +5V excitation voltage. The ADS1230 can achieve 17.5 noise-free bits at 10SPS when PGA = 128. With the extra software filtering/averaging (typically done by a microprocessor), an extra bit can be expected.

$$\text{Noise-Free Counts} = \left(2^{BIT_{Eff}}\right)\left(\frac{FS_{LC}}{FS_{AD}}\right)$$

Where:

BIT_{EFF} = effective noise-free bits (17.5 + 1 bit from software filtering/averaging)

FS_{LC} = full-scale output of the load cell (10mV)

FS_{AD} = full-scale input of the ADS1230 (39mV, when PGA = 128)

Therefore:

$$\text{Noise-Free Counts} = \left(2^{(17.5+1)}\right)\left(\frac{10mV}{39mV}\right) = 95,058$$

With +5V supply voltage, 95,058 noise-free counts can be expected from the ADS1230.

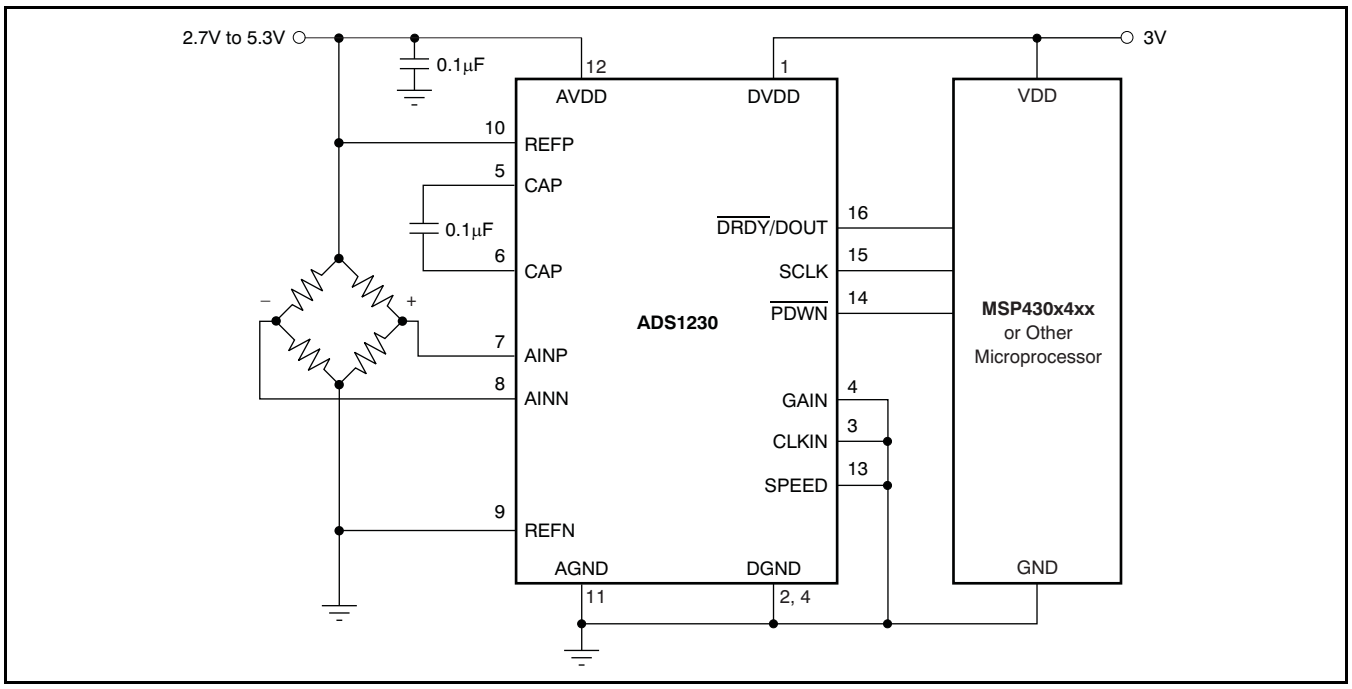


Figure 33. Weigh Scale Application

SUMMARY OF SERIAL INTERFACE WAVEFORMS

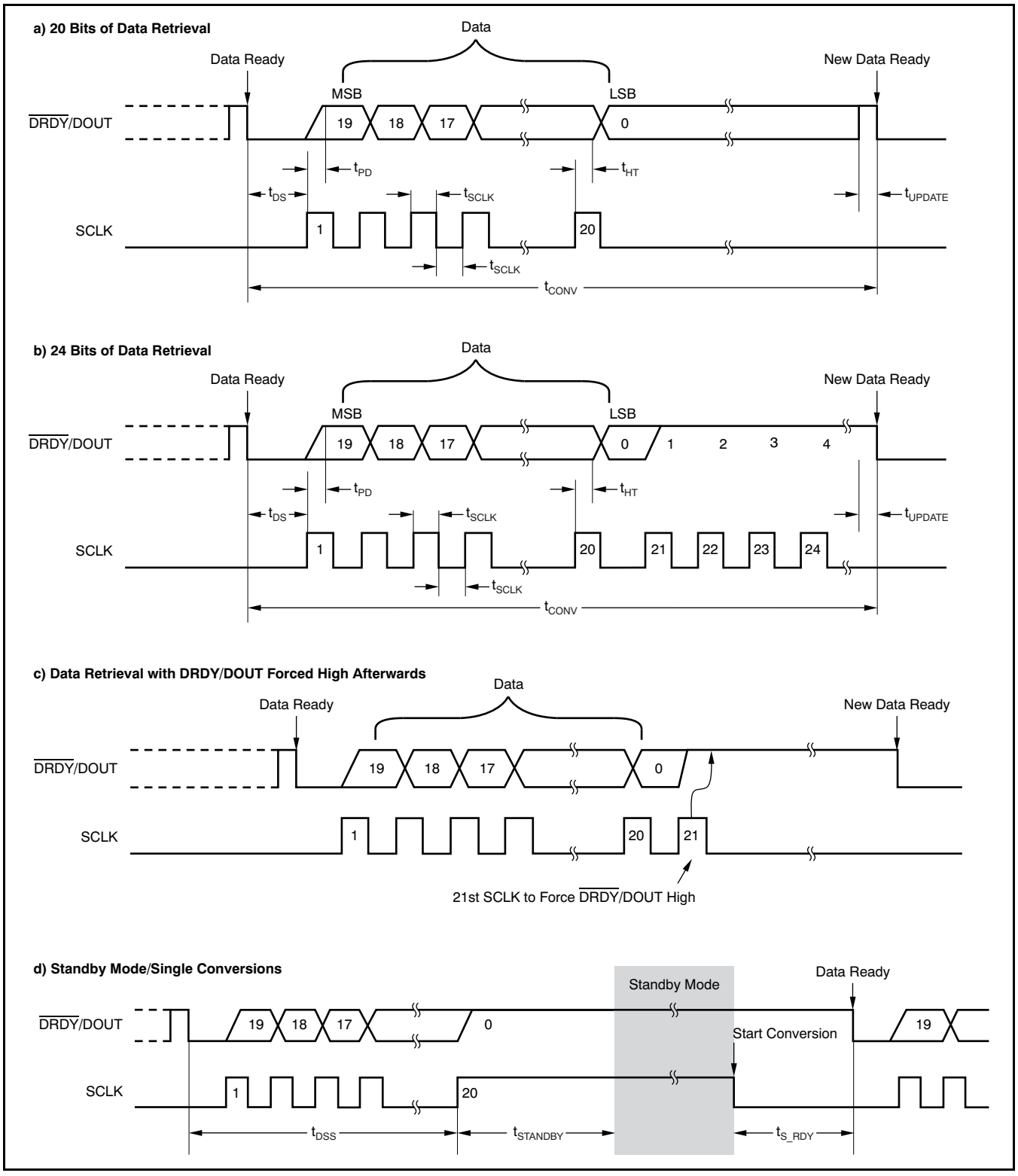


Figure 34. Summary of Data Retrieval Waveforms

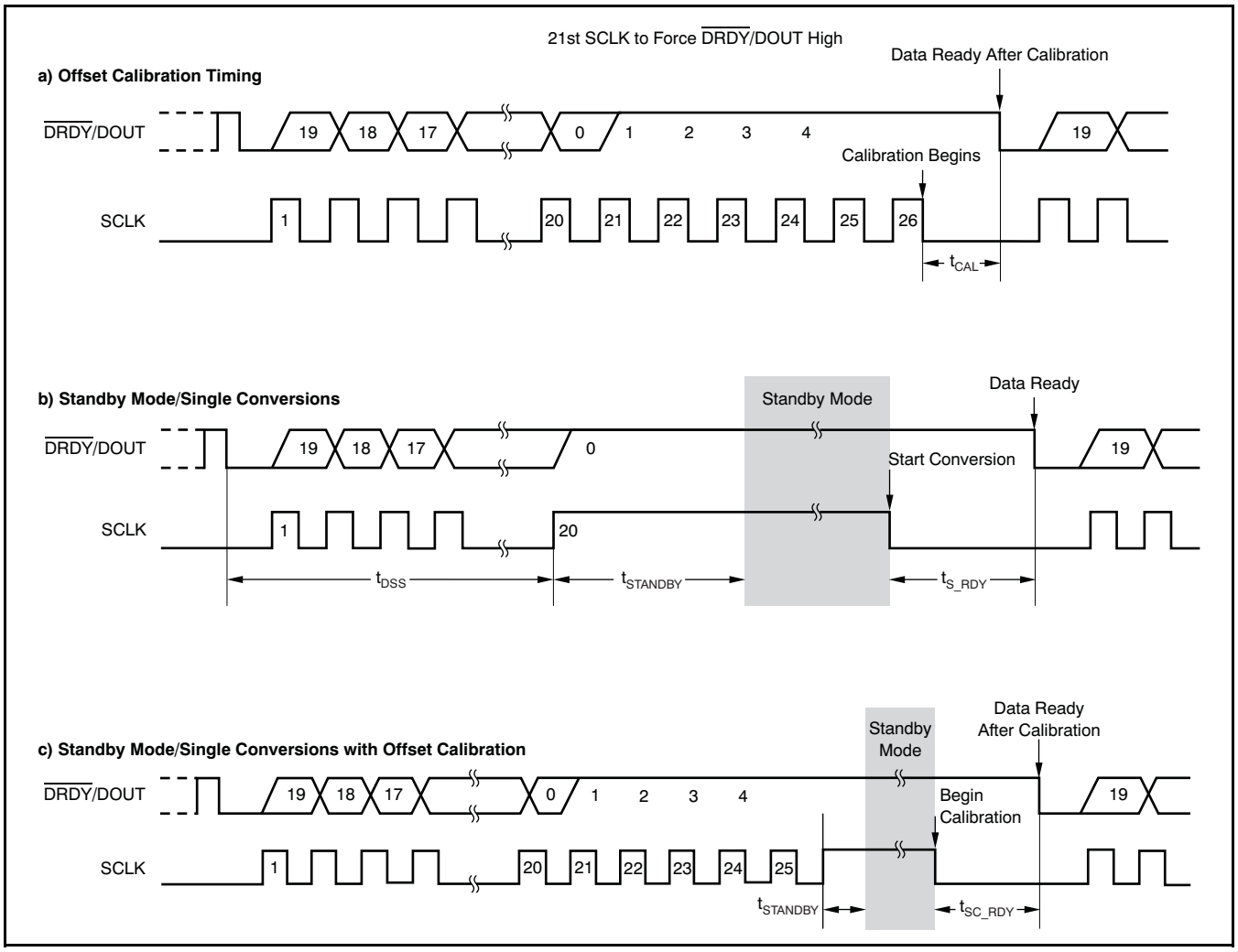


Figure 35. Summary of Standby Mode and Calibration Waveforms

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2007) to Revision B **Page**

- Deleted "Not recommended for new design" watermark from entire document 1

Changes from Original (October 2006) to Revision A **Page**

- Deleted min and max values for Data Rate Internal Oscillator 3
- Changed Normal Mode Rejection format and added min values 3
- Changed *Voltage Reference Input* section 11
- Changed Figure 19 11
- Deleted second sentence of *Serial Clock Input (SCLK)* section 14
- Added *Power-Up Sequence* section with new text and two new figures (Figure 30 and Figure 31) 19
- Changed Figure 33 20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS1230IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS1230IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS1230IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS1230IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

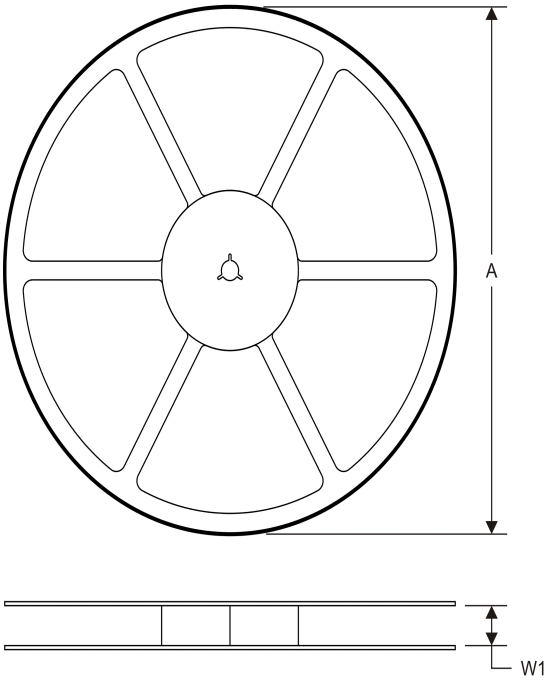
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

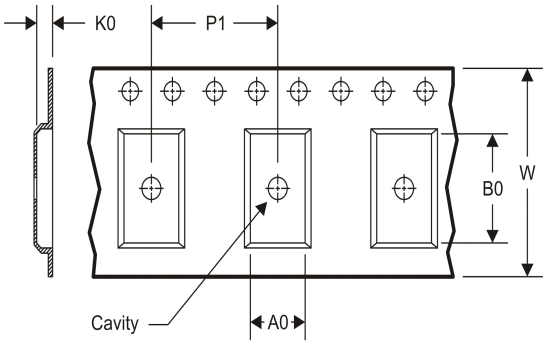
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



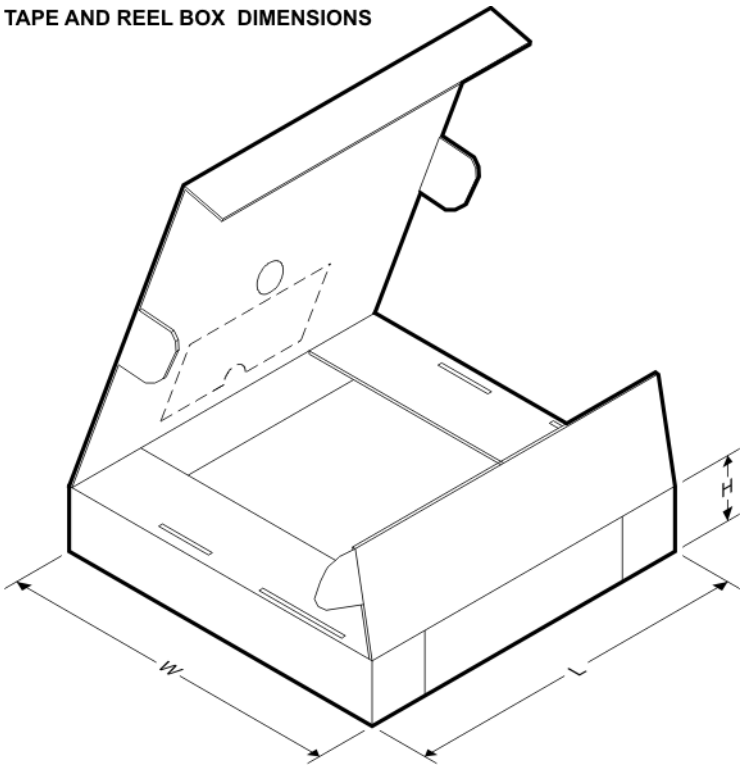
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1230IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

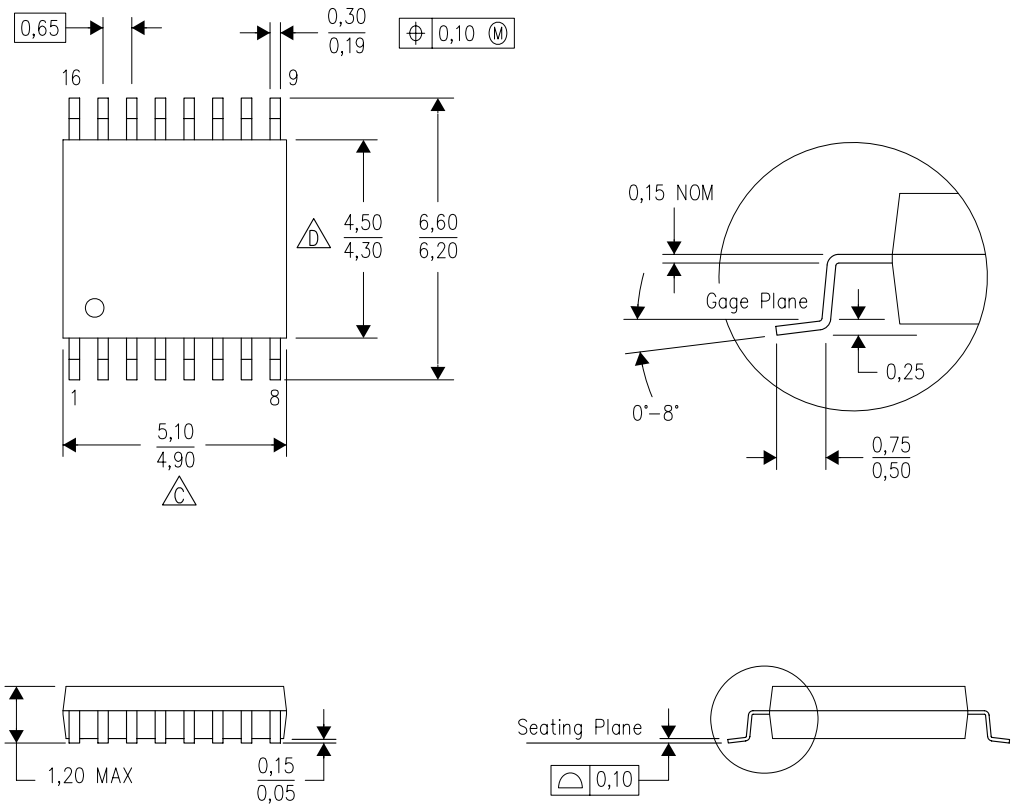
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1230IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

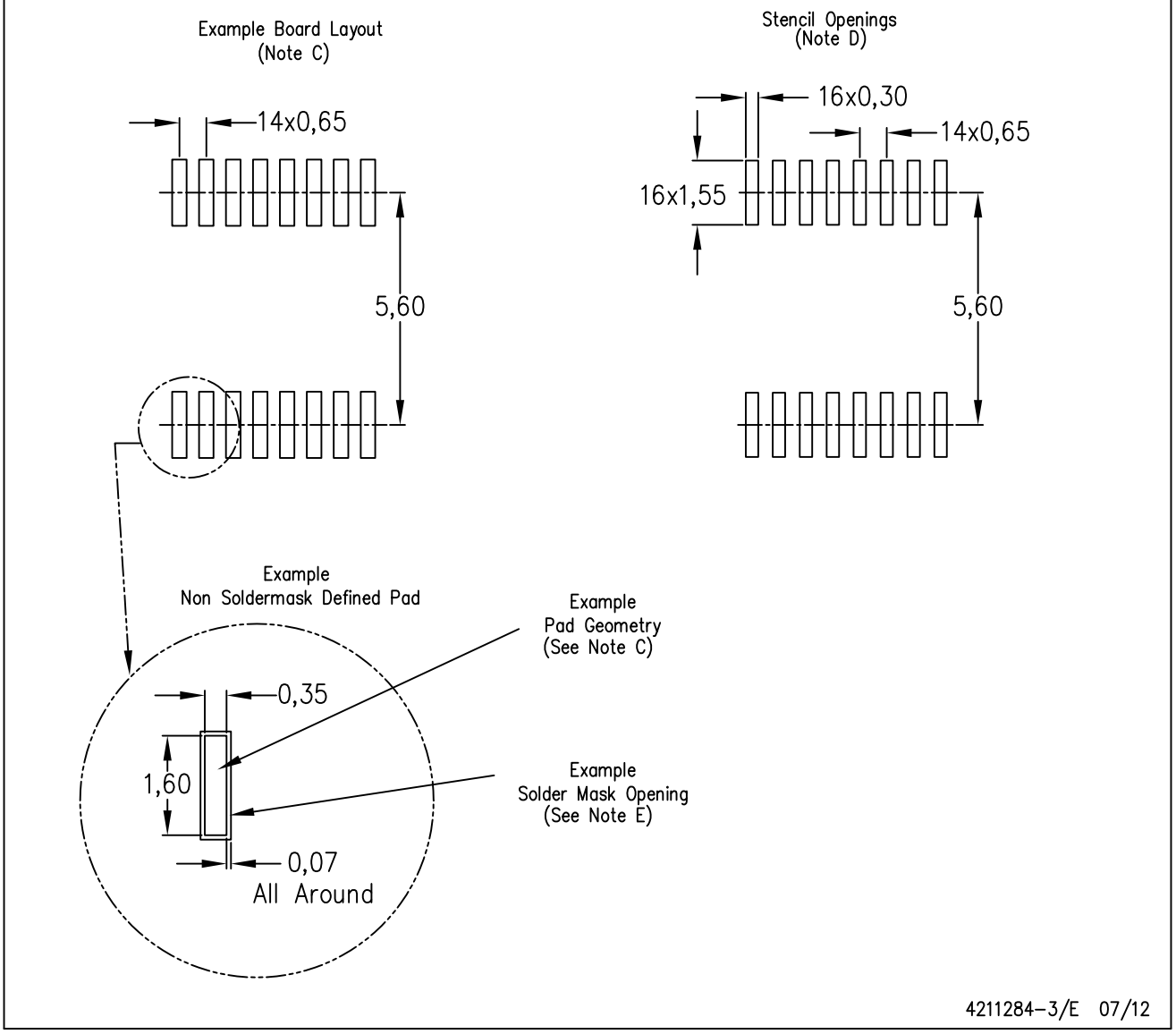
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.