PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

MITSUBISHI ALSTTLs

M74ALS163BP

T-45-23-05

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

DESCRIPTION

The M74ALS163BP is a semiconductor integrated circuit of a synchronous presettable 4-bit binary (hexadecimal) counter with a synchronous reset input.

FEATURES

- Synchronous reset and load inputs
- Enable inputs and carry output for cascade connection
- Wide operating temperature range (T_a=−20~+75℃)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

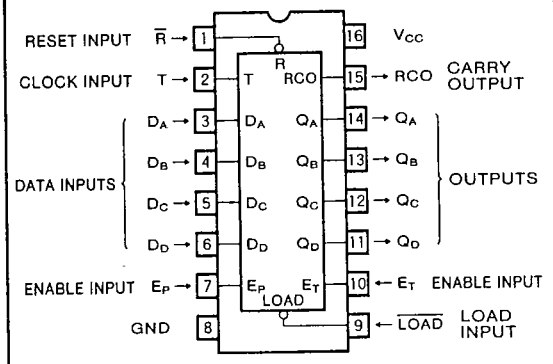
When the count pulse is applied to clock input T, the number of count pulse appears in 4-bit binary code on $Q_A \sim Q_D$ synchronized with the count pulse. Counting occurs as T changes from low-level to high-level.

Preset is synchronized with the count pulse. Irrespective of the enable inputs E_P and $\overline{E_T}$, $D_A \sim D_D$ signals appear on $Q_A \sim Q_D$ when load input $\overline{LOAD}$ is set low and T changes from low to high.

When reset R is set low and T changes from low to high, reset occurs synchronously and $Q_A \sim Q_D$ become low.

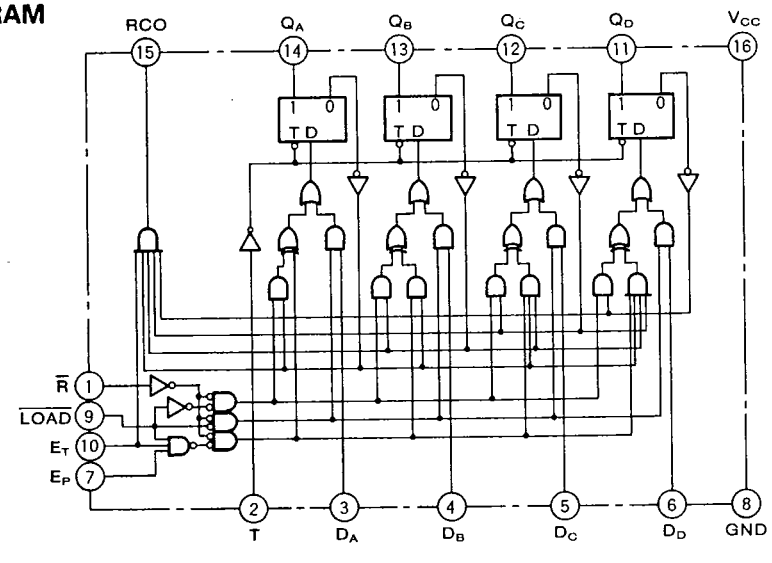
Carry output RCO becomes high only when $Q_A \sim Q_D$ and E_T are high, E_P, E_T and RCO are used when counters are connected in synchronous cascade connection and made an n-bit counter.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM



MITSUBISHI ELECTRIC

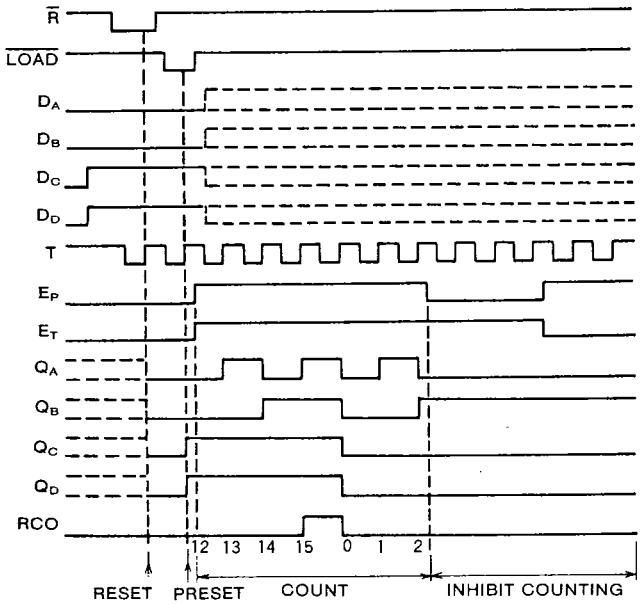
FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

Inputs					Outputs				
$\overline{R}$	$\overline{LOAD}$	E_T	E_P	T	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit counting				L
H	H	H	L	X	Inhibit counting				L*

Note 1. ↑ : Transition from low to high (positive edge trigger)
* : RCO, usually low, becomes high when Q_A, Q_D and E_T are high, i.e., $RCO = Q_A \cdot Q_D \cdot E_T$.
X : Irrelevant

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−0.4	mA
I_{OL}	Low-level output current	0		8	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

ELECTRICAL CHARACTERISTICS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5~5.5V, I_{OH}=−0.4mA		V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V	I_{OL}=4mA		0.25	0.4	V
			I_{OL}=8mA		0.35	0.5	
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.2	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−30		−112	mA
I_{CC}	Supply current	V_{CC}=5.5V			12	21	mA

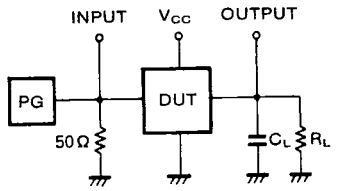
*: All typical values are at V_{CC}=5V, T_a=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Inputs	Outputs	Test conditions/Limits (Note 2)						Unit
				V_{CC}=5V, C_L=15pF, R_L=500Ω	V_{CC}=4.5~5.5V, C_L=50pF, R_L=500Ω					
				T_a=25℃	T_a=0~70℃			T_a=−20~+75℃		
				Typ	Min	Typ*	Max	Min	Typ*	Max	
f_{max}	Maximum clock frequency	T	Q_A~Q_D		40			37			MHz
t_{PLH}	Propagation time	T	RCO		5		20	5		21	ns
t_{PHL}					5		20	5		21	
t_{PLH}		T	Q_A~Q_D		4		15	4		16	ns
t_{PHL}					6		20	6		21	
t_{PLH}		E_T	RCO		3		13	3		14	ns
t_{PHL}					3		13	3		14	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

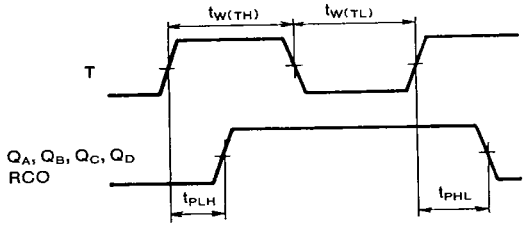
TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R_L=500Ω)

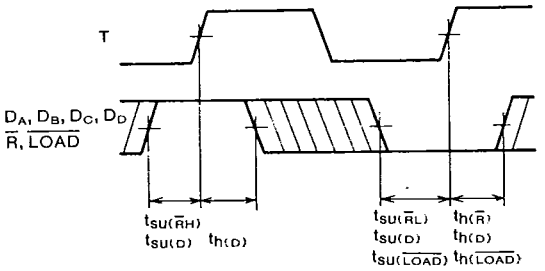
Symbol	Parameter		Limits						Unit
			T_a=0~70℃			T_a=−20~+75℃			
			Min	Typ*	Max	Min	Typ*	Max	
$t_{w(TH)}$	Pulse width	T "H"	12.5			13.5			ns
$t_{w(TL)}$		T "L"	12.5			13.5			
$t_{su(D)}$	Setup time before T↑	D_A~D_D	15			16			ns
$t_{su(\overline{LOAD})}$		$\overline{LOAD}$ "L"	15			16			
$t_{su(\overline{RL})}$		$\overline{R}$ "L"	15			16			
$t_{su(\overline{RH})}$		$\overline{R_D}$ "H" (inactive)	10			11			
$t_{su(E)}$		E_P, E_T	15			16			
$t_{h(D)}$	Hold time after T↑	D_A~D_D	0			1			ns
$t_{h(\overline{LOAD})}$		$\overline{LOAD}$ "L"	0			1			
$t_{h(\overline{R})}$		$\overline{R}$ "L"	0			1			
$t_{h(E)}$		E_P, E_T	0			1			

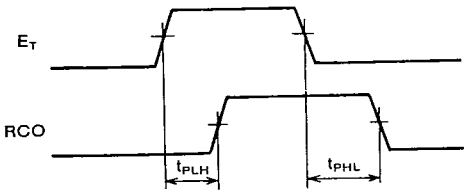
*: All typical values are at V_{CC}=5V, T_a=25℃.

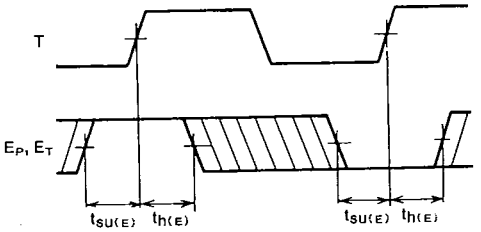
↑: Transition from low to high

TIMING DIAGRAM (Reference level=1.3V)





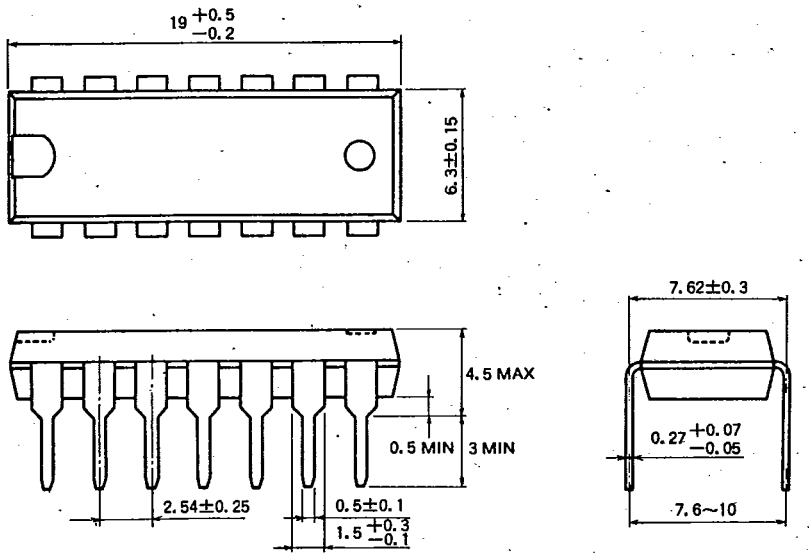




Note 3: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

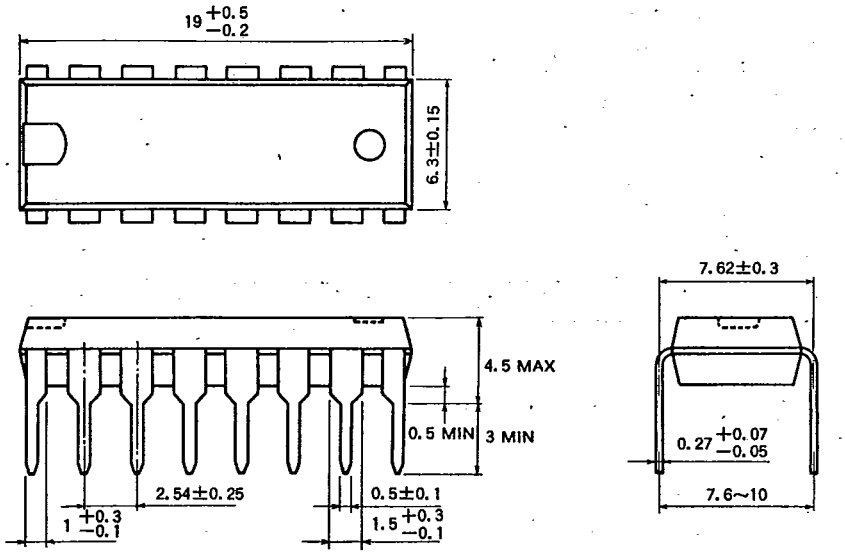
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm

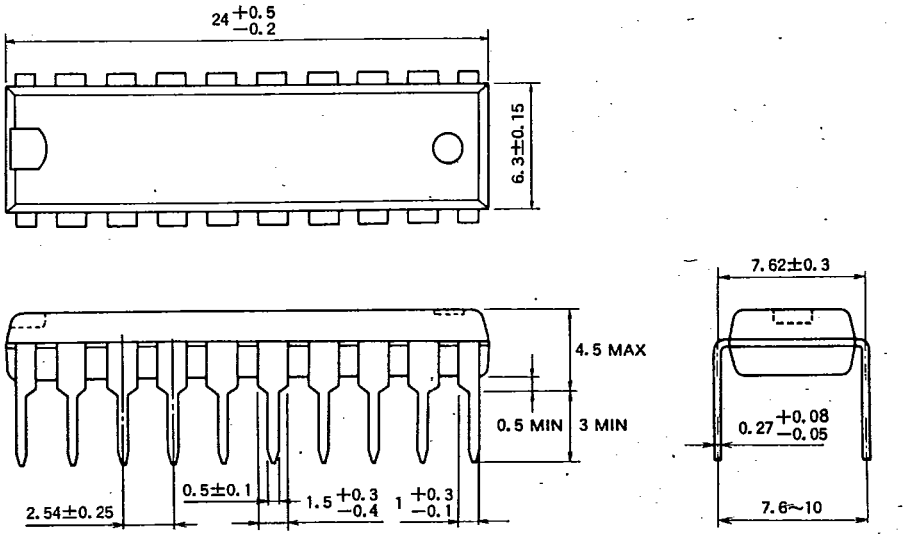


PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)
91D 12324 D T-90-20

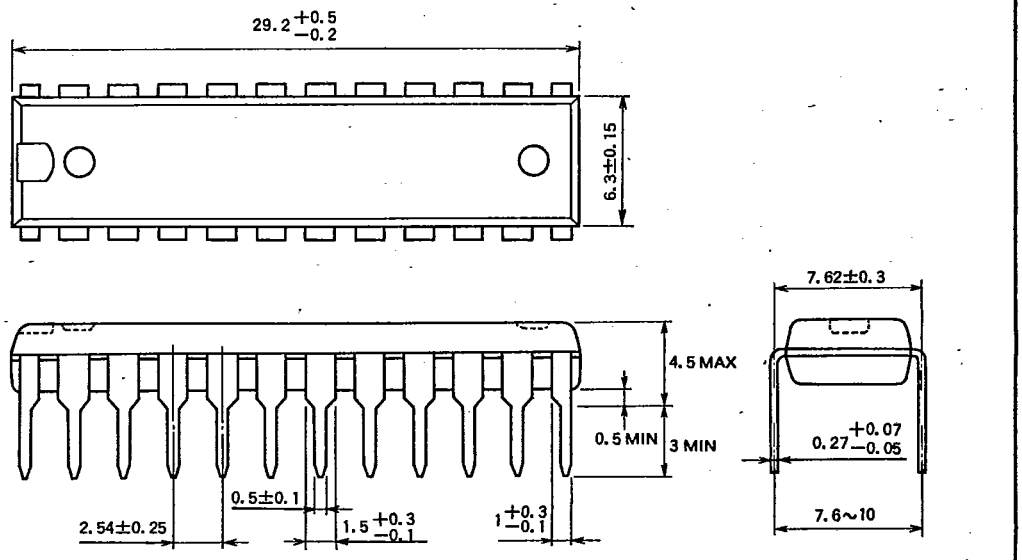
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE DESIGNATION TABLE

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	★	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	★	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	★	Hex Inverter	14P2P
M74ALS05ADP	★★	Hex Inverter with Open Colletor Output	14P2P
M74ALS08DP	★	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	★★	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	★	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	★	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	★★	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	★★	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	★★	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	★	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	★★	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	★★	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	★	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	★★	Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	★	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	★★	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	★	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	★★	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	★	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	★★	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	★★	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	★★	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	★	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	★★	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	★★	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	★	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	★	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	★	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	★★	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	★★	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	★★	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	★★	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	★★	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	★★	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	★★	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	★★	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	★★	Hex Noninverting Buffer	14P2P

★: New product ★★ : Under development

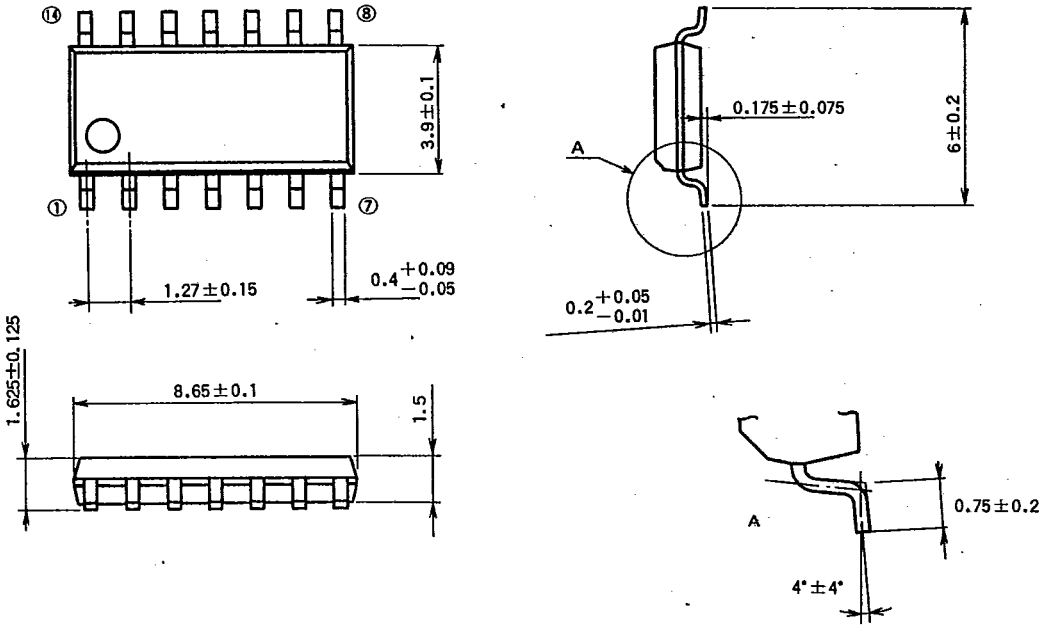
DESCRIPTION

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

MITSUBISHI (DGTL LOGIC) 91D D 6249827 0012786 0 MIT3
T-90-20

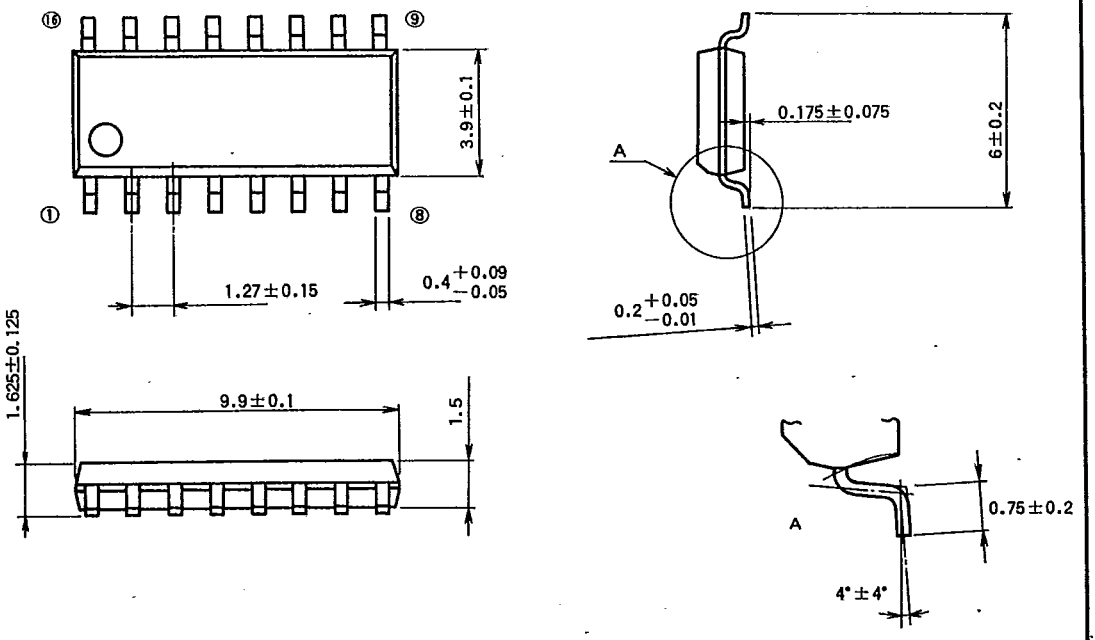
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP (JEDEC 300mil body)

Dimension in mm