MC3487 Quadruple Differential Line Driver

1 Features

- Meets or exceeds requirements of ANSI TIA/EIA-422-B and ITU recommendation V.11
- 3-state, TTL-compatible outputs
- Fast transition times
- High-impedance inputs
- Single 5V supply
- Power-up and power-down protection

2 Applications

- Factory automation
- ATM and cash counters
- Smart grid
- AC and servo motor drives

3 Description

The MC3487 offers four independent differential line drivers designed to meet the specifications of ANSI TIA/EIA-422-B and ITU Recommendation V.11. Each driver has a TTL compatible input buffered to reduce current and minimize loading.

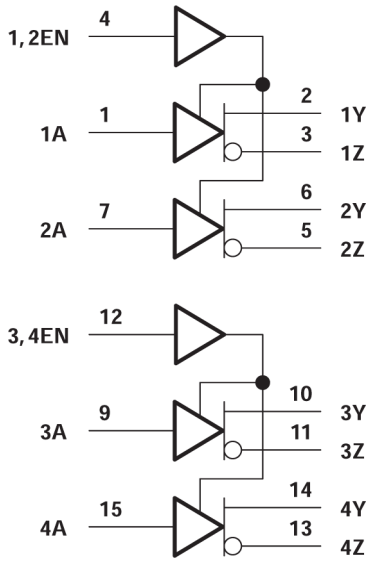
The driver outputs uses 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided a high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low.

The MC3487 is designed for best performance when used with the MC3486 quadruple line receiver. The device is available in a 16-pin dual-in-line package and operates from a single 5V supply.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
MC3486	D (SOIC, 16)	19.3mm × 9.4mm
	N (PDIP, 16)	19.3mm × 9.4mm
	NS (SOP, 16)	10.2mm × 7.8mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

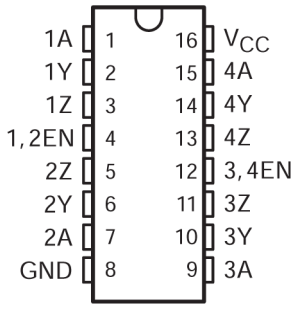


Figure 4-1. D, N, or NS Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	1	I	Single Ended Data Input for Channel 1
1Y	2	O	Non-Inverting Output for Differential Driver on Channel 1
1Z	3	O	Inverting Output of Differnetial Driver on Channel 1
1,2EN	4	I	Enable Input for Channels 1 and 2
2Z	5	O	Inverting Output of Differnetial Driver on Channel 2
2Y	6	O	Non-Inverting Output for Differential Driver on Channel 2
2A	7	I	Single Ended Data Input for Channel 2
GND	8	GND	Device Ground
3A	9	I	Single Ended Data Input for Channel 3
3Y	10	O	Non-Inverting Output for Differential Driver on Channel 3
3Z	11	O	Inverting Output of Differential Driver on Channel 3
3,4EN	12	I	Enable Input for Channels 3 and 4
4Z	13	O	Inverting Output of Differential Driver on Channel 4
4Y	14	O	Non-Inverting Output for Differential Driver on Channel 4
4A	15	I	Single Ended Data Input for Channel 4
V_{CC}	16	P	5V Power Supply Positive Terminal Connection

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, GND = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC} (see (2))	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage		7	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

5.3 Thermal Information

THERMAL METRIC(1)		D (SOIC)	N (PDIP)	NS (SOP)	UNIT
		16-PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	40.6	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA				-1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OH} = -20 mA	2.5		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.5	V
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω	See Figure 6-1		2		
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(1)	R_L = 100 Ω	See Figure 6-1			±0.4	V
V_{OC}	Common-mode output voltage(2)	R_L = 100 Ω	See Figure 6-1			3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(1)	R_L = 100 Ω	See Figure 6-1			±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	µA
			V_O = -0.25 V			-100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	V_O = 2.7 V			100	µA
			V_O = 0.5 V			-100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	µA
I_{IH}	High-level input current	V_I = 2.7 V				50	µA
I_{IL}	Low-level input current	V_I = 0.5 V				-400	µA
I_{OS}	Short-circuit output current(3)	V_I = 2 V			-40	-140	mA
I_{CC}	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled,	No load			85	

(1) $\Delta_{|VOD|}$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(2) In ANSI Standard TIA/EIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(3) Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

5.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF,	See Figure 6-2		20	ns
t_{PHL}	Propagation delay time, high- to low-level output				20	
t_{sk}	Skew time	C_L = 15 pF,	See Figure 6-2		6	ns
$t_{t(OD)}$	Differential-output transition time	C_L = 15 pF,	See Figure 6-3		20	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF,	See Figure 6-4		30	ns
t_{PZL}	Output enable time to low level				30	
t_{PHZ}	Output disable time from high level	C_L = 50 pF,	See Figure 6-4		25	ns
t_{PLZ}	Output disable time from low level				30	

6 Parameter Measurement Information

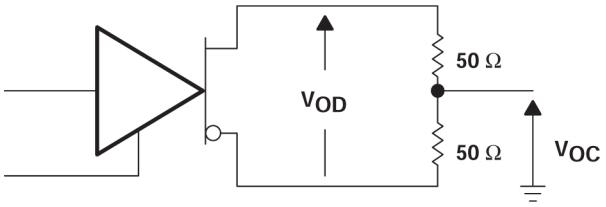
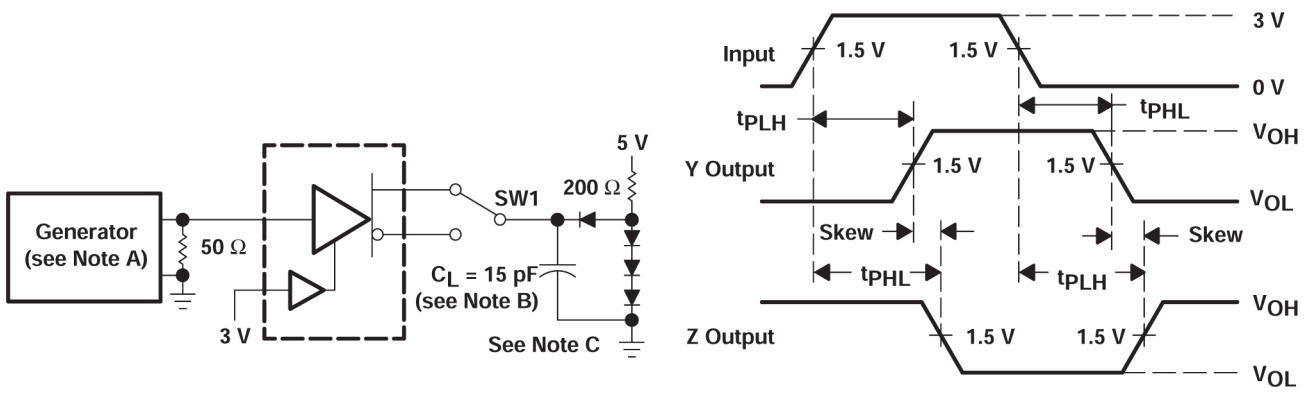


Figure 6-1. Differential and Common-Mode Output Voltages

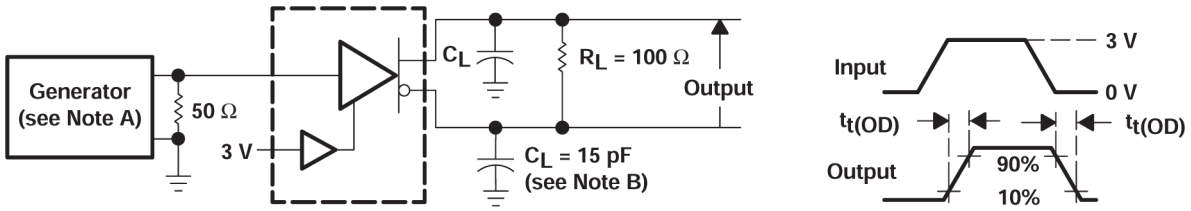


A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 5 ns, t_f ≤ 5 ns, PRR ≤ 1 MHz, duty cycle = 50% Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

C. All diodes are 1N916 or 1N3064.

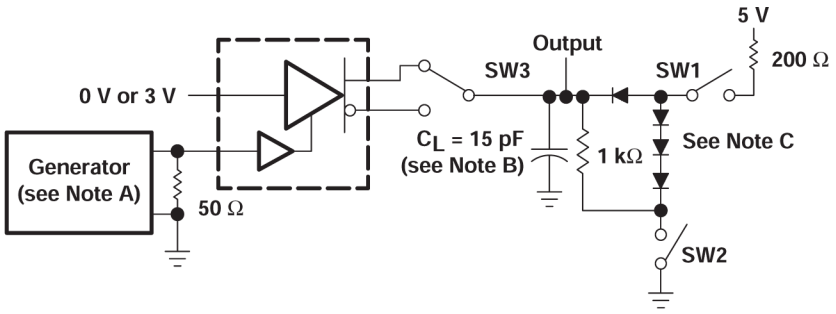
Figure 6-2. Test Circuit and Voltage Waveforms



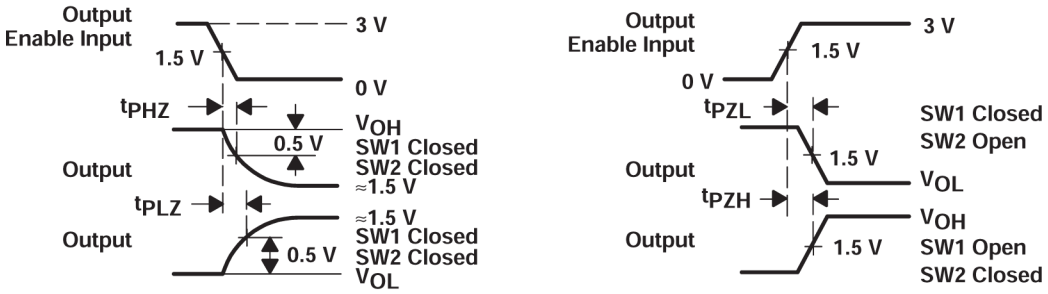
A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 5 ns, t_f ≤ 5 ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

Figure 6-3. Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 5 ns, t_f ≤ 5 ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

C. All diodes are 1N916 or 1N3064.

Figure 6-4. Driver Test Circuit and Voltage Waveforms

7 Device Functional Modes

Table 7-1. Function Table (Each Driver)

INPUT	OUTPUT ENABLE(1)	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = TTL high level, L = TTL low level, X = irrelevant, Z = High impedance

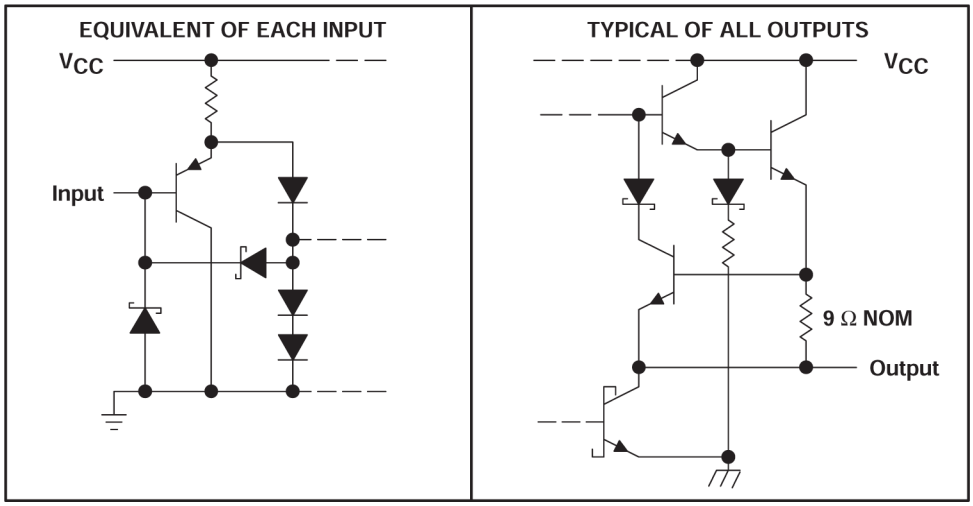


Figure 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2004) to Revision D (March 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC3487D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	MC3487	
MC3487DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples
MC3487N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC3487N	Samples
MC3487NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC3487N	Samples
MC3487NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

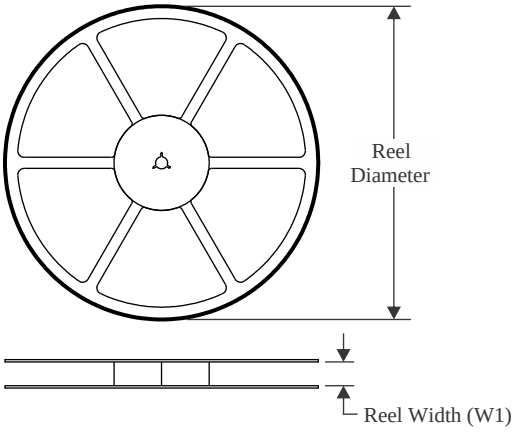
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

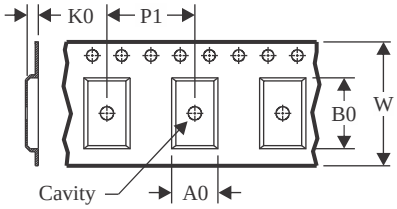
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

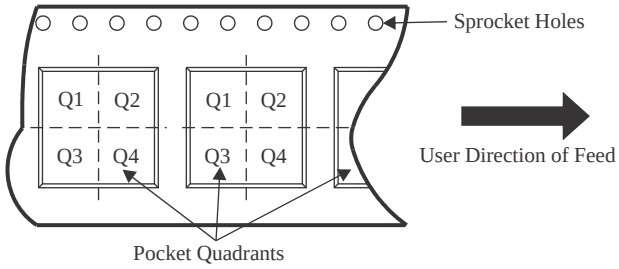


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

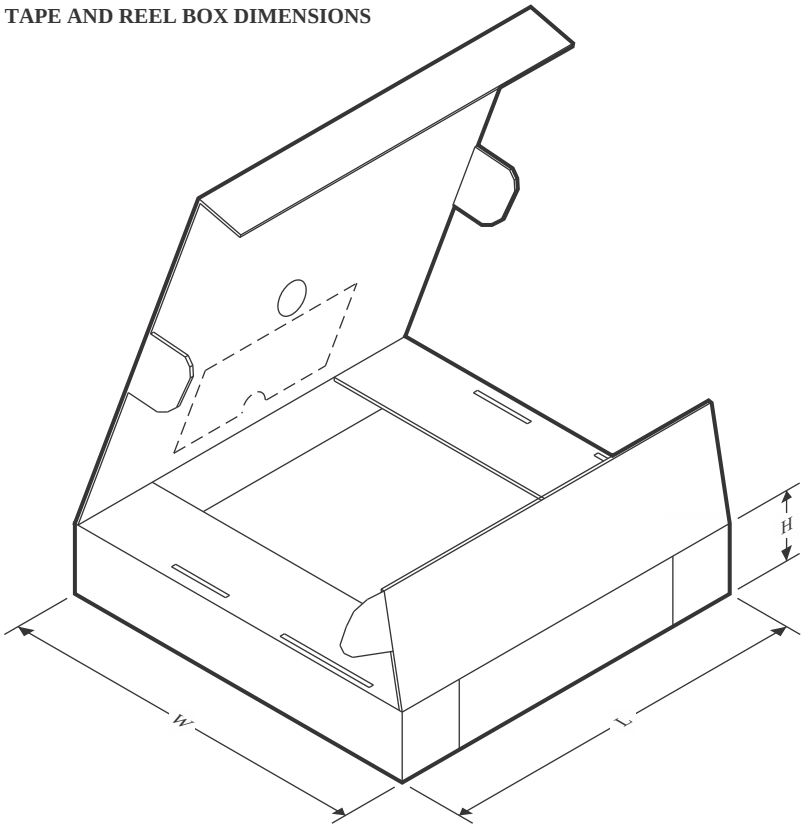
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3487NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

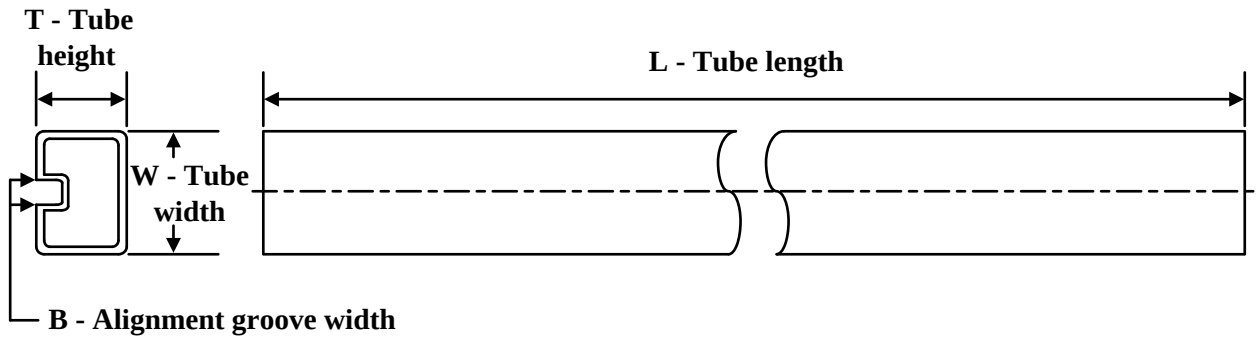
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

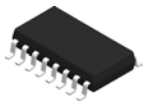
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3487DR	SOIC	D	16	2500	340.5	336.1	32.0
MC3487DR	SOIC	D	16	2500	353.0	353.0	32.0
MC3487NSR	SOP	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MC3487N	N	PDIP	16	25	506	13.97	11230	4.32
MC3487N	N	PDIP	16	25	506	13.97	11230	4.32
MC3487NE4	N	PDIP	16	25	506	13.97	11230	4.32
MC3487NE4	N	PDIP	16	25	506	13.97	11230	4.32

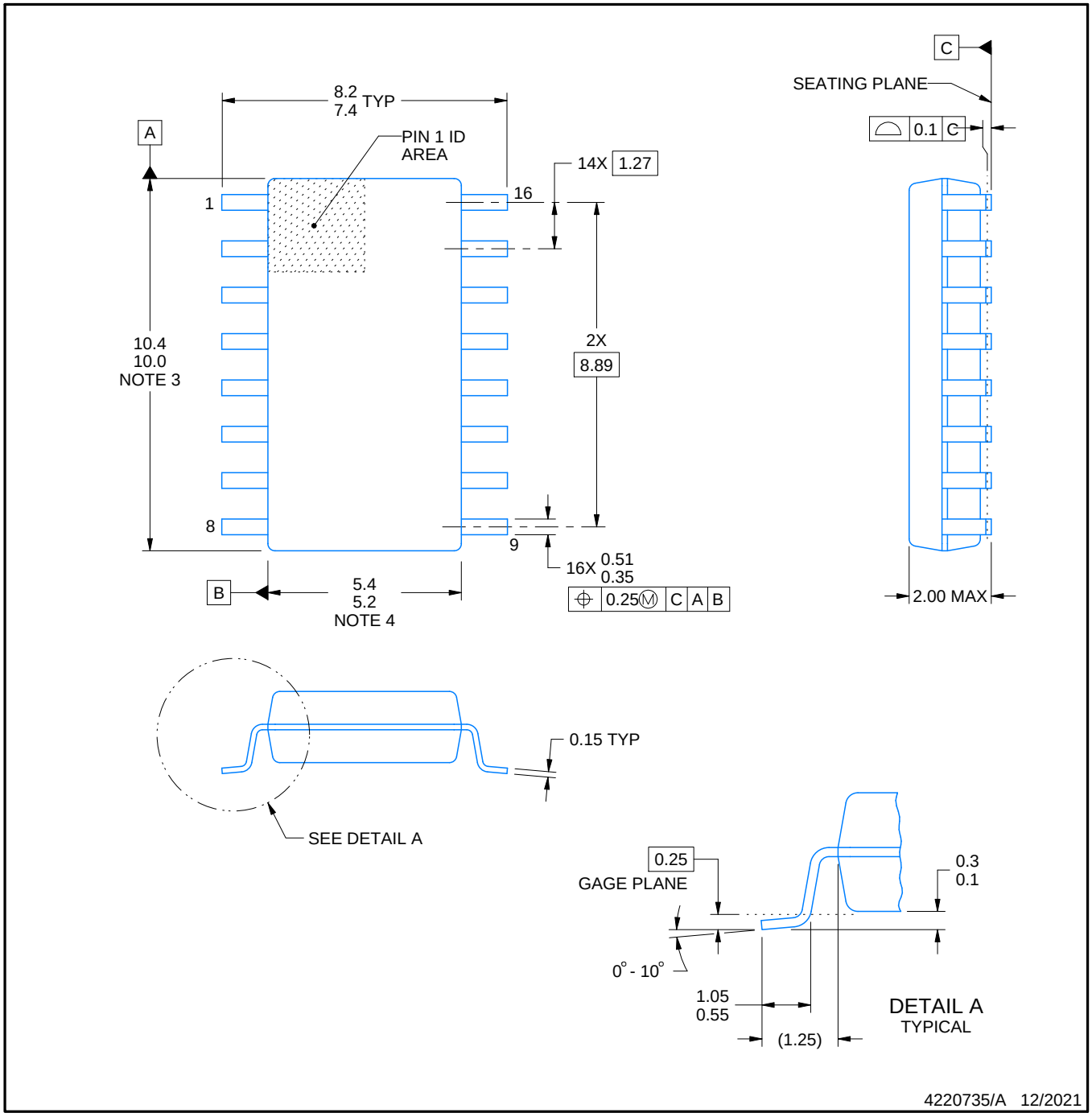


PACKAGE OUTLINE

NS0016A

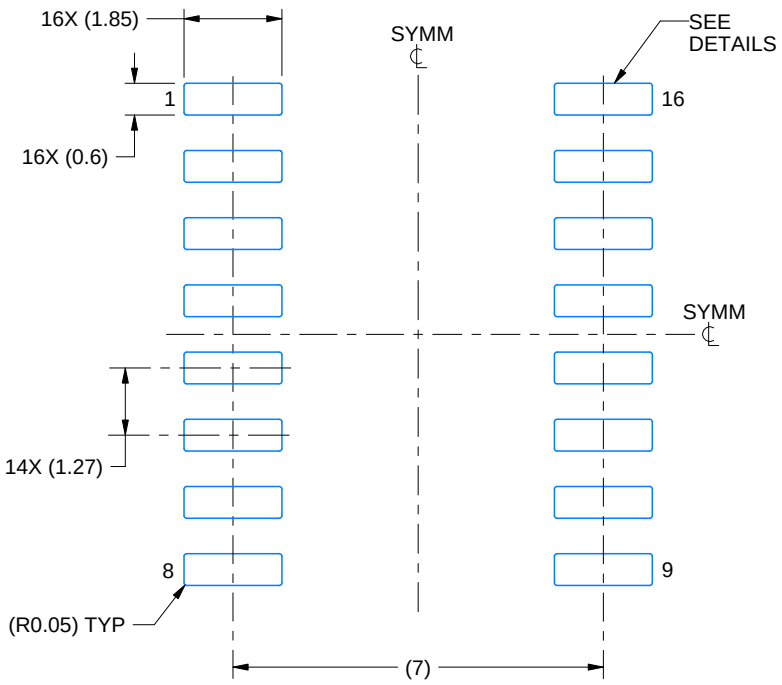
SOP - 2.00 mm max height

SOP

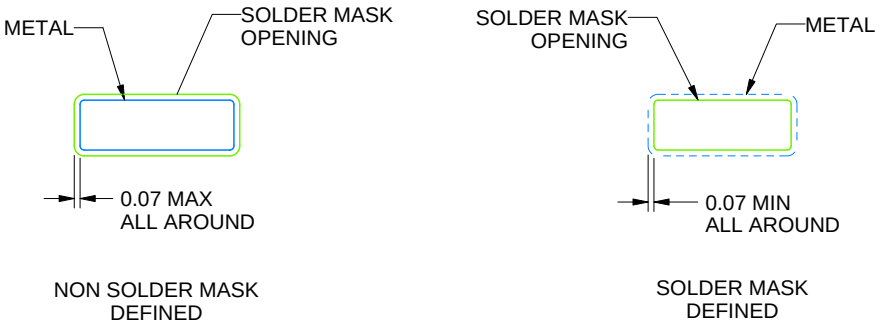


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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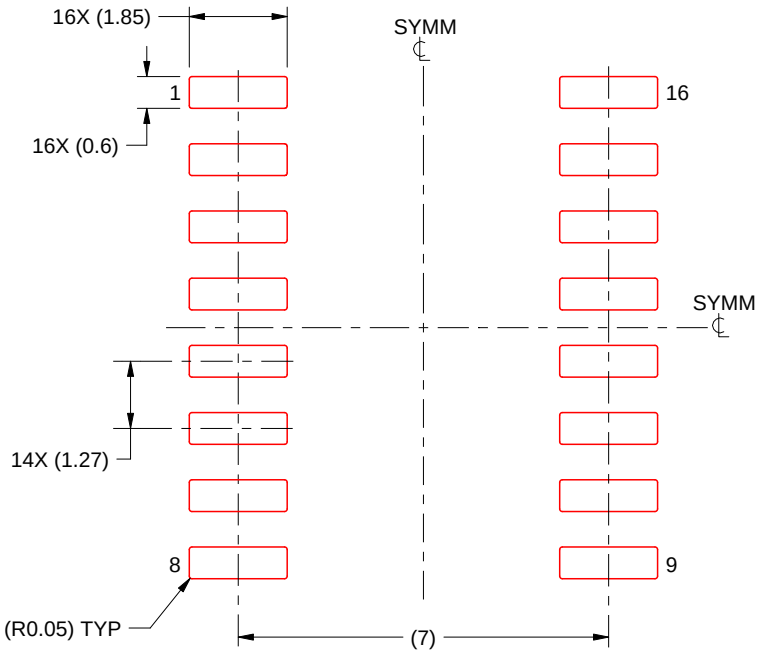
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



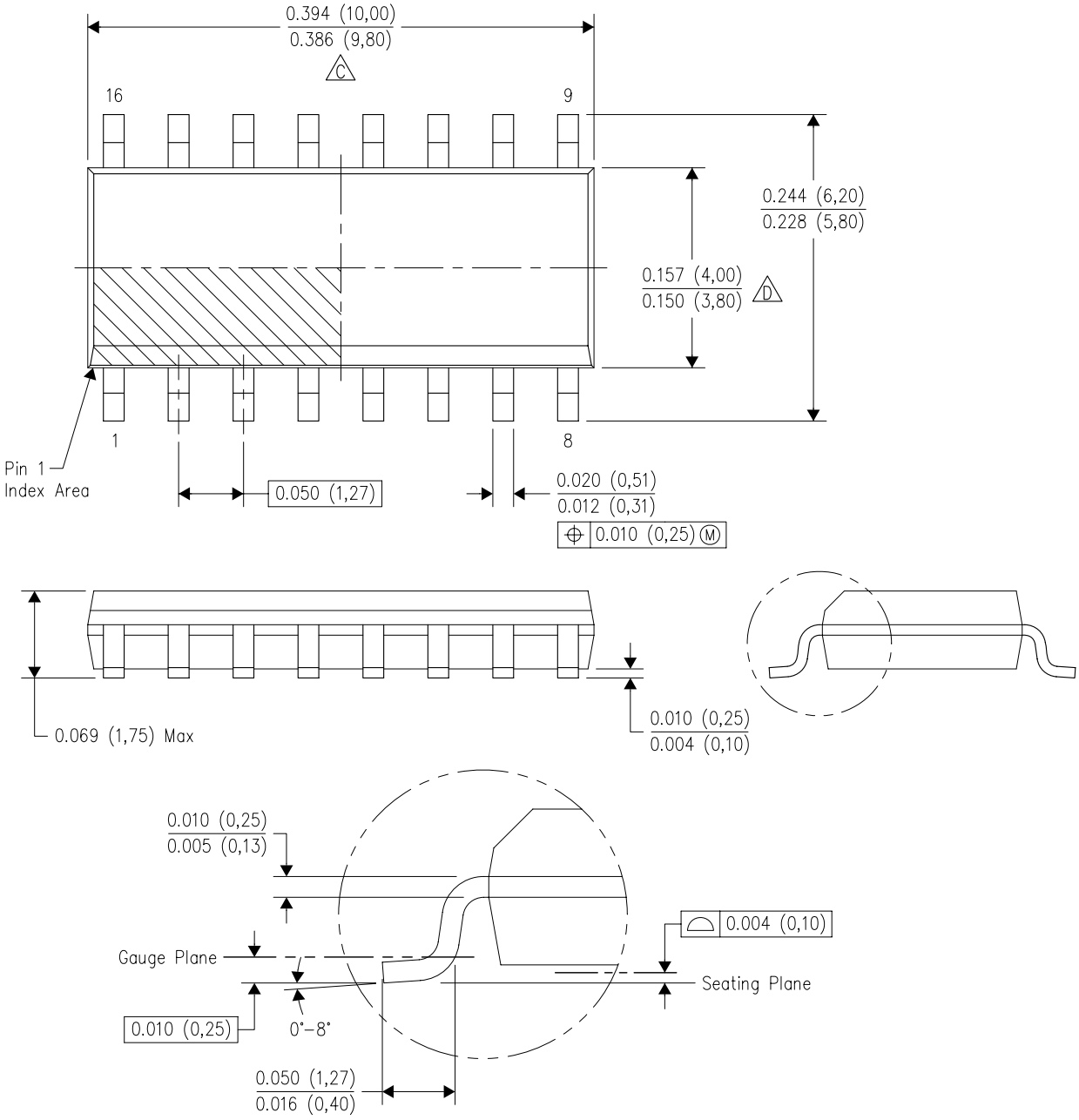
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

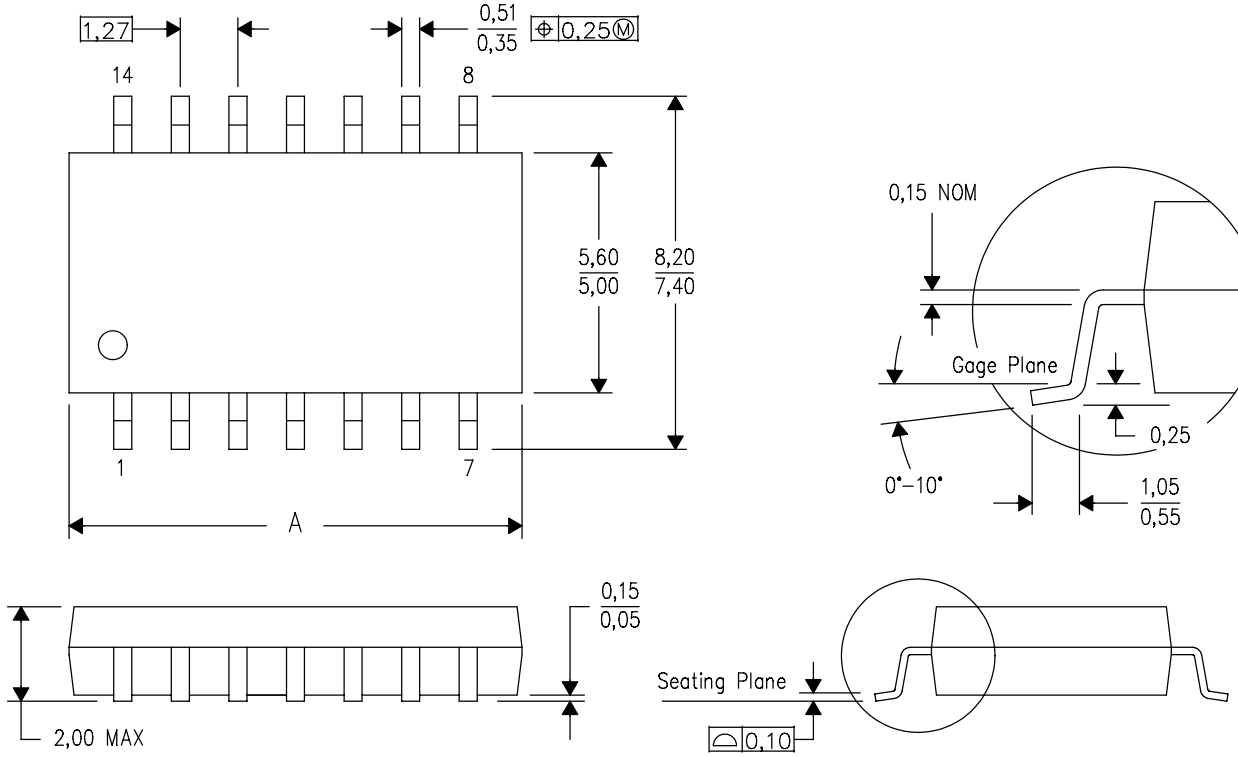


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

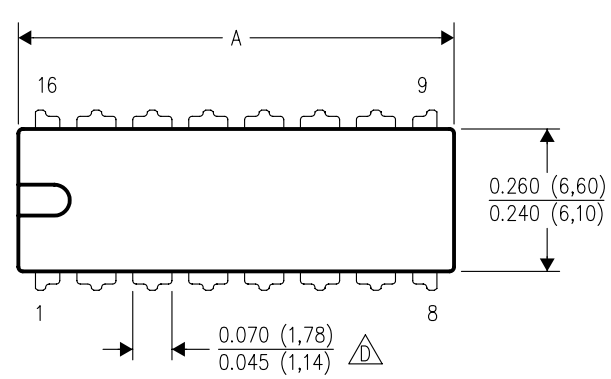
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

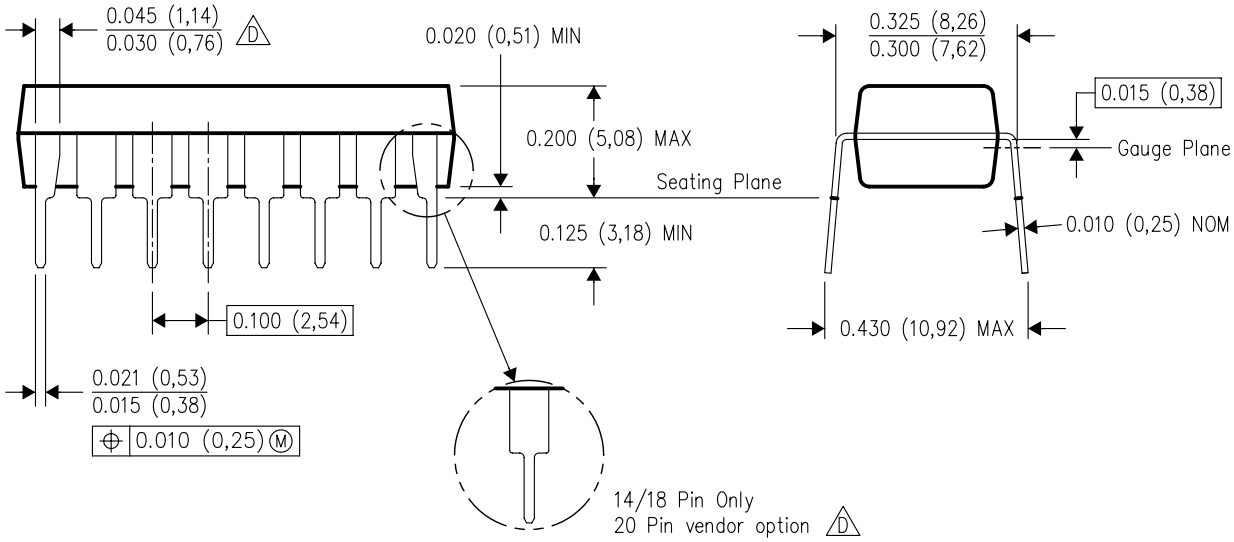
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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