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Specifications for approval

(ROHS)

NO. Q/TANCAP.CC (T) 4.09-12-18

Product Name: **CC (T) 4 Multilayer Ceramic Capacitor (Radial)**

Customer: _____

Type and Specification: **Full Range**

WRITTEN	CHECKED	APPROVED
Wang Xunguo	Wang Baiping	Wang Li

Signature of Approval: **Wang Li**

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Product Name	CC4(CT4)Radial leaded type Multilayer Ceramic Capacitors

1.Scope:

This specification applies to CC4 (CT4) Radial leaded type Multilayer Ceramic Capacitors produced by our company for use in electronic equipment of (name of customer)

2.Standard:

《Detail specification for electronic components fixed ceramic dielectric capacitors CC4 Assessment level E》 SJ/T10569-94

《Detail specification for electronic components fixed ceramic dielectric capacitors CT4 Assessment level E》 SJ/T10569-94

3.Classify:

CC4: Material of dielectric is: NPO（N）。

CT4: Material of dielectric is:X7R（B）、Z5U、Y5V（Y）。

4.Test Conditions:

4.1: Standard Condition: If there are no specific prescribe，The test will be done according to standard condition(Temperature 15-35℃;Relative Humidity 45-75%), But If there are any problems subject to standard condition or there are some specific requirements. Please test according to 4.2

4.2: Fundamental Condition: Temperature is 20℃;Relative Humidity is 60-70%; Atmospheric pressure is 800-1060mbar。

5.Testing Method:

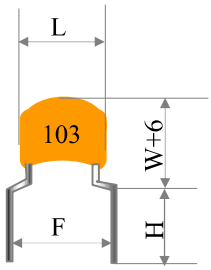
When the products will be tested, In order to avoid the error of result, The capacitors must be placed in the temperature that the capacitors be tested for 30 minutes and discharged fully.

Product Name	CC4(CT4)Radial leaded type Multilayer Ceramic Capacitors

5.Testing Items:

Item	Performance Characteristics			Testing Method
Dimensions	See page 3			Measured by Dimensions gauge
Appearance	Correct Marking、clear, No pinhole、No burr、No damage			Visual examination
Insulation Resistance	CC4	C_R≤10nF R≥10000MΩ C_R > 10nF C_R ×R≥100s		Rated Voltage applied for 1 Minute Charging current≤50mA
	CT4	C_R≤25nF R≥4000MΩ C_R > 25nF C_R ×R≥100s		
Capacitance Tolerance	CC4	B=±0.1pF C=±0.25pF D=±0.5pF G=±2% J=±5% K=±10% M=±20%		1MHz 1VDC
	CT4	B	K=±10%， M=±20% S= $^{+50}_{-20}$%	1KHz 1VDC
		Y	M=±20%， S= $^{+50}_{-20}$%， Z= $^{+80}_{-20}$%	1KHz 0.3VDC
Dissipation factor (Tanδ)	CC4	≤0.15%		1MHz 1VDC
	CT4	B	≤2.5%	1KHz 1VDC
		Y	≤5%	1KHz 0.3VDC
Withstanding Voltage	No dielectric breakdown or mechanical Breakdown			250% of the rated voltage for 1-5sec is applied with less than 50mA current
Solderability	The dipped portion of termination is at least 95% covered by a new solder coating.			Solder temperature: 235±5℃ Immersion times:2±0.5S
Temperature Characteristics	CC4	Change of capacitance: 30ppm/℃ 60ppm/ ℃		
	CT4	B	Change of capacitance:+30% ~ -80%	
		Y	Change of capacitance: +22- ~ -56%	
Life Test	CC4	200%rated voltage at125℃; 1000hr		
	CT4	B	200%rated voltage at125℃; 1000hr	
		Y	150%rated voltage at 85℃; 1000hr	

Product Name	CC4 (CT4) Radial leaded type Multilayer Ceramic Capacitors



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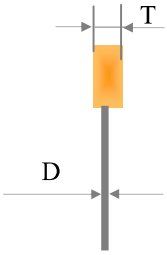
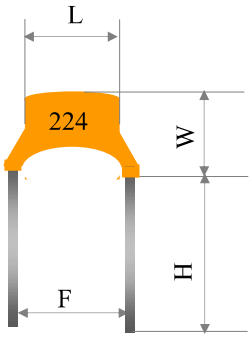
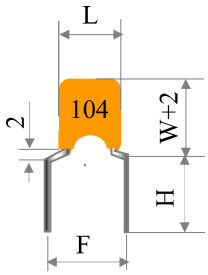
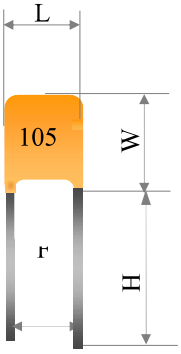




B1 type



B2 type

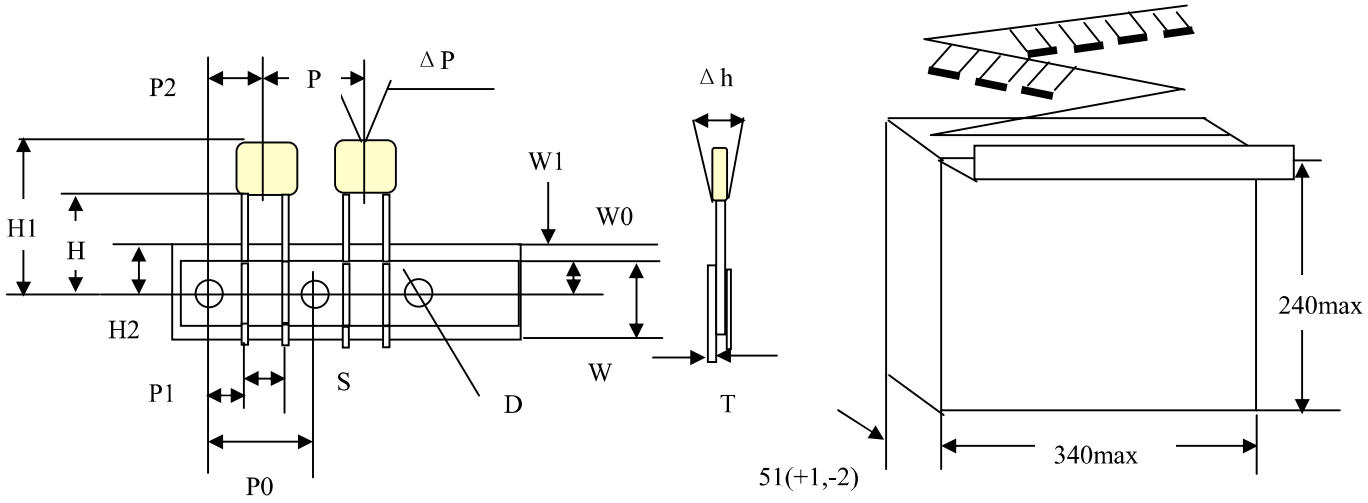


C type

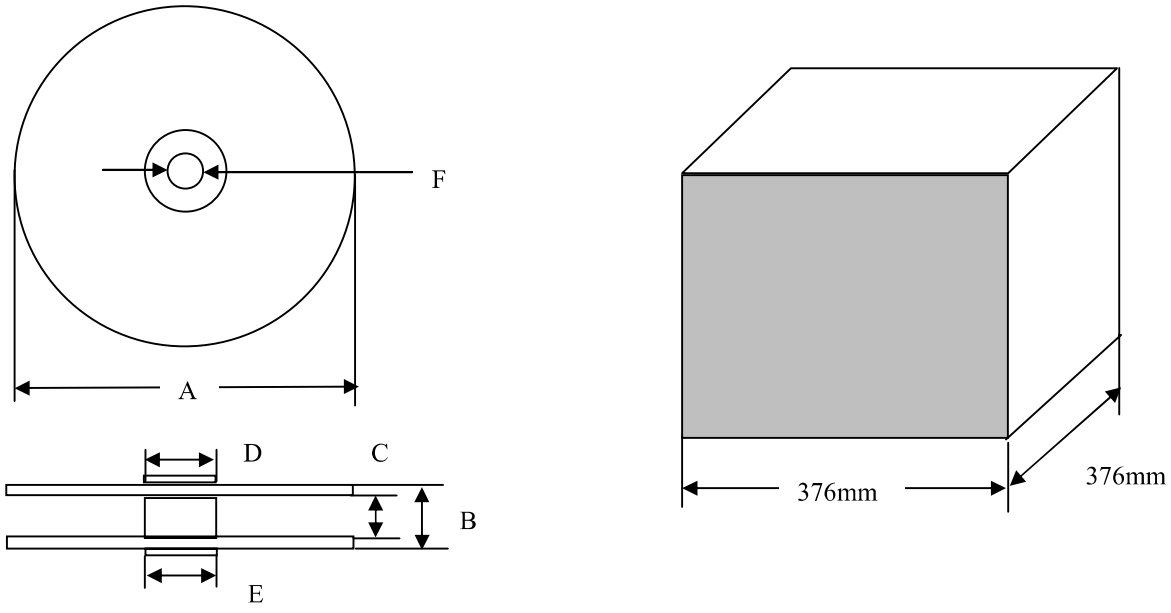
Dimensions	Appearance	Unit：（mm）						Working Voltage （V）	Capacitance （pF）		
		F	Hmin	Lmax	Wmax	Tmax	D		COG （NPO）	X7R	Y5V （Z5U）
0805	A B_1 C_1	5.0 5.0 2.5	5.0	4.2	3.8	3.8	0.5	25 50 100	0R5~332 0R5~222 0R5~102	221~105 221~105 221~683	103~105 103~684
1206	B_2 C_2	5.0 4.0	5.0	5.0	4.5	3.8	0.5	25 50 100	0R5~682 0R5~472 0R5~392	102~105 102~105 102~683	103~125 103~105
1210	C_3 C_2	5.0 4.0	5.0	7.6	5.5	3.8	0.5	25 50 100	561~103 561~682 561~472	102~334 102~105 102~104	104~155 104~155
1812	C_3	5.0	5.0	8.5	8.5	3.8	0.5	25 50 100	102~153 102~103 102~682	103~474 103~334 103~224	154~335 154~325
2225	C_4	7.5	5.0	10.5	9.5	4.2	0.5	25 50 100	102~223 102~223 102~103	103~105 103~105 103~474	684~475 684~335
3035	C_4	7.5	5.0	12.5	10.5	4.2	0.5	25 50 100	102~104 102~473 102~333	103~225 103~225 103~105	105~106 105~685

Packaging Style

Ammo Package



Code	P	P0	W	W0	H2	W2	H1	D	T	ΔH	H	S	P1	P2	ΔP
Dim	12.7	12.7	18	5	9	0	32.5	4	0.5	0	16-18	5	3.85	6.35	1.3
Tol	±1	±0.3	+1 -0.51	min	±0.5	±1	max	±0.2	±2.0	±0.2	±0.5	±0.5	±0.7	±0.4	max



Reel Package

A	B	C	D	E	F
355-365	5.08max	38.10-46.02	102.01max	86.36max	25.40-30.48

Packaging Quantity

Reel Package	Ammo Package	Bulk Package
2500	4000	1000

Application Notes for Multilayer Capacitors

1. Effect of Temperature

Both capacitance and dissipation are affected by variations in temperature. The maximum capacitance change with temperature is defined by the temperature characteristic. However, this only defines a “box” bounded by the upper and lower operating temperatures and the minimum and maximum capacitance values. Within this “box”, the variation with temperature depended upon the specific dielectric formulation.

Insulation resistance decreases with temperature. Typical the insulation resistance at maximum rated temperature is 10% of the 25℃ value.

2. Effect of Voltage

Class Ⅰ ceramic capacitors are not affected by variations in applied AC or DC voltages. For Class Ⅱ and Ⅲ ceramic capacitors, variations in voltage affect only the capacitance and dissipation factor. The application of DC voltage higher than 5 DC reduces both the capacitance and dissipation factor. The application of AC voltage up to 10-20 Vac tend to increase both capacitance and dissipation factor. At higher AC voltage, both capacitance and dissipation factor begin to decrease.

3. Effect of Frequency

Frequency affects both capacitance and dissipation factor.

The variation of impedance with frequency is an important consideration in the application of multilayer ceramic capacitors. Total impedance of the capacitor is the vector of the capacitive reactance, the inductive reactance, and the ESR. As frequency increases, the capacitive reactance decreases. However, the series inductance (L) produces inductive reactance, which increases with frequency. At some frequency, the impedance ceases to be capacitive and becomes inductive. This point is the self-resonant frequency. At the self-resonant frequency, the reactance is zero, and the impedance consists of the ESR only.

Lead configuration and lead length have a significant impact on the series inductance. The lead inductance is approximately 10nH/inch, which is large compared to the inductance of chip. The effect of this additional inductance is a decrease in the self-resonant frequency, and an increase in impedance in the inductive region above the self- resonant frequency.

4. Effect of Time

The capacitance of Class Ⅱ and Ⅲ dielectrics change with time as well as with temperature, voltage and frequency. This change with time is known as “aging”. It is caused by gradual realignment of the crystalline structure of the ceramic dielectric material as it is cooled below its Curie temperature, which produces a loss of capacitance with time. The aging process is predictable and follows a logarithmic decay. Typical aging rates for C0G, X7R, and Z5U dielectrics are as follows:

C0G:	None
X7R:	1.0% per decade of time
Z5U:	5.0% per decade of time
Y5V:	6.0% per decade of time

The aging process is reversible. If the capacitor is heated to a temperature above its Curie point for some period of time, de-aging will occur and the capacitor will regain the capacitance lost during the aging process. The amount of de-aging depends on both the elevated temperature and the length of time at that temperature. Exposure to 150℃ for one-half hour or 125℃ for two hour is usually sufficient to return the capacitor to its initial value.

Because the capacitance changes rapidly immediately after de-aging, capacitance measurements are usually delayed for at least 10 hours after the de-aging process, which is often referred to as “last heat”. In addition, manufacturers utilize the aging rates to set factory test limits which will bring the capacitance within the specified tolerance at some future time, to allow for customer receipt and use. Typically, the test limits are adjusted so that capacitance will be within the specified tolerance after either 1,000 hours or 100 days, depending on the manufacturer and the product type.

5. Thermal Shock.

Multilayer ceramic capacitors are sensitive to thermal shock due to device construction consisting of interleaved layers of ceramic dielectric and metal electrodes with metal terminations for electrical contact.

Thermal shock is mechanical damage caused by a structure’s inability to absorb mechanical stress caused by excessive changes of temperature in a shot period of time. This stress is caused by differences in CTE(coefficient of thermal expansion), δT(thermal conductivity) and the rate of change of temperature. CTE andδT are a function of the materials used in the component’s manufacture and the rate of change of temperature is dependent on the soldering process.

When the temperature rate of change is too great, thermal shock cracks occur. These cracks are initiated where the structure is weakest and mechanical stress is concentrated. This is at or near the ceramic / termination interface in the middle of the exposed termination. Mechanical stress is greatest at the corners where the chip is strongest but cracks tend to start where the structure is weakest. When temperature rates of change are excessive, as in uncontrolled wave soldering, large visible cracks are formed.

Thermal shock has two manifestations obvious visible cracks and the more insidious, invisible micro crack. The same forces are involved but on a smaller magnitude so smaller cracks are formed. Again it starts in the middle of the exposed surface at or just under the ceramic / termination interface and propagates slowly with temperature changes or assembly flexure during handling. In a matter of weeks a micro crack can propagate through the ceramic causing open, intermittent or excessive leakage currents, a time bomb due to processing.

Thermal shock cracks are always caused by improper solder processing or clearing. Wave soldering is the biggest culprit because it has the highest heat transfer rate (using liquid metal) and the largest temperature changes with cause both visible and micro cracks. Vapor phase soldering has the second highest heat transfer rate and temperature changes that can induce micro cracks when inadequate preheat is used. Infrared (IR) reflow soldering has the lowest heat transfer rates and thermal shock is unheard of for this soldering technique. Assembly cleaning cannot be ignored because thermal shock can occur during heating or cooling. An assembly should be allowed to cool to less than 60℃ before it is subjected to the cleaning process.

It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4℃/second and a target figure 2℃/second is recommended. An 80℃ to 120℃ temperature differential between the component surface and the soldering temperature is preferred.