

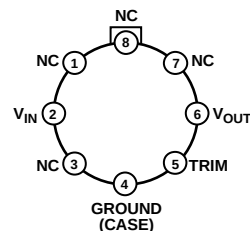
FEATURES

- 10 V output, $\pm 0.3\%$ maximum
- Adjustment range, $\pm 3\%$ minimum
- Excellent temperature stability, 8.5 ppm/ $^{\circ}\text{C}$ maximum
- Low noise, 30 μV p-p maximum
- Low supply current, 1.4 mA maximum
- Wide input voltage range, 12 V to 40 V
- High load driving capability, 10 mA
- No external components
- Short-circuit proof

GENERAL DESCRIPTION

The REF01 precision voltage reference provides a stable 10 V output that can be adjusted over a 3% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 12 V to 40 V, a low current drain of 1 mA, and excellent temperature stability are achieved with an improved band gap design. Low cost, low noise, and low power make the REF01 an excellent choice whenever a stable voltage reference is required. Applications include DACs and ADCs, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available. For new designs, refer to ADR01.

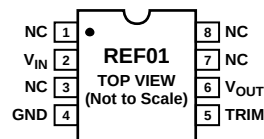
PIN CONFIGURATIONS



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

00373-F-001

Figure 1. TO-99 (J Suffix)



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

00373-F-002

Figure 2. 8-Lead PDIP (P-Suffix)
8-Lead CERDIP (Z-Suffix)
8-Lead SOIC (S-Suffix)

OUTPUT RESISTORS

REF01 OPTION	R9	R11	R12
P AND S PACKAGES	18k Ω	4.5k Ω	33.3k Ω
J AND Z PACKAGES, AND 883C PRODUCT	50k Ω	2k Ω	16.7k Ω

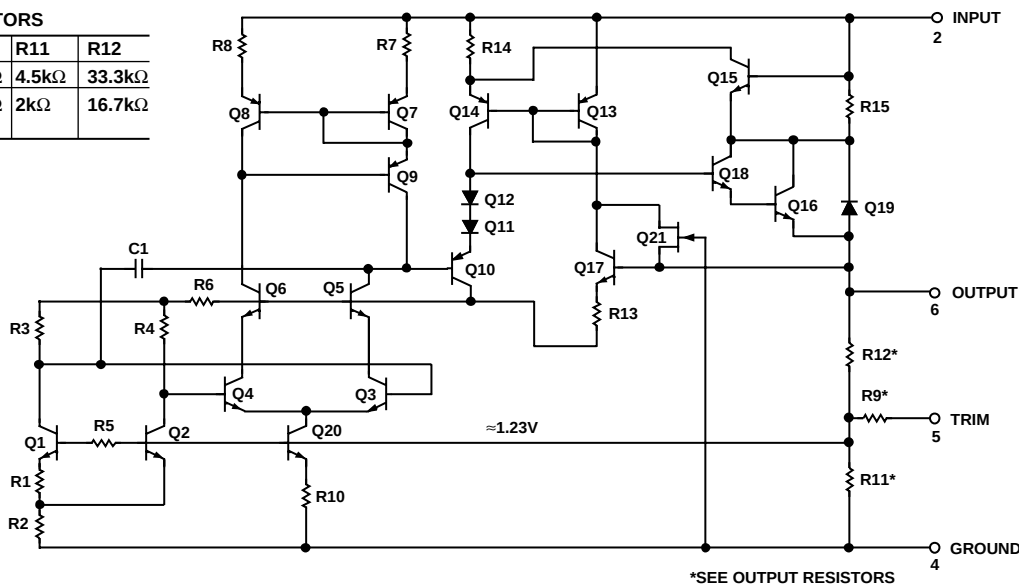


Figure 3. Simplified Schematic

00373-F-003

Rev. H

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REVISION HISTORY

12/05—Rev. G to Rev. H

Changes to Figure 12.....	8
Changes to Ordering Guide	12

2/05—Rev. F to Rev. G

Changes to Electrical Specifications	3
Changes to Electrical Specifications	4

7/04—Rev. E to Rev. F

Updated Format.....	Universal
Changes to Simplified Schematic	1
Changes to Specifications	3
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2/04—Rev. D to Rev. E

Changes to Simplified Schematic	1
Changes to Ordering Guide	4
Replaced Figure 6	5
Replaced Figure 7	5

10/03—Rev. C to Rev. D

Changes to Features	1
Changes to Electrical Specifications	2
Deleted Figure 13.....	3
Deleted Wafer Test Limits	4
Deleted Typical Electrical Characteristics.....	4
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Updated Outline Dimensions.....	8

10/02—Rev. B to Rev. C

Edits to Features.....	1
Delete RC-Suffix.....	1
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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

@ $V_{IN} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	REF01A/REF01E			REF01H			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	$I_L = 0\text{ mA}$	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{TRIM}	$R_P = 10\text{ k}\Omega$	± 3.0	± 3.3		± 3.0	± 3.3		%
Output Voltage Noise ¹	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		30			30		$\mu\text{V p-p}$
S, Z, P Packages	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		35			35		$\mu\text{V p-p}$
J, 883 Parts									
Line Regulation ²		$V_{IN} = 13\text{ V to } 33\text{ V}$		0.006	0.010		0.006	0.010	%/V
Load Regulation ²		$I_L = 0\text{ mA to } 10\text{ mA}$		0.005	0.008		0.006	0.010	%/mA
Turn-On Settling Time ³	t_{ON}	To $\pm 0.1\%$ of final value		5			5		μs
Quiescent Supply Current	I_{SY}	No load		1.0	1.4		1.0	1.4	mA
Load Current	I_L		10			10			mA
Sink Current ⁴	I_S		-0.3	-0.5		-0.3	-0.5		mA
Short-Circuit Current	I_{SC}	$V_O = 0$		30			30		mA

¹ Sample tested.

² Line and load regulation specifications include the effect of self-heating.

³ Guaranteed by design, not production tested.

⁴ During sink current test, the device meets the output voltage specified.

@ $V_{IN} = 15\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for REF01A/REF01E, and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for REF01H, and $I_L = 0\text{ mA}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	REF01A/REF01E			REF01H			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage Change	ΔV_{OT}	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.02	0.06		0.07	0.17	%
with Temperature ^{1, 2}		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.06	0.15		0.18	0.45	%
Output Voltage	TCV_O			3.0	8.5		10.0	25.0	ppm/ $^\circ\text{C}$
Temperature Coefficient ³									
Change in V_O Temperature Coefficient		$R_P = 10\text{ k}\Omega$		0.7			0.7		ppm/%
with Output Adjustment									
Line Regulation		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.007	0.012		0.007	0.012	%/V
($V_{IN} = 13\text{ V to } 33\text{ V}$) ⁴		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.009	0.015		0.009	0.015	%/V
Load Regulation		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.006	0.010		0.007	0.012	%/mA
($I_L = 0\text{ mA to } 8\text{ mA}$) ⁴		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.007	0.012		0.009	0.015	%/mA

¹ ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10 V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10\text{ V}} \right| \times 100$$

² ΔV_{OT} specification applies trimmed to 10000 V or untrimmed.

³ TCV_O is defined as ΔV_{OT} divided by the temperature range; therefore,

$$TCV_O(0^\circ\text{C to } 70^\circ\text{C}) = \frac{\Delta V_{OT}(0^\circ\text{C to } 70^\circ\text{C})}{70^\circ\text{C}} \text{ and } TCV_O(-55^\circ\text{C to } 125^\circ\text{C}) = \frac{\Delta V_{OT}(-55^\circ\text{C to } 125^\circ\text{C})}{180^\circ\text{C}}$$

⁴ Line and load regulation specifications include the effect of self-heating.

REF01

@ $V_{IN} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	REF01C			Unit
			Min	Typ	Max	
Output Voltage	V_O	$I_L = 0\text{ mA}$	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{TRIM}	$R_P = 10\text{ k}\Omega$	± 2.7	± 3.3		%
Output Voltage Noise ¹						
S, Z, P Packages	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		30		$\mu\text{V p-p}$
J, 883 Parts	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		35		$\mu\text{V p-p}$
Line Regulation ²		$V_{IN} = 13\text{ V to }33\text{ V}$		0.009	0.015	%/V
Load Regulation ²		$I_L = 0\text{ mA to }8\text{ mA}$		0.006	0.015	%/mA
Turn-On Settling Time ³	t_{ON}	To $\pm 0.1\%$ of final value		5		μs
Quiescent Supply Current	I_{SY}	No load		1.0	1.6	mA
Load Current	I_L		8			mA
Sink Current ⁴	I_S		-0.3	-0.5		mA
Short-Circuit Current	I_{SC}	$V_O = 0$		30		mA

¹ Sample tested.

² Line and load regulation specifications include the effect of self-heating.

³ Guaranteed by design, not production tested.

⁴ During sink current test, the device meets the output voltage specified.

@ $V_{IN} = 15\text{ V}$, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for REF01CJ, REF01CZ, and $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for REF01CP and REF01CS, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	REF01C			Unit
			Min	Typ	Max	
Output Voltage Change with Temperature ^{1,2}	ΔV_{OT}			0.14	0.45	%
Output Voltage Temperature Coefficient ³	TCV_O			20	65	ppm/ $^\circ\text{C}$
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10\text{ k}\Omega$		0.7		ppm/ $^\circ\text{C}$
Line Regulation ⁴		$V_{IN} = 13\text{ V to }30\text{ V}$		0.011	0.018	%/V
Load Regulation ⁴		$I_L = 0\text{ to }5\text{ mV}$		0.008	0.018	%/mA

¹ ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10 V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10\text{ V}} \right| \times 100$$

² ΔV_{OT} specification applies trimmed to $\pm 10,000\text{ V}$ or untrimmed.

³ TCV_O is defined as ΔV_{OT} divided by the temperature range; therefore,

$$TCV_O(0^\circ\text{C to }70^\circ\text{C}) = \frac{\Delta V_{OT}(0^\circ\text{C to }70^\circ\text{C})}{70^\circ\text{C}} \text{ and } TCV_O(-55^\circ\text{C to }125^\circ\text{C}) = \frac{\Delta V_{OT}(-55^\circ\text{C to }125^\circ\text{C})}{180^\circ\text{C}}$$

⁴ Line and load regulation specifications include the effect of self-heating.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating ¹
Input Voltage	40 V
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite
Storage Temperature Range	
J, S, and Z Packages	–65°C to +150°C
P Package	–65°C to +125°C
Operating Temperature Range	
REF01A	–55°C to +125°C
REF01CJ	0°C to 70°C
REF01CP, REF01CS, REF01E, REF01H	–40°C to +85°C
Junction Temperature (T_J)	–65°C to +150°C
Lead Temperature (Soldering @ 60 sec)	300°C

¹ Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA} ¹	θ_{JC}	Unit
TO-99 (J)	170	24	°C/W
8-Lead CERDIP (Z)	162	26	°C/W
8-Lead PDIP (P)	110	50	°C/W
8-Pin SOIC (S)	160	44	°C/W

¹ θ_{JA} is specified for worst-case mounting conditions; that is, θ_{JA} is specified for device in socket for TO, CERDIP, and PDIP packages. θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

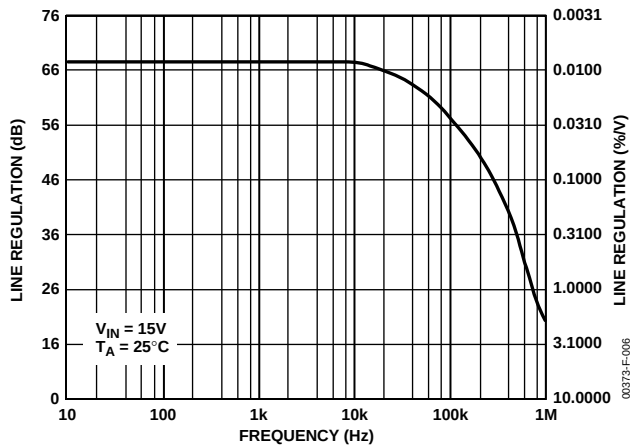


Figure 4. Line Regulation vs. Frequency

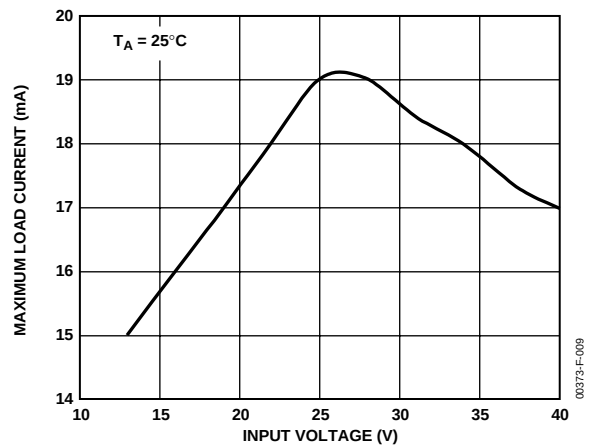


Figure 7. Maximum Load Current vs. Input Voltage

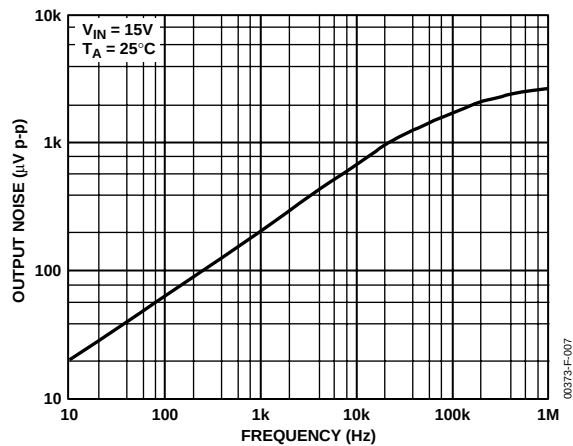
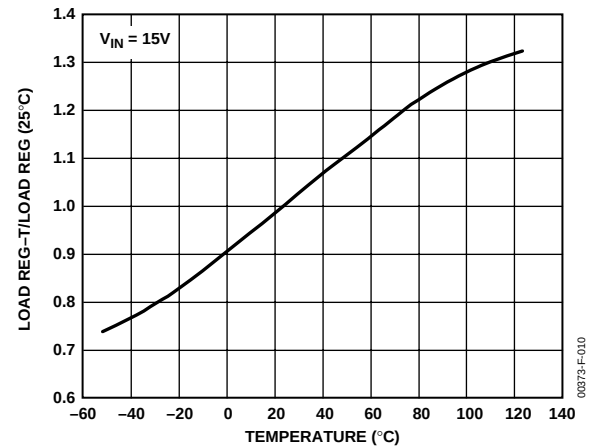
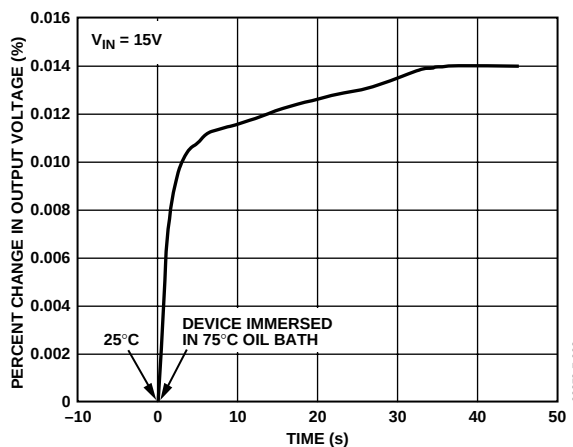
Figure 5. Output Wideband Noise vs. Bandwidth
(0.1 Hz to Frequency Indicated)Figure 8. Normalized Load Regulation ($\Delta I_L = 10$ mA) vs. Temperature

Figure 6. Output Change due to Thermal Shock

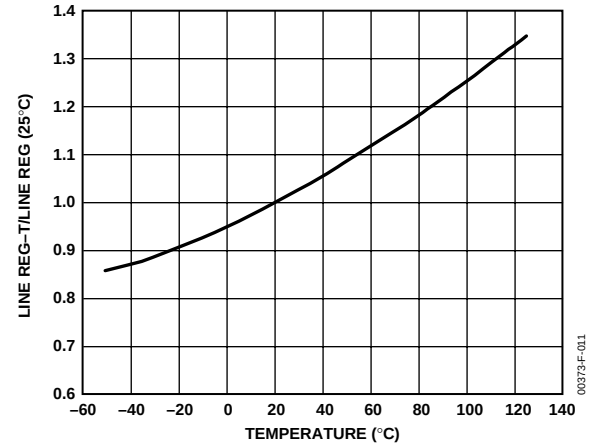


Figure 9. Normalized Line Regulation vs. Temperature

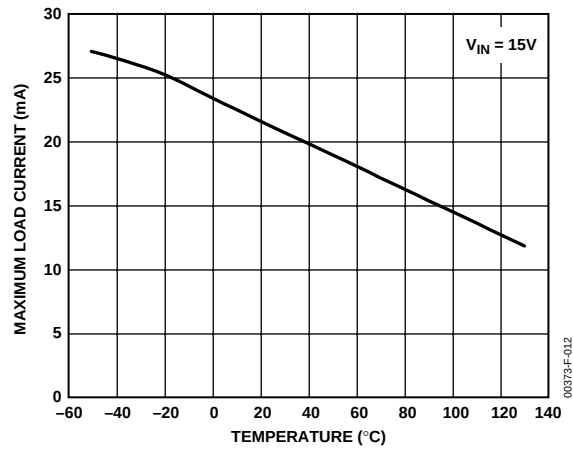


Figure 10. Maximum Load Current vs. Temperature

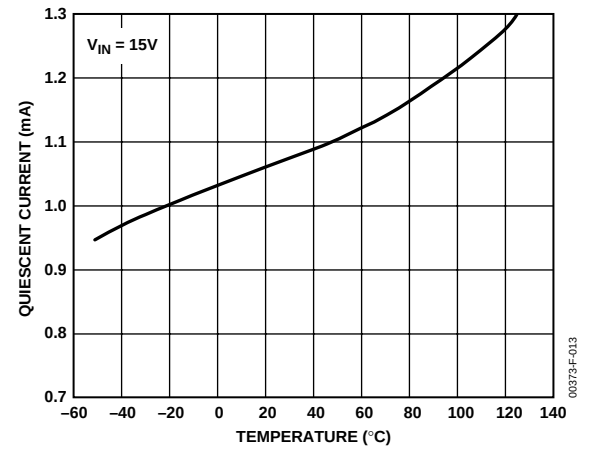


Figure 11. Quiescent Current vs. Temperature

APPLICATIONS

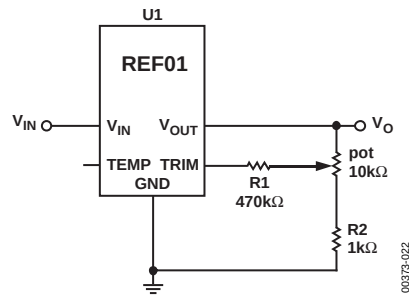


Figure 12. Output Adjustment

The REF01 trim terminal can be used to adjust the output voltage over a $10\text{ V} \pm 300\text{ mV}$ range. This feature lets the system designer trim system errors by setting the reference to a voltage other than 10 V. The output also can be set exactly to 10.000 V or to 10.240 V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/°C for 100 mV of output adjustment.

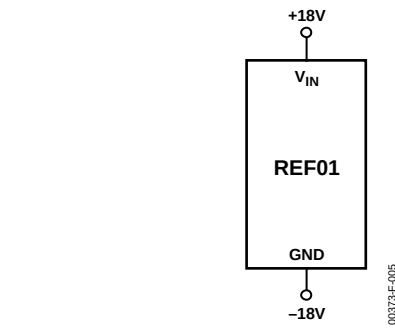
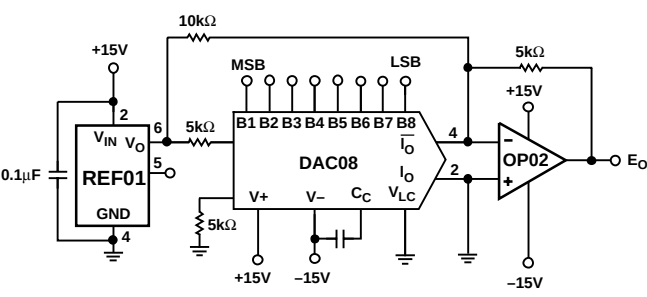


Figure 13. Burn-In Circuit



	B1	B2	B3	B4	B5	B6	B7	B8	E
POS. FULL SCALE -1LSB	1	1	1	1	1	1	1	1	+4.960
ZERO SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL SCALE +1LSB	0	0	0	0	0	0	0	1	-4.960
NEG. FULL SCALE	0	0	0	0	0	0	0	0	-5.000

Figure 14. Burn-In Circuit

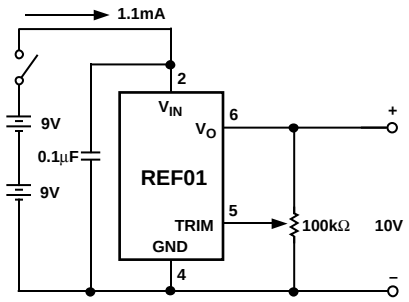


Figure 15. Precision Calibration Standard

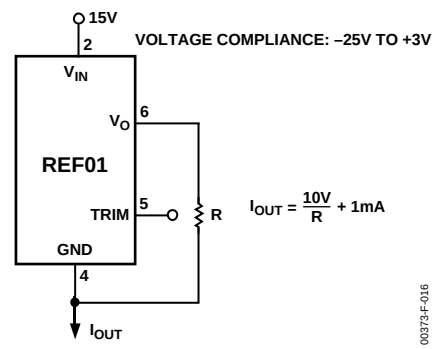


Figure 16. Current Source

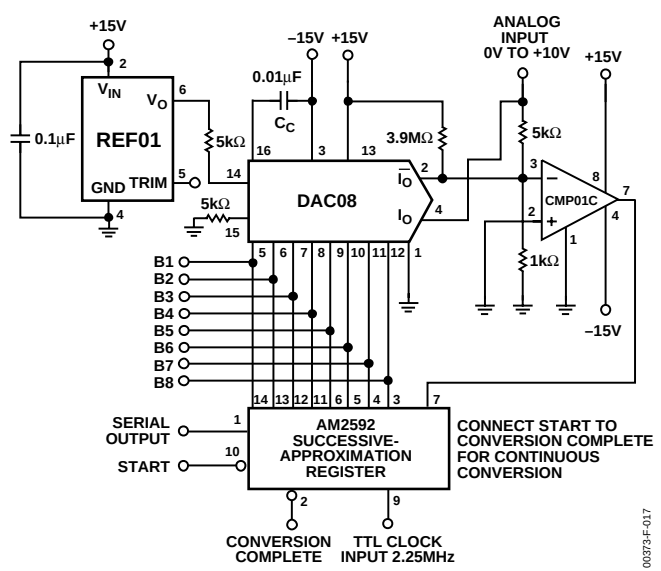


Figure 17. DAC Reference



Figure 18. $\pm 10\text{ V}$ Reference



Figure 19. Current Sink

PRECISION CURRENT SOURCE

A current source with 25 V output compliance and excellent output impedance can be obtained using this circuit. REF01 keeps the line voltage and power dissipation constant in the device; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3 \mu\text{V/V}$ PSRR of the OP02E creates an 8 ppm change ($3 \mu\text{V/V} \times 25 \text{ V}/10 \text{ V}$) in output current over a 25 V range. For example, a 10 mA current source can be built ($R = 1 \text{ k}\Omega$) with $300 \text{ M}\Omega$ output impedance.

$$R_o = \frac{25 \text{ V}}{8 \times 10^{-6} \times 10 \text{ mA}}$$

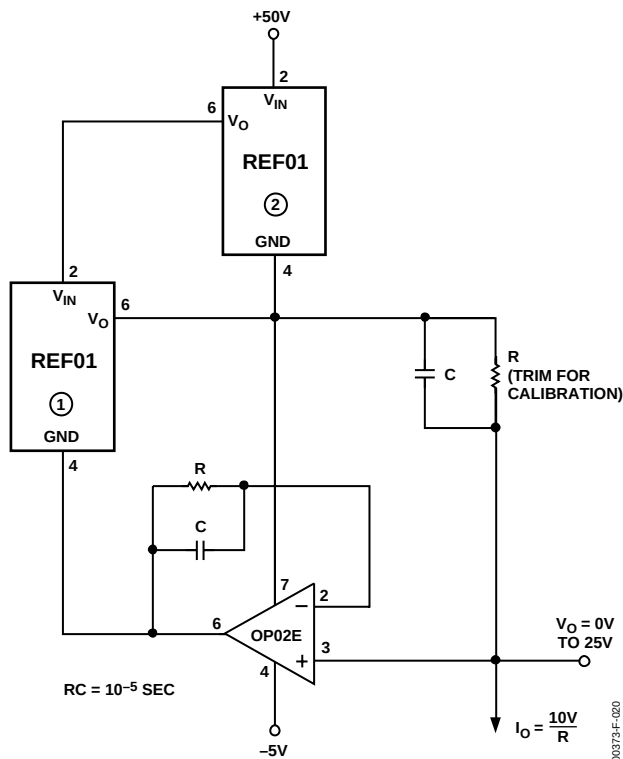


Figure 20. Precision Current Source

SUPPLY BYPASSING

For best results, it is recommended that the power supply pin be bypassed with a $0.1 \mu\text{F}$ disc ceramic capacitor.

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF01s can be stacked to yield 10 V, 20 V, and 30 V outputs. An additional advantage is near-perfect line regulation of the 10.0 V and 20.0 V output. A 32 V to 60 V input change produces an output change that is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SV}) of the 20 V regulator.

In general, any number of REF01s can be stacked this way. For example, 10 devices will yield outputs of 10 V, 20 V, 30 V . . . 100 V. The line voltage can change from 105 V to 130 V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21 mA).

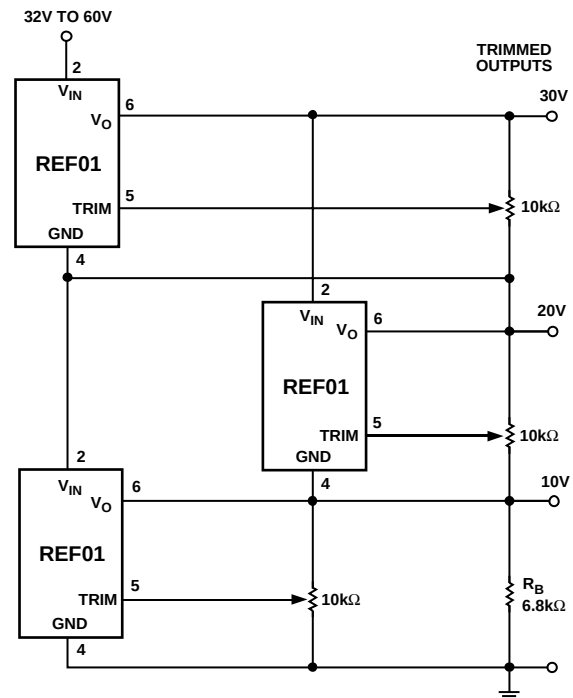
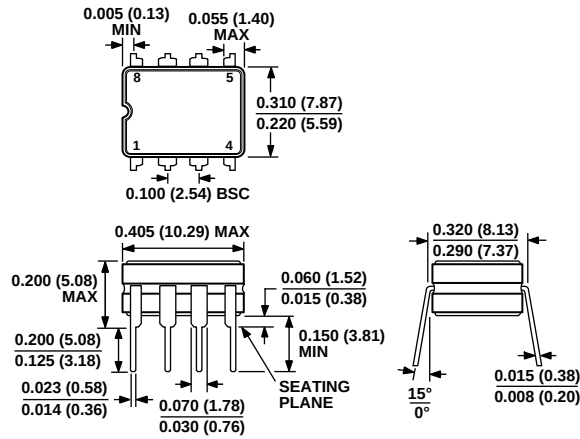


Figure 21. Reference Stack

OUTLINE DIMENSIONS



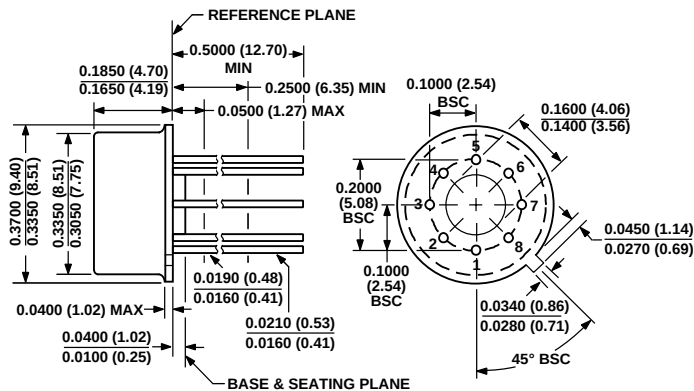
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 22. 8-Lead Ceramic Dual In-Line Package [CERDIP]

(Q-8)

Z-Suffix

Dimensions shown in inches and (millimeters)



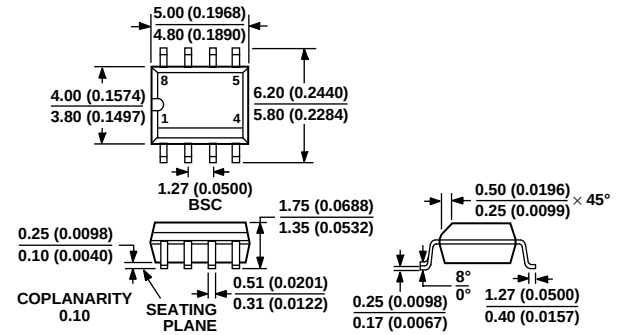
COMPLIANT TO JEDEC STANDARDS MO-002-AK
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 8-Lead Metal Header [TO-99]

(H-08)

J-Suffix

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

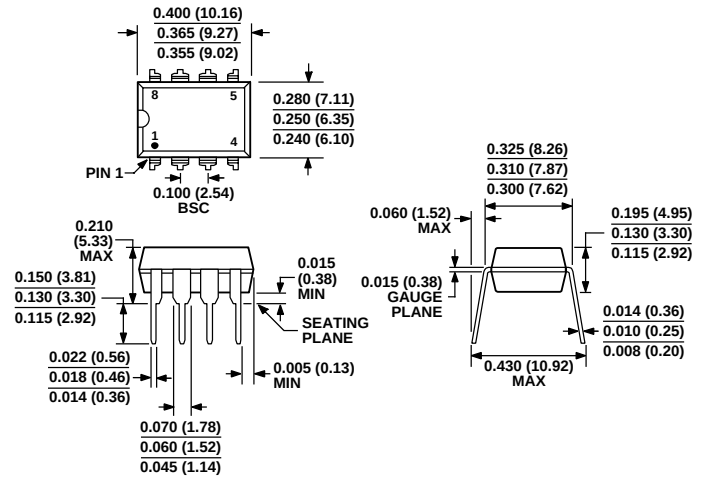
Figure 24. 8-Lead Standard Small Outline Package [SOIC]

Narrow Body

(R-8)

S-Suffix

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-001-BA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 25. 8-Lead Plastic Dual In-Line Package [PDIP]

Narrow Body

(N-8)

P-Suffix

Dimensions shown in inches and (millimeters)