DN74LS160A 74LS160A

Synchronous Decade Counters

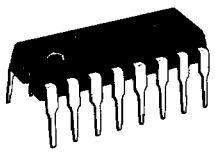
■ Description

DN74LS160A is a settable synchronous decade counter with direct-coupled reset input.

■ Features

- Direct-coupled reset input and synchronous set input
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 32MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

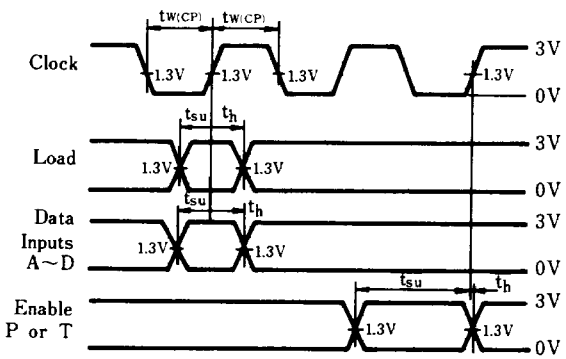


16-pin plastic DIL package

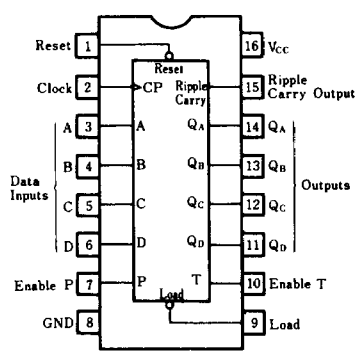
P-5

16-pin Panaflat package (SO-16D)

■ Timing definition



Pin configuration (top view)



■ Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		25	MHz
Clock pulse width		$t_{W(CP)}$	25			ns
Reset pulse width		$t_{W(Reset)}$	20			ns
Set-up time	Data A, B, C, D	t_{su}	20			ns
	Enable P, T		20			ns
	Load		20			ns
Hold time		t_h	0			ns

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	Data, Enable, P	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	Load, Clock, Enable, T						40	μA
	Reset						20	μA
	Data, Enable, P	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	Load, Clock, Enable, T						−0.8	mA
	Reset						−0.4	mA
	Data, Enable, P	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	A
	Load, Clock, Enable, T						0.2	mA
	Reset						0.1	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$ $V_o=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current***		I_{CCH}	$V_{CC}=5.25V$			18	31	mA
		I_{CCL}	$V_{CC}=5.25V$			19	32	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** I_{CCH} is measured first with all outputs open and all inputs at HIGH; next it is measured again under the same conditions except with the load inputs at LOW.

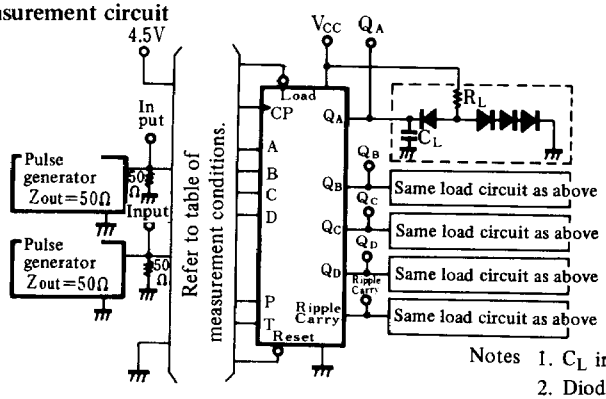
I_{CCL} is measured first with all outputs open and all inputs at LOW; next it is measured again under the same condition except with the clock inputs at LOW.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L=15pF$ $R_L=2k\Omega$	25	32		MHz
Propagation delay time	t_{PLH}	Clock	Ripple Carry			20	35	ns
	t_{PHL}					18	35	ns
	t_{PLH}	Clock (Load="H")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Clock (Load="L")	$Q_A \sim Q_D$			13	24	ns
	t_{PHL}					18	27	ns
	t_{PLH}	Enable T	Ripple Carry			9	16	ns
	t_{PHL}					9	25	ns
	t_{PHL}	Reset	$Q_A \sim Q_D$			20	28	ns

※ Switching parameter measurement information

1. Measurement circuit



Notes 1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161.

2. Table of measurement conditions

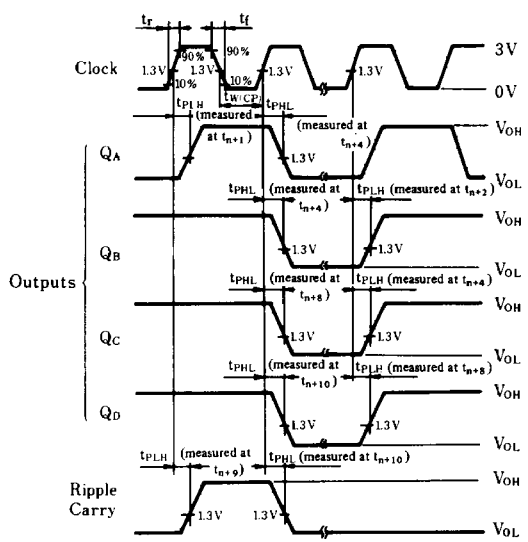
Parameter	Inputs/Outputs	Inputs									Outputs				
		Reset	Load	Enable P	Enable T	Clock	Data A	Data B	Data C	Data D	Q_A	Q_B	Q_C	Q_D	Ripple Carry
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CP→Ripple Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND					OUT
	CP→Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	
	CP→Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*	OUT	OUT	OUT	OUT	
	Enable T→Ripple Carry	4.5V	GND	4.5V	IN	IN**	4.5V	GND	GND	4.5V					OUT
	Reset→Q	IN	GND	GND	GND	IN**	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	

* Set to this state in accordance with measured output so that none of the various outputs, Q_A, Q_B, Q_C, and Q_D, exceeds HIGH, LOW, LOW, and HIGH, respectively.

** Applied for initialization.

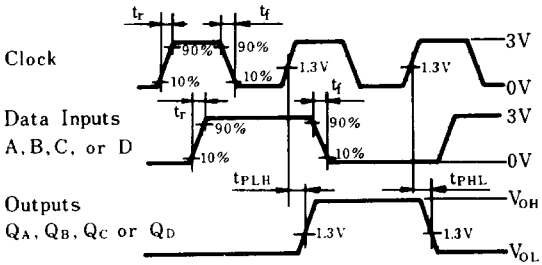
3.Waveforms

Waveforms-1 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, Ripple Carry)



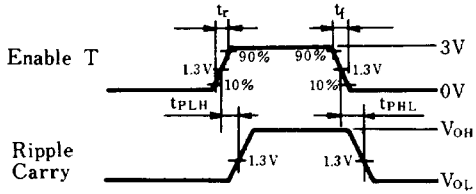
Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 5ns$, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.
3. t_n is the bit time when all outputs are LOW.

Waveforms-2 t_{PLH}, t_{PHL} (Clock → Q)



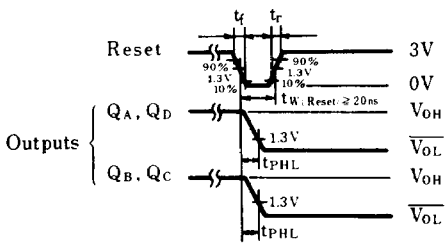
Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns.
2. Clock input: PRR = 1MHz, duty cycle = 50%.
3. Data input: PRR = 500kHz, duty cycle = 50%.

Waveforms-3 t_{PLH}, t_{PHL} (Enable T→Ripple Carry)



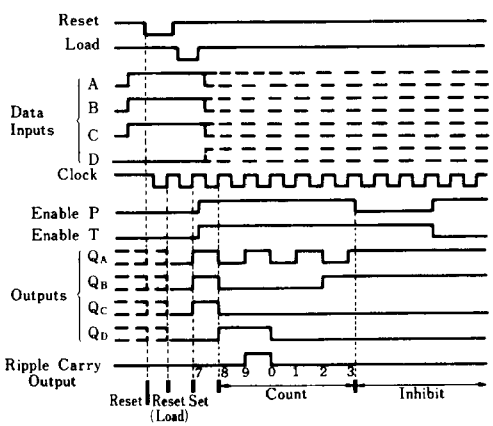
Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR=1MHz

Waveforms-4 t_{PHL} (Reset → Q)



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns

■ Timing chart



■ Logic diagram