HARRIS Semiconductor

# CD74HC191, CD74HCT191

## High Speed CMOS Logic Presettable Synchronous 4-Bit Up/Down Counters

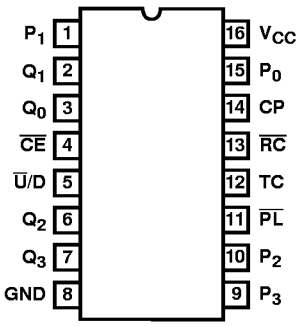
August 1997

## Features

- Synchronous Counting and Asynchronous Loading
- Two Outputs For N-Bit Cascading
- Look-Ahead Carry For High Speed Counting
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$

## Pinout

CD74HC191, CD74HCT191
(PDIP, SOIC)
TOP VIEW




## Description

The Harris CD74HC191, and CD74HCT191 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Presetting the counter to the number on preset data inputs ($P_0$-$P_3$) is accomplished by a Low asynchronous parallel load input ($\overline{PL}$). Counting occurs when $\overline{PL}$ is high, Count Enable ($\overline{CE}$) is low, and the Up/Down ($\overline{U}$/D) is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock (Figure 4).

When an overflow or underflow of the counter occurs, the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle.This output can be used for look-ahead carry in high speed cascading. The TC output also initiates the Ripple Clock. ($\overline{RC}$) output which, normally high, goes low and remains low for the low level portion of the clock pulse. These counters can cascaded using the Ripple Clock output (Figure 5).

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one or two counts as shown in state diagrams.

## Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CD74HC191E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74HCT191E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74HC191M | -55 to 125 | 16 Ld SOIC | M16.15 |
| CD74HCT191M | -55 to 125 | 16 Ld SOIC | M16.15 |
| CD74HC191W | -55 to 125 | Wafer | |

NOTES:

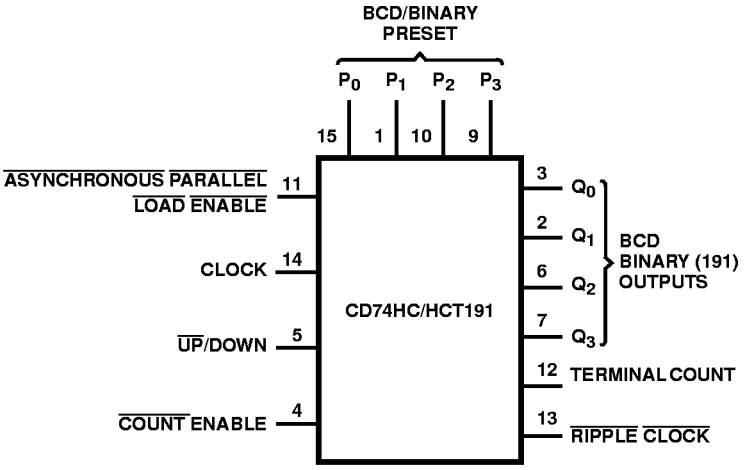
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.



File Number **1662.1**

## Functional Diagram




**TRUTH TABLE**

| INPUTS | | | | FUNCTION |
|---|---|---|---|---|
| $\overline{PL}$ | $\overline{CE}$ | $\overline{U}$/D | CP | |
| H | L | L | ↑ | Count Up |
| H | L | H | ↑ | Count Down |
| L | X | X | X | Asynchronous Preset |
| H | H | X | X | No Change |

NOTES:

3. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level
4. $\overline{U}$/D or $\overline{CE}$ should be changed only when clock is high.

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

| Thermal Resistance (Typical, Note 5) | $\theta_{JA}$ (°C/W) |
|---|---|
| PDIP Package | 90 |
| SOIC Package | 185 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

5. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 6) | $\Delta I_{CC}$ | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

6. For dual-supply systems theorectical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| P0-P3 | 0.4 |
| CP | 1.5 |
| $\overline{PL}$ | 1.5 |
| $\overline{U}$/D | 1.2 |
| $\overline{CE}$ | 1.5 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

## Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Setup TIme $P_n$ to $\overline{PL}$, $\overline{CE}$ to CP | $t_{SU}$ | - | 2 | 60 | - | - | 75 | - | 90 | - | ns |
| | | | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| | | | 6 | 10 | - | - | 13 | - | 15 | - | ns |

## Prerequisite For Switching Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $\overline{U}$/D to CP | $t_{SU}$ | - | 2 | 90 | - | - | 115 | - | 135 | - | ns |
| | | | 4.5 | 18 | - | - | 23 | - | 27 | - | ns |
| | | | 6 | 15 | - | - | 20 | - | 23 | - | ns |
| Hold Time | $t_H$ | - | 2 | 2 | - | - | 2 | - | 2 | - | ns |
| $P_n$ to $\overline{PL}$, $\overline{CE}$ to CP | | | 4.5 | 2 | - | - | 2 | - | 2 | - | ns |
| | | | 6 | 2 | - | - | 2 | - | 2 | - | ns |
| $\overline{U}$/D to CP | | | 2 | 0 | - | - | 0 | - | 0 | - | ns |
| | | | 4.5 | 0 | - | - | 0 | - | 0 | - | ns |
| | | | 6 | 0 | - | - | 0 | - | 0 | - | ns |
| Maximum Frequency (Note 7) | $f_{MAX}$ | - | 2 | 6 | - | - | 5 | - | 4 | - | MHz |
| | | | 4.5 | 30 | - | - | 25 | - | 20 | - | MHz |
| | | | 6 | 35 | - | - | 29 | - | 23 | - | MHz |
| Recovery Time | $t_{REC}$ | - | 2 | 60 | - | - | 75 | - | 90 | - | ns |
| | | | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| | | | 6 | 10 | - | - | 13 | - | 15 | - | ns |
| CP Pulse Width | $t_W$ | - | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| $\overline{PL}$ Pulse Width | $t_W$ | - | 2 | 100 | - | - | 125 | - | 150 | - | ns |
| | | | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| | | | 6 | 17 | - | - | 21 | - | 26 | - | ns |
| **HCT TYPES** | | | | | | | | | | | |
| Setup Time | $t_{SU}$ | - | | | | | | | | | |
| Pn to $\overline{PL}$, $\overline{CE}$ to CP | | | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| $\overline{U}$/D to CP | | | 4.5 | 18 | - | - | 23 | - | 27 | - | ns |
| Hold Time | $t_H$ | - | 4.5 | 2 | - | - | 2 | - | 2 | - | ns |
| Pn to $\overline{PL}$, $\overline{CE}$ to CP | | | | | | | | | | | |
| $\overline{U}$/D to CP | | | 4.5 | 0 | - | - | 0 | - | 0 | - | ns |
| Maximum Frequency (Note 7) | $f_{MAX}$ | - | 4.5 | 30 | - | - | 25 | - | 20 | - | MHz |
| Recovery Time | $t_{REC}$ | - | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| CP Pulse Width | $t_W$ | - | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| $\overline{PL}$ Pulse Width | $t_W$ | - | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 195 | - | 245 | - | 295 | ns |
| $\overline{PL}$ to $Q_n$ | | $C_L$ = 50pF | 4.5 | - | - | 39 | - | 49 | - | 59 | ns |
| | | $C_L$ = 15pF | 5 | - | 16 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 33 | - | 42 | - | 50 | ns |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Pn to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 175 | - | 220 | - | 265 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L$ = 15pF | 5 | - | 14 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 30 | - | 37 | - | 45 | ns |
| CP to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 170 | - | 215 | - | 255 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 34 | - | 43 | - | 51 | ns |
| | | $C_L$ = 15pF | 5 | - | 14 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 29 | - | 37 | - | 43 | ns |
| CP to $\overline{RC}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | $C_L$ = 15pF | 5 | - | 10 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 21 | - | 26 | - | 32 | ns |
| CP to TC | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 210 | - | 265 | - | 315 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 36 | - | 45 | - | 54 | ns |
| $\overline{U}$/D to $\overline{RC}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 150 | - | 190 | - | 225 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 30 | - | 38 | - | 45 | ns |
| | | $C_L$ = 15pF | 5 | - | 12 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 26 | - | 33 | - | 38 | ns |
| $\overline{U}$/D to TC | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 165 | - | 205 | - | 250 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 33 | - | 41 | - | 50 | ns |
| | | $C_L$ = 15pF | 5 | - | 13 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 28 | - | 35 | - | 43 | ns |
| $\overline{CE}$ to $\overline{RC}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| | | $C_L$ = 50pF | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | $C_L$ = 15pF | 5 | - | 10 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 21 | - | 26 | - | 32 | ns |
| Output Transition Time $Q_n$, TC, $\overline{RC}$ | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ | - | - | - | 55 | - | - | - | - | - | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay $\overline{PL}$ to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | $C_L$ =15pF | 5 | - | 17 | - | - | - | - | - | ns |
| $P_n$ to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | | $C_L$ =15p | 5 | - | 16 | - | - | - | - | - | ns |
| CP to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L$ =15p | 5 | - | 14 | - | - | - | - | - | ns |

## Switching Specifications Input $t_r$, $t_f$ = 6ns (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| CP to $\overline{RC}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| | | $C_L$ =15p | 5 | - | 11 | - | - | - | - | - | ns |
| CP to TC | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| | | $C_L$ =15p | 5 | - | 18 | - | - | - | - | - | ns |
| $\overline{U}$/D to $\overline{RC}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 30 | - | 38 | - | 45 | ns |
| | | $C_L$ =15p | 5 | - | 12 | - | - | - | - | - | ns |
| $\overline{U}$/D to TC | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | | $C_L$ =15p | 5 | - | 16 | - | - | - | - | - | ns |
| $\overline{CE}$ to $\overline{RC}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| | | $C_L$ =15p | 5 | - | 11 | - | - | - | - | - | ns |
| Output Transition Time $Q_n$, TC, $\overline{RC}$ | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 15 | - | 19 | - | 22 | pF |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 8, 9) | $C_{PD}$ | 191 | - | - | 68 | - | - | - | - | - | pF |

NOTES:

7. Applies to noncascaded operation only. With cascaded counter clock-to-terminal propagation delays, count enable ($\overline{CE}$)-to-clock setup times, and count enable ($\overline{CE}$)-to-clock hold times determine max. clock frequency. For example, with these HC devices:

$$f_{MAX}(CP) = \frac{1}{CP-to-prop.delay + CE-to-setup + CE-to-CPHold} = \frac{1}{42+12+2} \approx 18MHz$$

8. $C_{PD}$ is used to determine the dynamic power consumption, per gate/package.
9. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where $f_i$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms

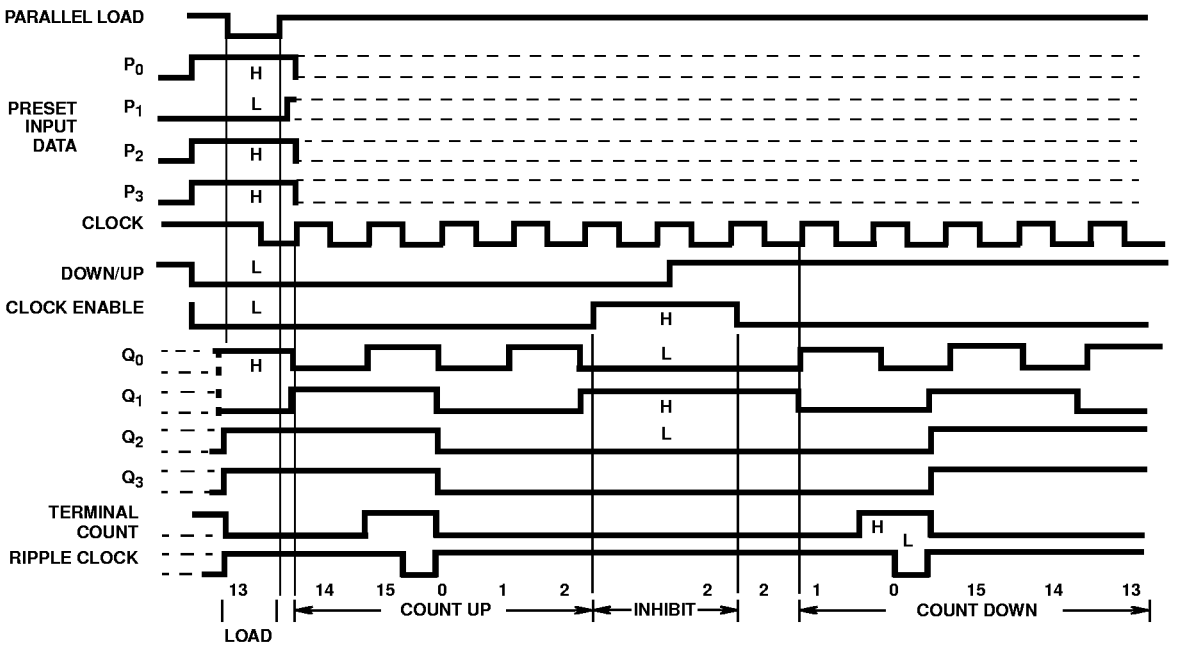
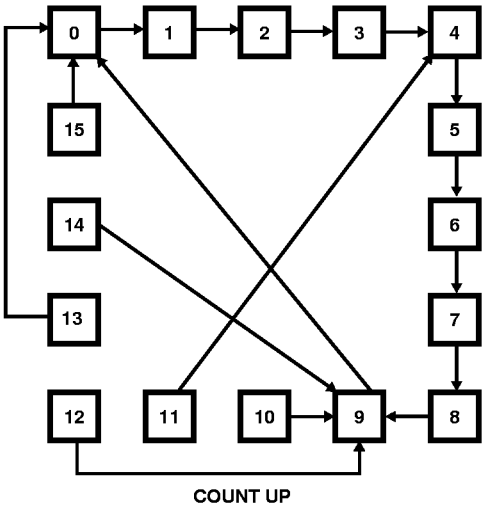
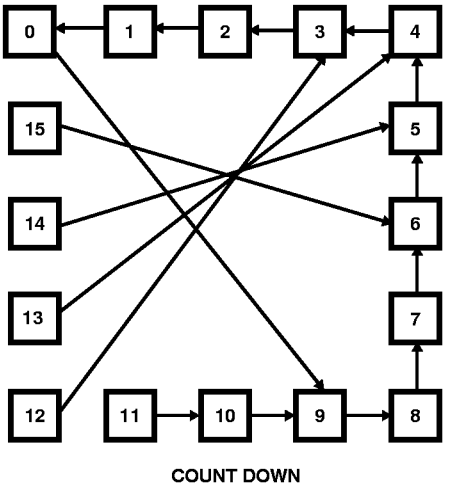



FIGURE 1. HC/HCT191 BINARY COUNTERS TYPICAL LOAD, COUNT ADN INHIBIT SEQUENCES

## Test Circuits and Waveforms (Continued)




NOTE: Illegal states in BCD counters corrected in one count.




NOTE: Illegal states in BCD counters corrected in one or two counts.

FIGURE 2. CD74HC191 STATE DIAGRAMS

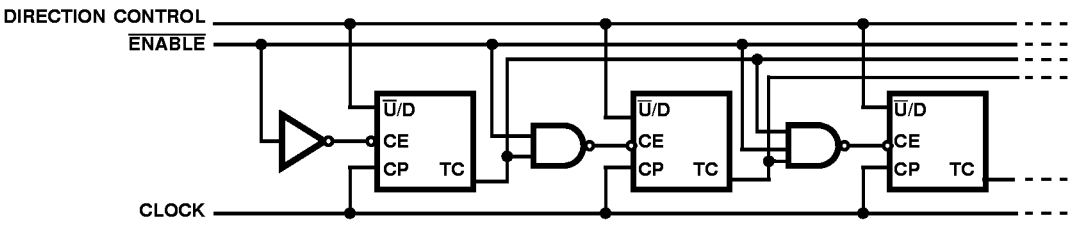



FIGURE 3. SYNCHRONOUS N-STAGE COUNTER WITH PARALLEL GATED TERMINAL COUNT

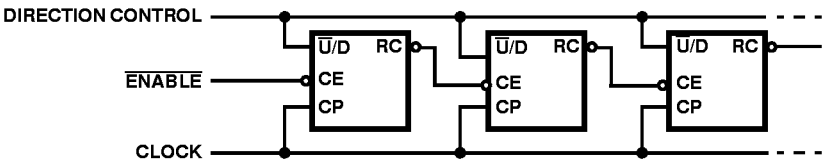



FIGURE 4. SYNCHRONOUS N-STAGE COUNTER USING RIPPLE CLOCK

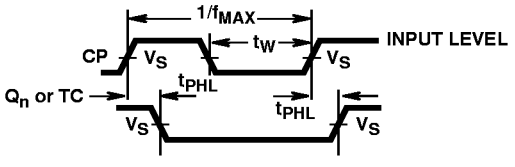



FIGURE 5.

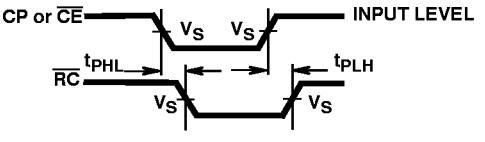



FIGURE 6.

## Test Circuits and Waveforms (Continued)

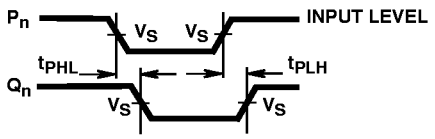



FIGURE 7.

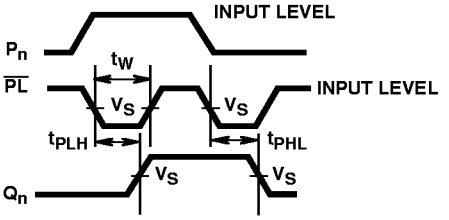



FIGURE 8.

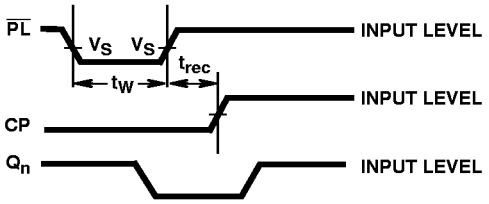



FIGURE 9.

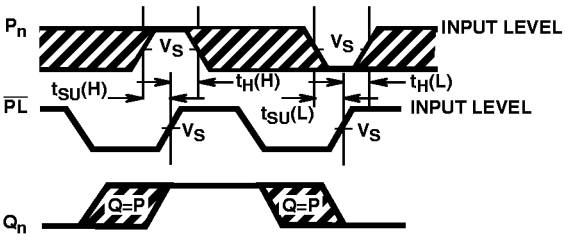



FIGURE 10.

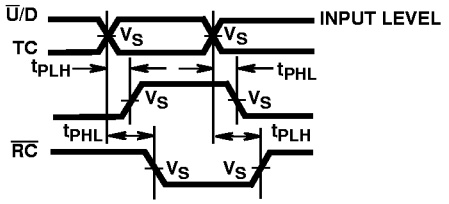



FIGURE 11.

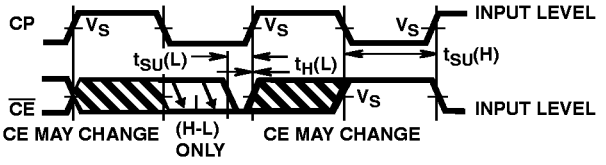



FIGURE 12.