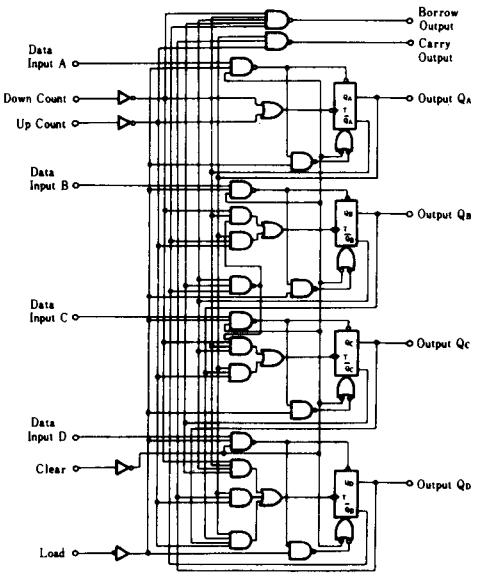
HD74LS192 ●Synchronous Up/Down Decade Counters (dual clock lines)

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high. This counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words. This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions.

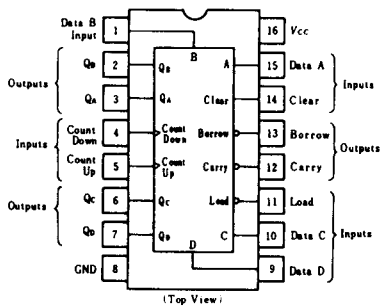
The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists.

The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Pulse width	t_w	20	—	—	ns
Setup time (Clear)	$t_{su(CLR)}$	40	—	—	ns
Setup time	t_{su}	20	—	—	ns
Hold time	t_h	3	—	—	ns

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■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
			$I_{OL}=8mA$	–	–	0.5	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$		–	19	34	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

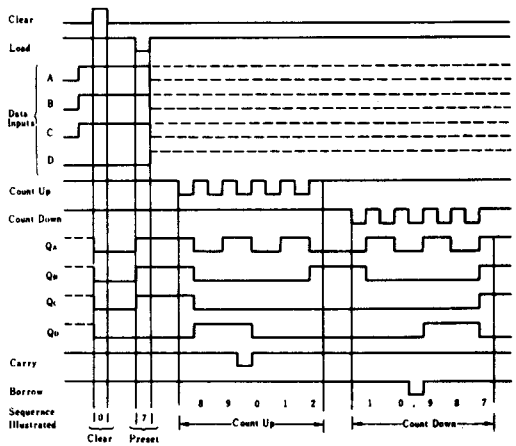
* V_{CC}=5V, Ta=25°C

** I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

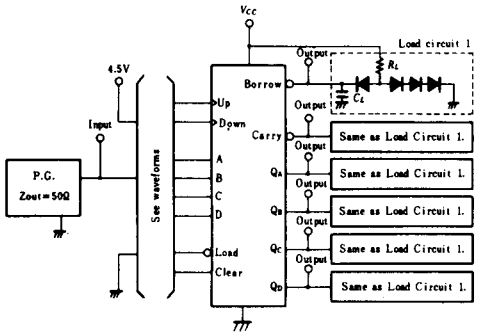
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	25	32	–	MHz
Propagation delay time	t_{PLH}	Count-up	Carry		–	17	26	ns
	t_{PHL}				–	18	24	
	t_{PLH}	Count-down	Borrow		–	16	24	ns
	t_{PHL}				–	15	24	
	t_{PLH}	Either Count	Q		–	27	38	ns
	t_{PHL}				–	30	47	
	t_{PLH}	Load	Q		–	24	40	ns
	t_{PHL}				–	25	40	
	t_{PHL}	Clear	Q		–	23	35	ns

■COUNT SEQUENCE



■TESTING METHOD

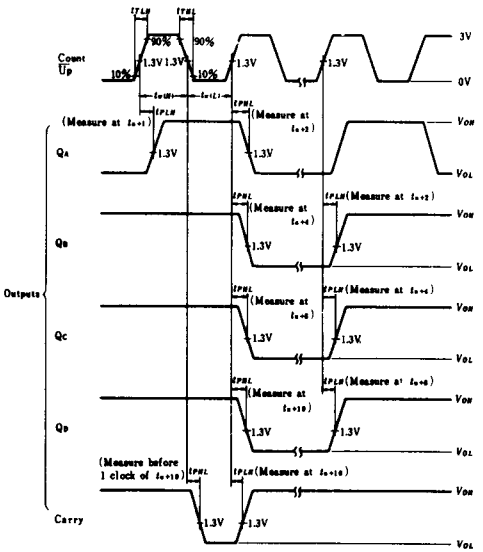
1) Test Circuit



Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

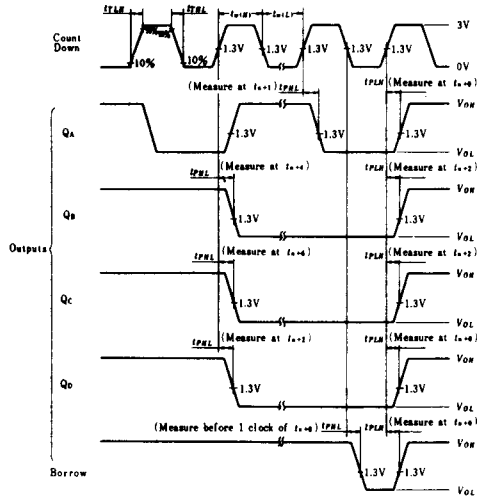
Input pulse: $t_{TLH}, t_{THL} \leqq 7$ns, PRR=500kHz (Data input).
PRR=1MHz (except data input)
Duty Cycle=50%

Waveform−1 f_{max}, t_{PLH}, t_{PHL} (Count Up)



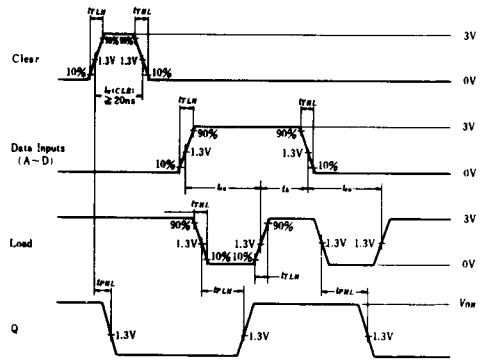
Notes) 1. Input pulse: $t_{TLH} \leqq 7$ns, $t_{THL} \leqq 7$ns, PRR=1MHz, duty cycle 50%
2. for f_{max}, t_{TLH}, $t_{THL} \leqq 2.5$ns
3. t_n is reference bit time when all outputs are low.

Waveform−2 f_{max}, t_{PLH}, t_{PHL} (Count Down)



Notes) 1. for f_{max}, t_{TLH}=$t_{THL} \leqq 2.5$ns.
2. t_n is reference bit time when all outputs are high.

Waveform−3 t_{PLH}, t_{PHL} (Load, Clear→Q)



Note) Input pulse: $t_{TLH} \leqq 7$ns, $t_{THL} \leqq 7$ns

2) Testing Table

Item	From input to output	Inputs								Outputs					
		CLR	Load	Up	Down	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Carry	Borrow
f_{max}		GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	–
		GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	–	OUT
t_{PLH} t_{PHL}	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	–
	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	–	OUT
	Load→Q	GND	IN	GND	GND	IN	IN	IN	IN	OUT	OUT	OUT	OUT	–	–
	Clear→Q	IN	IN*	GND	GND	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	–	–

* for initialized

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PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

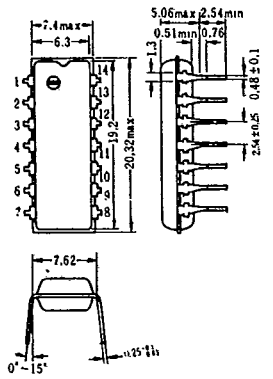
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

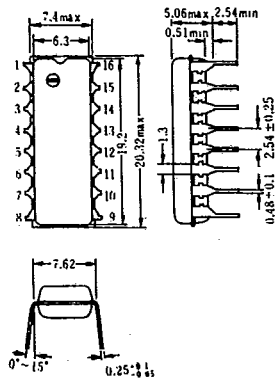
●14 Pin

DP-14



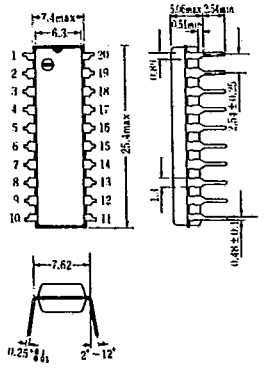
●16 Pin

DP-16



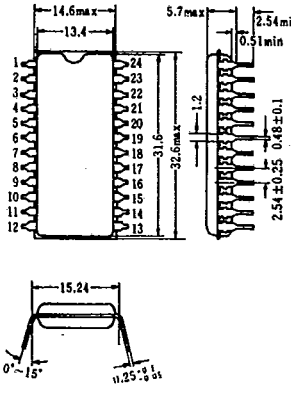
●20 Pin

DP-20



●24 Pin

DP-24



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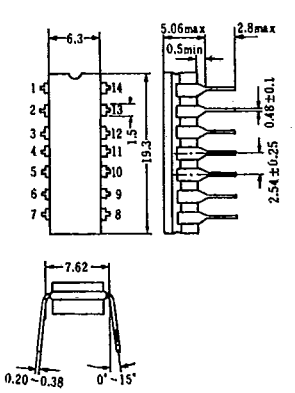
PACKAGING INFORMATIONS

■Cerdip

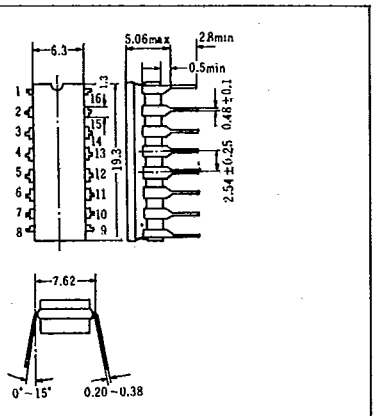
●14 Pin

DG-14



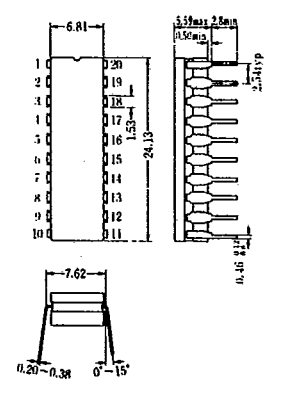
●16 Pin

DG-16



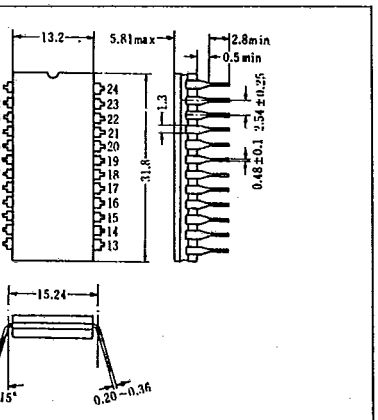
●20 Pin

DG-20



●24 Pin

DG-24



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