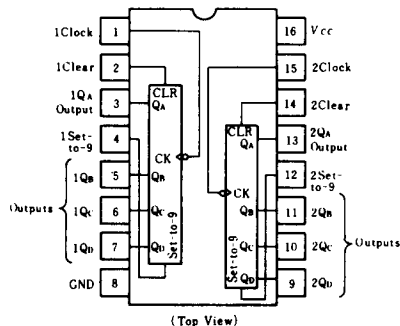


HD74LS490 • Dual 4-bit Decade Counters

This circuit contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single HD74LS490. Buffering on each output is provided to ensure that susceptibility to collector communication is reduced significantly. All inputs are diode-clamped to reduce the effects of line ringing. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

PIN ARRANGEMENT



RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Output current	I_{OH}	—	—	-400	μA
Output current	I_{OL}	—	—	8	mA
Count frequency	f_{count}	0	—	25	MHz
Pulse width	t_w	20	—	—	ns
Setup time	t_{su}	25	↓	—	ns

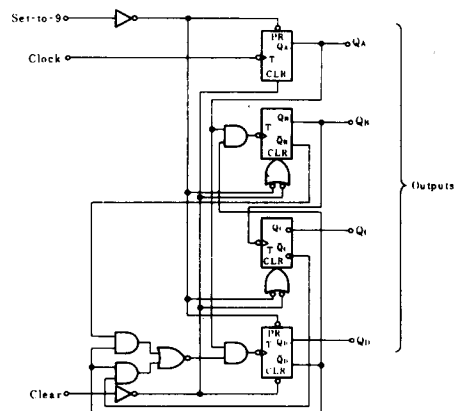
↓; The arrows indicates the falling edge from clock transition.

FUNCTION TABLE

CLEAR/SET-TO-9

Inputs		Outputs			
CLEAR	SET-TO-9	QA	QB	QC	QD
H	L	L	L	L	L
L	H	H	L	L	H
L	L	Count			

BLOCK DIAGRAM (1/2)



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	CLOCK	5.5	V
	CLEAR, SET-TO-9	7.0	
Operating temperature range	T_{op}	-20 ~ +75	°C
Storage temperature range	T_{stg}	-65 ~ +125	°C

BCD Count Sequence

Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		V_{IH}		2.0	—	—	V
		V_{IL}		—	—	0.8	V
Output voltage		V_{OH}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OH} = 400\mu\text{A}$	2.7	—	—	V
		V_{OL}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OL} = 4\text{mA}$	—	—	0.4	
			$I_{OL} = 8\text{mA}$	—	—	0.5	
Input current	Clear Set-to-9	I_{IH}	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$	—	—	20	μA
	Clock			—	—	100	
	Clear Set-to-9	I_{IL}	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$	—	—	-0.4	mA
	Clock			—	—	-1.6	
	Clear Set-to-9	I_i	$V_{CC} = 5.25\text{V}$	—	—	0.1	mA
	Clock			—	—	0.2	
			$V_i = 7\text{V}$	—	—	0.1	
			$V_i = 5.5\text{V}$	—	—	0.2	
Short-circuit output current		I_{OS}	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA
Supply current		I_{CC}^{**}	$V_{CC} = 5.25\text{V}$	—	15	26	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75\text{V}$, $I_{IH} = -18\text{mA}$	—	—	-1.5	V

* $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

** I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

■ SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	f_{max}	Clock	Q_A	$C_L=15\text{pF}$, $R_L=2\text{k}\Omega$	25	35	—	MHz
Propagation delay time	t_{PLH}	Clock	Q_A		—	12	20	ns
	t_{PHL}				—	13	20	
	t_{PLH}	Clock	Q_B, Q_D		—	24	39	
	t_{PHL}				—	26	39	
	t_{PLH}	Clock	Q_C		—	32	54	
	t_{PHL}				—	36	54	
	t_{PHL}	Clear	Any		—	24	39	
	t_{PLH}	Set-to-9	Q_A, Q_D		—	24	39	
	t_{PHL}		Q_B, Q_C		—	20	36	



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