

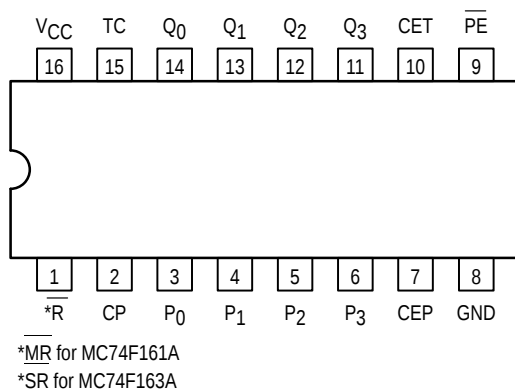


SYNCHRONOUS PRESETTABLE BINARY COUNTER

The MC74F161A and MC74F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74F161A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Frequency of 120 MHz

CONNECTION DIAGRAM

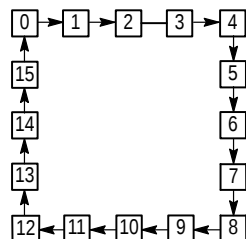


FUNCTION TABLE

SR	PE	CET	CEP	ACTION ON THE RISING CLOCK EDGE ($\uparrow$)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P_n Q_n)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

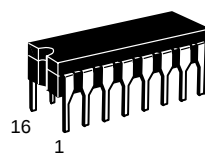
H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

STATE DIAGRAM

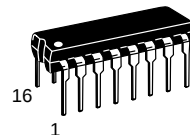


MC74F161A
MC74F163A

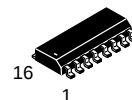
SYNCHRONOUS PRESETTABLE
BINARY COUNTER
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

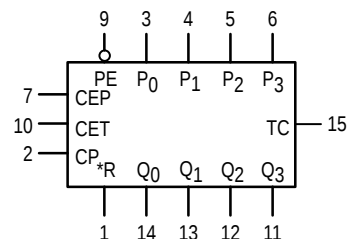


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXAJ Ceramic
MC74FXXXAN Plastic
MC74FXXXAD SOIC

LOGIC SYMBOL



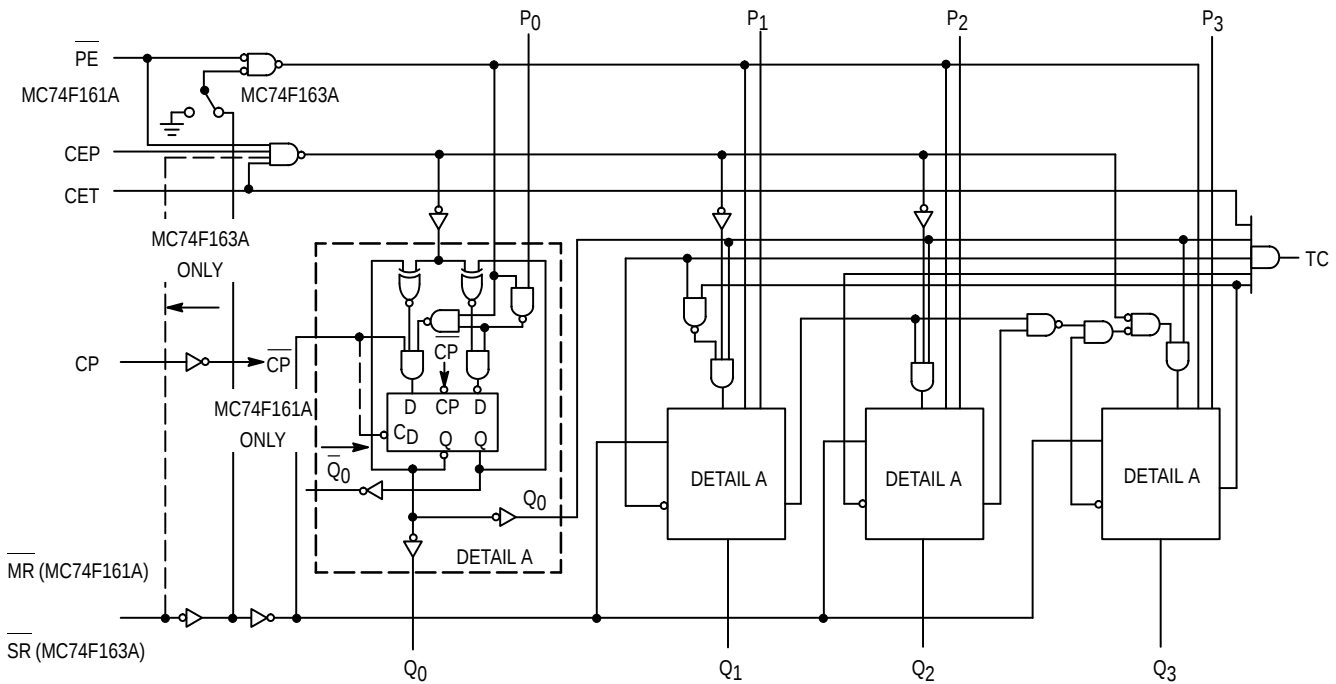
VCC = PIN 16
GND = PIN 8

*MR for MC74F161A
*SR for MC74F163A

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MC74F161A • MC74F163A

LOGIC DIAGRAM



NOTE:

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74F161A and MC74F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the MC74F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (MC74F161A), synchronous reset (MC74F163A), parallel load, count-up and hold. Five control inputs—Master Reset (MR, MC74F161A), Synchronous Reset (SR, MC74F163A), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Function Table. A LOW signal on MR overrides

all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and MR (MC74F161A) or SR (MC74F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74F161A and MC74F163A use D-type edge-triggered flip-flops and changing the SR, PE, CEP, and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

MC74F161A • MC74F163A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			– 1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage				–1.2	V	V _{CC} = MIN, I _{IN} = – 18 mA
V _{OH}	Output HIGH Voltage	74	2.5	3.4		V	I _{OH} = –1.0 mA, V _{CC} = 4.50 V
		74	2.7	3.4		V	I _{OH} = –1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Data, CEP, Clock PE, CET, SR				–0.6 –1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)		–60		– 150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current			37	55	mA	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is there-

fore not recommended for use as a clock or asynchronous reset for flip-flops, counters, or registers.

Logic Equations:

Count Enable = CEP • CET • $\overline{\text{PE}}$

TC = Q₀ • Q₁ • Q₂ • Q₃ • CET

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AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{max}	Maximum Count Frequency	100		90		MHz
t _{PLH}	Propagation Delay, Count	3.5	6.0	3.5	7.0	ns
t _{PHL}	CP to Q _n (PE Input HIGH)	3.5	10	3.5	11	
t _{PLH}	Propagation Delay	3.5	7.0	3.5	9.5	
t _{PHL}	CP to Q _n (PE Input LOW)	4.0	8.5	4.0	9.5	
t _{PLH}	Propagation Delay	5.0	14	5.0	15	ns
t _{PHL}	CP to TC	4.5	14	4.5	15	
t _{PLH}	Propagation Delay	2.5	7.5	2.5	8.5	ns
t _{PHL}	CET to TC	2.5	7.5	2.5	8.5	
t _{PHL}	Propagation Delay MR to Q _n (MC74F161A)	5.5	12	5.5	13	ns
t _{PHL}	Propagation Delay MR to TC (MC74F161A)	4.5	10.5	4.5	11.5	ns

AC OPERATING REQUIREMENTS

		74F		74F		
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
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Symbol	Parameter	Min	Max	Min	Max	Unit
t _S (H)	Setup Time, HIGH or LOW	5.0	5.0	5.0		ns
t _S (L)	CEP or CET to CP	5.0	5.0	5.0		
t _H (H)	Hold Time, HIGH or LOW	2.0	2.0	2.0		
t _H (L)	CEP or CET to CP	2.0	2.0	2.0		
t _W (H)	Clock Pulse Width (Load)	5.0	5.0	5.0		
t _W (L)	HIGH or LOW	5.0	5.0	5.0		ns
t _W (H)	Clock Pulse Width (Count)	4.0	4.0	4.0		
t _W (L)	HIGH or LOW	6.0	6.0	7.0		
t _W (L)	MR Pulse Width, LOW (MC74F161A)	5.0	5.0	5.0		ns
t _{rec}	Recovery Time, MR to CP (MC74F161A)	6.0	6.0	6.0		

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