

# I<sup>2</sup>C BUS Control 5-Input 2-Output AV Switch Monolithic IC MM1313

## Outline

This IC is a 5-input 2-output AV switch with I<sup>2</sup>C control, developed for use in televisions. Two outputs enable it to support two screens or "picture-in-picture".

## Features

1. Serial control by I<sup>2</sup>C bus.
2. 5-inputs, 2-outputs.
3. Video and audio system switches can be controlled independently.
4. 6dB amplifier built in to video system.
5. Built-in Y/C MIX circuit.
6. Slave address can be changed : 90H or 92H.
7. Audio muting possible by external pin.
8. Maintains high impedance even when I<sup>2</sup>C BUS line (SDA, SCL) power supply is off.
9. Built-in 3 value discrimination function.
10. On-chip power ON reset function.
11. Two types of audio input impedance : 60kΩ and 30kΩ.  
     MM1313AD : 60kΩ      MM1313BD : 30kΩ
12. Supports 2-screen or P-IN-P TV.

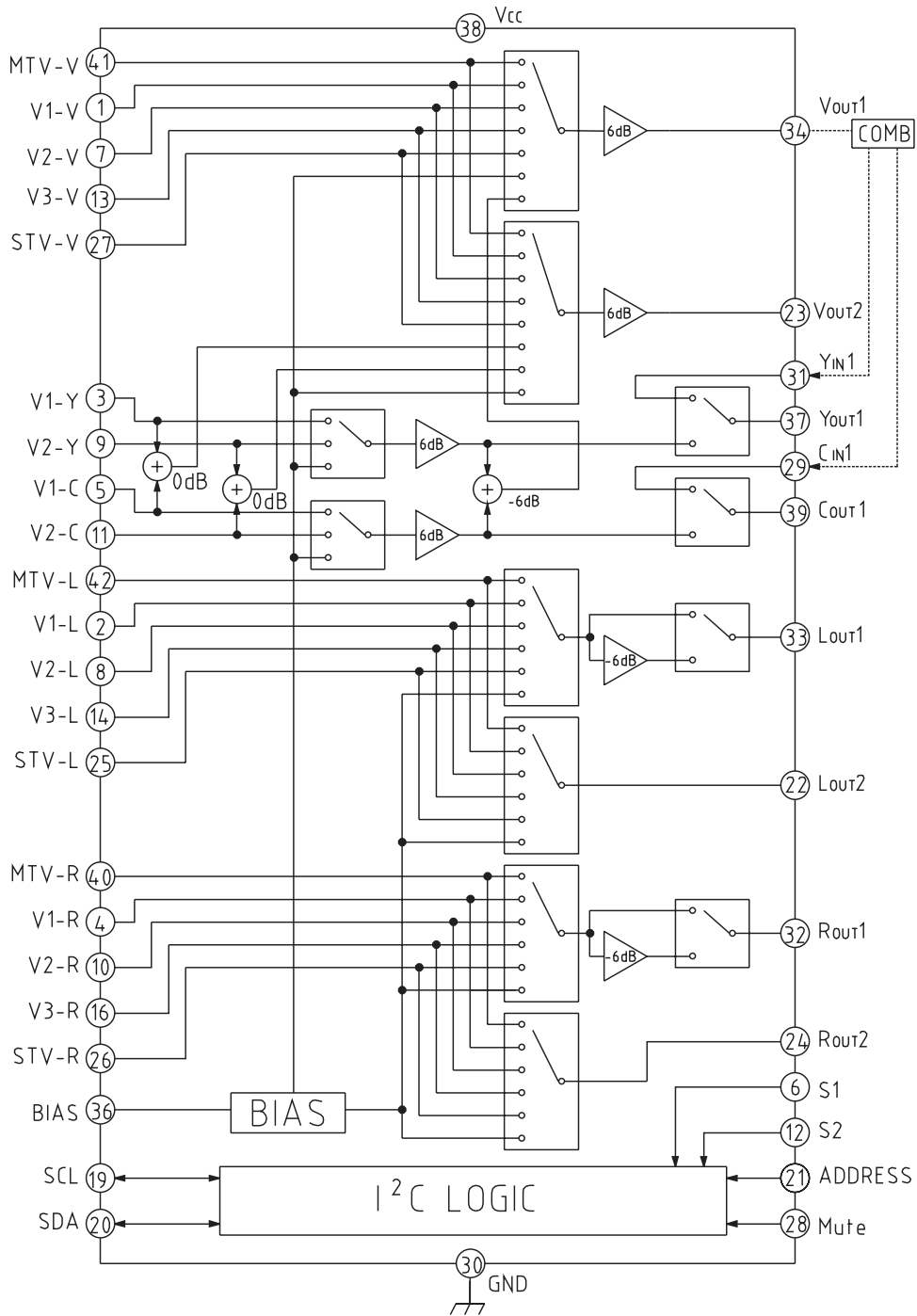
## Package

SDIP-42A (MM1313AD, MM1313BD)

## Applications

1. Televisions
2. Other video equipment

Equivalent Block Diagram



Pin Function

Pin No.	Name	Internal equivalent circuit diagram	Pin No.	Name	Internal equivalent circuit diagram
41 1 7 13 27 3 9 31	MTV-V V1-V V2-V V3-V STV-V V1-Y V2-Y Y <sub>IN1</sub>		33 22 32 24	Lout1 Lout2 Rout1 Rout2	
5 11 29	V1-C V2-C C <sub>IN1</sub>		36	BIAS	
42 2 8 14 25 40 4 10 16 26	MTV-L V1-L V2-L V3-L STV-L MTV-R V1-R V2-R V3-R STV-R		19	SCL	
34 23	Vout1 Vout2		20	SDA	
37 39	Yout1 Cout1		6 12 21 28	S1 S2 ADR Mute	

**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage	V <sub>CC</sub>	12	V
Allowable power dissipation	P <sub>d</sub>	850	mW

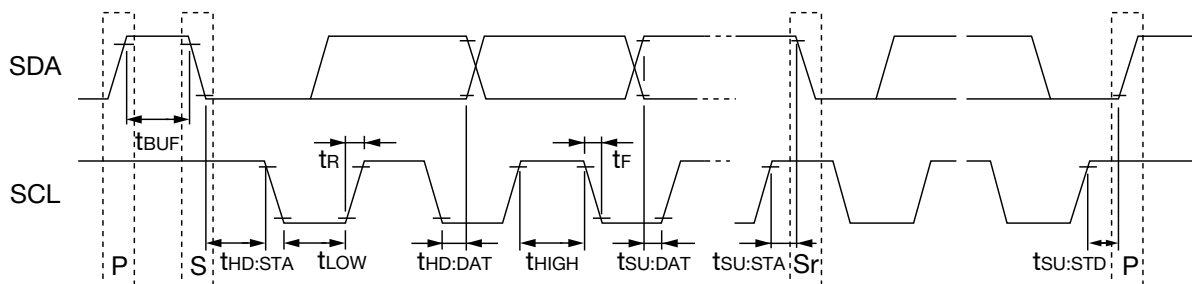
**Electrical Characteristics** (Ta=25°C, V<sub>CC</sub>=9V)

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Operating power supply voltage	V <sub>CC</sub>			8	9	10	V
Current consumption	I <sub>CC</sub>	38	V <sub>CC</sub> =9V, no signal, no load		40	52	mA
<b>V<sub>OUT1</sub> output</b>							
Voltage gain	G <sub>v1</sub>	TP1	Sine wave 1.0V <sub>P-P</sub> , 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F <sub>v1</sub>	TP1	Sine wave 1.0V <sub>P-P</sub> , 10MHz/100kHz	-1.0	0	1.0	dB
Differential gain	DG <sub>v1</sub>	TP1	V <sub>n-V</sub> : Staircase 1V <sub>P-P</sub> APL=10~90%	-3	0	3	%
			V <sub>n-Y</sub> : Staircase (luminance signal) 1V <sub>P-P</sub> V <sub>n-C</sub> : Chroma signal 0.3V <sub>P-P</sub> APL=10~90%				
Differential phase	DP <sub>v1</sub>	TP1	V <sub>n-V</sub> : Staircase 1V <sub>P-P</sub> APL=10~90%	-3	0	3	deg
			V <sub>n-Y</sub> : Staircase (luminance signal) 1V <sub>P-P</sub> V <sub>n-C</sub> : Chroma signal 0.3V <sub>P-P</sub> APL=10~90%				
Input dynamic range	D <sub>v1</sub>	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V <sub>P-P</sub>
<b>V<sub>OUT2</sub> output</b>							
Voltage gain	G <sub>v2</sub>	TP6	Sine wave 1.0V <sub>P-P</sub> , 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F <sub>v2</sub>	TP6	Sine wave 1.0V <sub>P-P</sub> 10MHz/100kHz	-1.0	0	1.0	dB
Differential gain	DG <sub>v2</sub>	TP6	V <sub>n-V</sub> : Staircase 1V <sub>P-P</sub> APL=10~90%	-3	0	3	%
			V <sub>n-Y</sub> : Staircase (luminance signal) 1V <sub>P-P</sub> V <sub>n-C</sub> : Chroma signal 0.3V <sub>P-P</sub> APL=10~90%				
Differential phase	DP <sub>v2</sub>	TP6	V <sub>n-V</sub> : Staircase 1V <sub>P-P</sub> APL=10~90%	-3	0	3	deg
			V <sub>n-Y</sub> : Staircase (luminance signal) 1V <sub>P-P</sub> V <sub>n-C</sub> : Chroma signal 0.3V <sub>P-P</sub> APL=10~90%				
Input dynamic range	D <sub>v2</sub>	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V <sub>P-P</sub>
<b>Y<sub>OUT1</sub> output</b>							
Voltage gain	G <sub>Y1</sub>	TP2	V <sub>n-Y</sub> : Sine wave 1.0V <sub>P-P</sub> , 100kHz	5.5	6.0	6.5	dB
	G <sub>Y2</sub>	TP2	Y <sub>IN1</sub> : Sine wave 2.0V <sub>P-P</sub> , 100kHz	-0.5	0	0.5	
Frequency characteristics	F <sub>Y1</sub>	TP2	V <sub>n-Y</sub> : Sine wave 1.0V <sub>P-P</sub> 10MHz/100kHz	-1.0	0	1.0	dB
	F <sub>Y2</sub>	TP2	Y <sub>IN1</sub> : Staircase 2.0V <sub>P-P</sub> 10MHz/100kHz	-1.0	0	1.0	
Differential gain	DG <sub>Y</sub>	TP2	V <sub>n-Y</sub> : Staircase 1V <sub>P-P</sub> APL=10~90%	-3	0	3	%
			Y <sub>IN1</sub> : Staircase 2V <sub>P-P</sub> APL=10~90%				
Differential phase	DP <sub>Y</sub>	TP2	V <sub>n-Y</sub> : Staircase 1V <sub>P-P</sub> APL=10~90%	-3	0	3	deg
			Y <sub>IN1</sub> : Staircase 2V <sub>P-P</sub> APL=10~90%				

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Input dynamic range	D <sub>v1</sub>	SG2	V <sub>n-Y</sub> : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V <sub>P-P</sub>
	D <sub>v2</sub>	SG4	V <sub>IN1</sub> : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	3.2	3.8		
Output impedance	Z <sub>oYC1</sub>				50		Ω
<b>C<sub>OUT1</sub> output</b>							
Voltage gain	G <sub>c1</sub>	TP3	V <sub>n-C</sub> : Sine wave 1.0V <sub>P-P</sub> , 100kHz	5.5	6.0	6.5	dB
	G <sub>c2</sub>	TP3	C <sub>IN1</sub> : Sine wave 2.0V <sub>P-P</sub> , 100kHz	-0.5	0	0.5	
Frequency characteristics	F <sub>c1</sub>	TP3	V <sub>n-C</sub> : Sine wave 1.0V <sub>P-P</sub> 10MHz/100kHz	-1.0	0	1.0	dB
	F <sub>c2</sub>	TP3	C <sub>IN1</sub> : Sine wave 2.0V <sub>P-P</sub> 10MHz/100kHz	-1.0	0	1.0	
Differential gain	DG <sub>c</sub>	TP3	C <sub>IN1</sub> : Staircase 2V <sub>P-P</sub> APL=10-90%	-3	0	3	%
Differential phase	DP <sub>c</sub>	TP3	C <sub>IN1</sub> : Staircase 2V <sub>P-P</sub> APL=10-90%	-3	0	3	deg
Input dynamic range	D <sub>c1</sub>	SG3	V <sub>n-C</sub> : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	2.75	3.25		V <sub>P-P</sub>
	D <sub>c2</sub>	SG5	C <sub>IN1</sub> : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	5.5	6.5		
Input impedance	Z <sub>ic</sub>		V <sub>n-C</sub> , C <sub>IN1</sub>	10	15	20	kΩ
Output impedance	Z <sub>oc1</sub>				50		Ω
<b>L<sub>OUT1</sub> output</b>							
Voltage gain	GL11	TP4	b <sub>7</sub> =0, Sine wave 2.5V <sub>P-P</sub> , 1kHz	-6.5	-6.0	-5.5	dB
	GL12	TP4	b <sub>7</sub> =1, Sine wave 2.5V <sub>P-P</sub> , 1kHz	-0.5	0.0	0.5	
Frequency characteristics	FL1	TP4	Sine wave 2.5V <sub>P-P</sub> , 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THDL1	TP4	Sine wave 2.5V <sub>P-P</sub> , 1kHz		0.03	0.1	%
Input dynamic range	DL1	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFL1</sub>	33	L <sub>OUT1</sub> pin DC difference during SW switching		0	±15	mV
Input impedance	Z <sub>IL1</sub>			42	60	78	kΩ
Output impedance	Z <sub>OL1</sub>				120		Ω
<b>L<sub>OUT2</sub> output</b>							
Voltage gain	GL2	TP7	Sine wave 2.5V <sub>P-P</sub> , 1kHz	-0.5	0.0	0.5	dB
Frequency characteristics	FL2	TP7	Sine wave 2.5V <sub>P-P</sub> , 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THDL2	TP7	Sine wave 2.5V <sub>P-P</sub> , 1kHz		0.03	0.1	%
Input dynamic range	DL2	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFL2</sub>	22	L <sub>OUT2</sub> pin DC difference during SW switching		0	±15	mV
Output impedance	Z <sub>OL2</sub>				120		Ω
<b>R<sub>OUT1</sub> output</b>							
Voltage gain	GR11	TP5	b <sub>7</sub> =0, Sine wave 2.5V <sub>P-P</sub> , 1kHz	-6.5	-6.0	-5.5	dB
	GR12	TP5	b <sub>7</sub> =1, Sine wave 2.5V <sub>P-P</sub> , 1kHz	-0.5	0.0	0.5	
Frequency characteristics	FR1	TP5	Sine wave 2.5V <sub>P-P</sub> , 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THDR1	TP5	Sine wave 2.5V <sub>P-P</sub> , 1kHz		0.03	0.1	%
Input dynamic range	DR1	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFR1</sub>	32	R <sub>OUT1</sub> pin DC difference during SW switching		0	±15	mV
Input impedance	Z <sub>IR1</sub>			42	60	78	kΩ
Output impedance	Z <sub>OR1</sub>				120		Ω

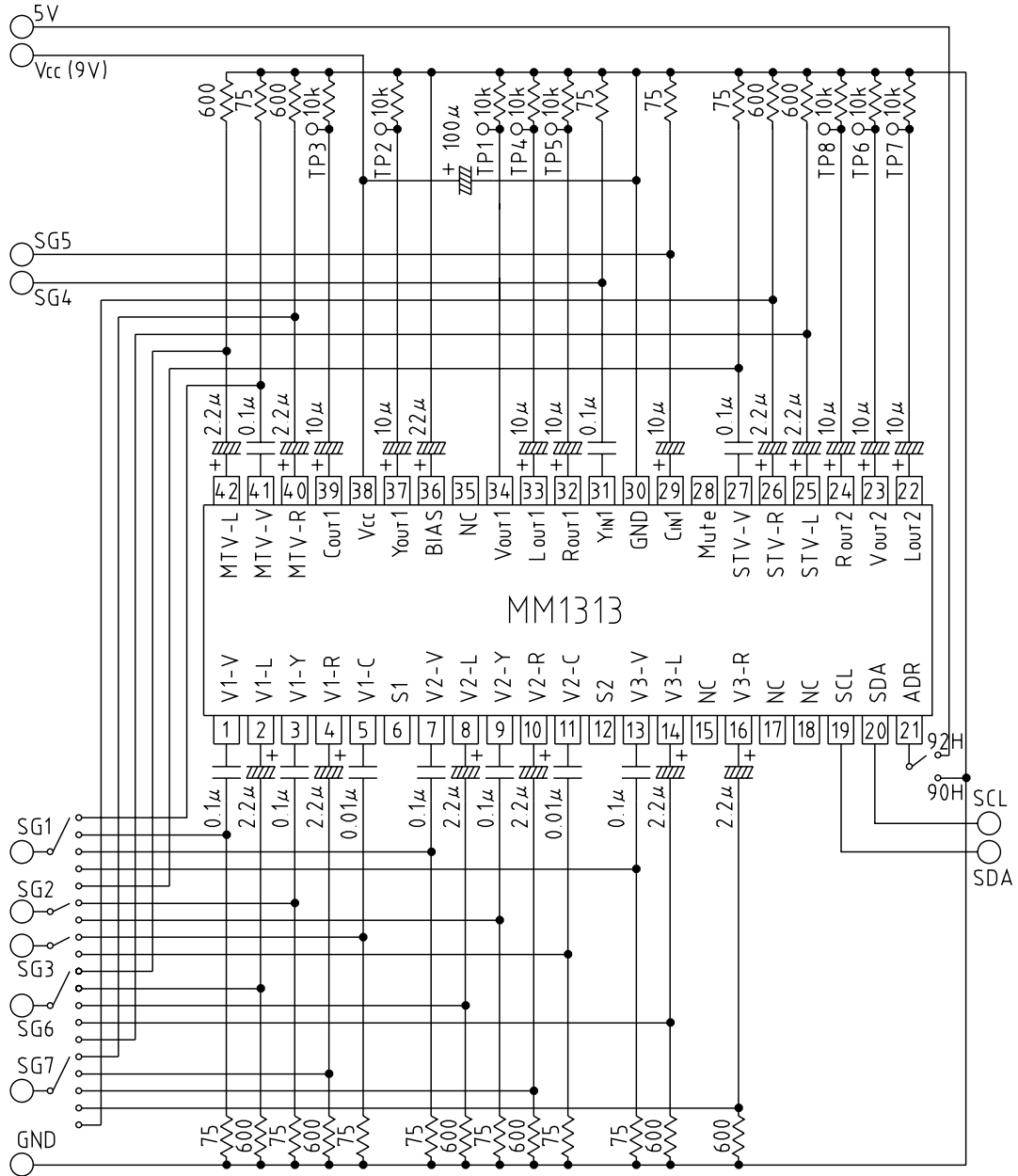
Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
<b>R<sub>OUT2</sub> output</b>							
Voltage gain	G <sub>R2</sub>	TP8	Sine wave 2.5V <sub>P-P</sub> , 1kHz	-0.5	0.0	0.5	dB
Frequency characteristics	F <sub>R2</sub>	TP8	Sine wave 2.5V <sub>P-P</sub> , 1MHz/1kHz	-3.0	0	1.0	dB
Total higher harmonic distortion	THD <sub>R2</sub>	TP8	Sine wave 2.5V <sub>P-P</sub> , 1kHz		0.03	0.1	%
Input dynamic range	D <sub>R2</sub>	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFR2</sub>	24	R <sub>OUT2</sub> pin DC difference during switching		0	±15	mV
Output impedance	Z <sub>OR2</sub>				120		Ω
<b>Crosswalk</b>							
V <sub>OUT 1</sub>	C <sub>TV1</sub>	TP1	Measurement Circuit Figure 2 for SG1 input : 4.43MHz, 1V <sub>P-P</sub> for SG2 input : 4.43MHz, 0.5V <sub>P-P</sub>		-60	-53	dB
V <sub>OUT 2</sub>	C <sub>TV2</sub>	TP2			-60	-53	dB
Y <sub>OUT 1</sub>	C <sub>TY1</sub>	TP3			-60	-53	dB
C <sub>OUT 1</sub>	C <sub>TC1</sub>	TP6			-60	-53	dB
L <sub>OUT 1</sub>	C <sub>TL1</sub>	TP4	Measurement Circuit Figure 2 1kHz, 2.5V <sub>P-P</sub>		-90	-80	dB
L <sub>OUT 2</sub>	C <sub>TL2</sub>	TP5			-90	-80	dB
R <sub>OUT 1</sub>	C <sub>TR1</sub>	TP7			-90	-80	dB
R <sub>OUT 2</sub>	C <sub>TR2</sub>	TP8			-90	-80	dB
<b>Video I/O Pin Voltage</b>							
Input pin voltage	V <sub>VIP</sub>		No signal, no load	4.6	4.9	5.2	V
Output pin voltage	V <sub>VOP</sub>		V <sub>OUT1</sub> pin, V <sub>OUT2</sub> pin No signal, no load	4.1	4.4	4.7	V
	V <sub>SOP</sub>		Y <sub>OUT1</sub> pin, C <sub>OUT1</sub> pin No signal, no load	3.3	3.6	3.9	V
<b>Audio I/O Pin Voltage</b>							
Input pin voltage	V <sub>AIP</sub>		No signal, no load	4.0	4.3	4.6	V
Output pin voltage	V <sub>AOP</sub>		No signal, no load	3.9	4.2	4.5	V
<b>Logic section (Refer to figure below)</b>							
Input voltage L	V <sub>IL</sub>		I <sup>2</sup> C logic low level discrimination value	0.0		1.5	V
Input voltage H	V <sub>IH</sub>		I <sup>2</sup> C logic high level discrimination value	3.0		5.0	V
Low level output voltage (SDA)	V <sub>OL</sub>		SDA for 3mA inflow	0.0		0.4	V
High level input current	I <sub>IH</sub>		when SDA, SCL=4.5V impressed	-10		+10	μA
Low level input current	I <sub>IL</sub>		when SDA, SCL=0.4V impressed	-10		+10	μA
Clock frequency	f <sub>SCL</sub>					100	kHz
Data transmission waiting time	t <sub>BUF</sub>			4.7			μS
SCL start hold time	t <sub>HD;STA</sub>			4.0			μS
SCL low level hold time	t <sub>LOW</sub>			4.7			μS
SCL high level hold time	t <sub>HIGH</sub>			4.0			μS
SCL start set-up time	t <sub>SU;STA</sub>			4.7			μS
SDA data hold time	t <sub>HD;DAT</sub>			200			nS
SDA data set-up time	t <sub>SD;DAT</sub>			250			nS
SCL rise time	t <sub>r</sub>					1000	nS
SCL fall time	t <sub>f</sub>					300	nS
SCL stop set-up time	t <sub>SU;STO</sub>			4.0			μS

I<sup>2</sup>C BUS BUS Control Signal

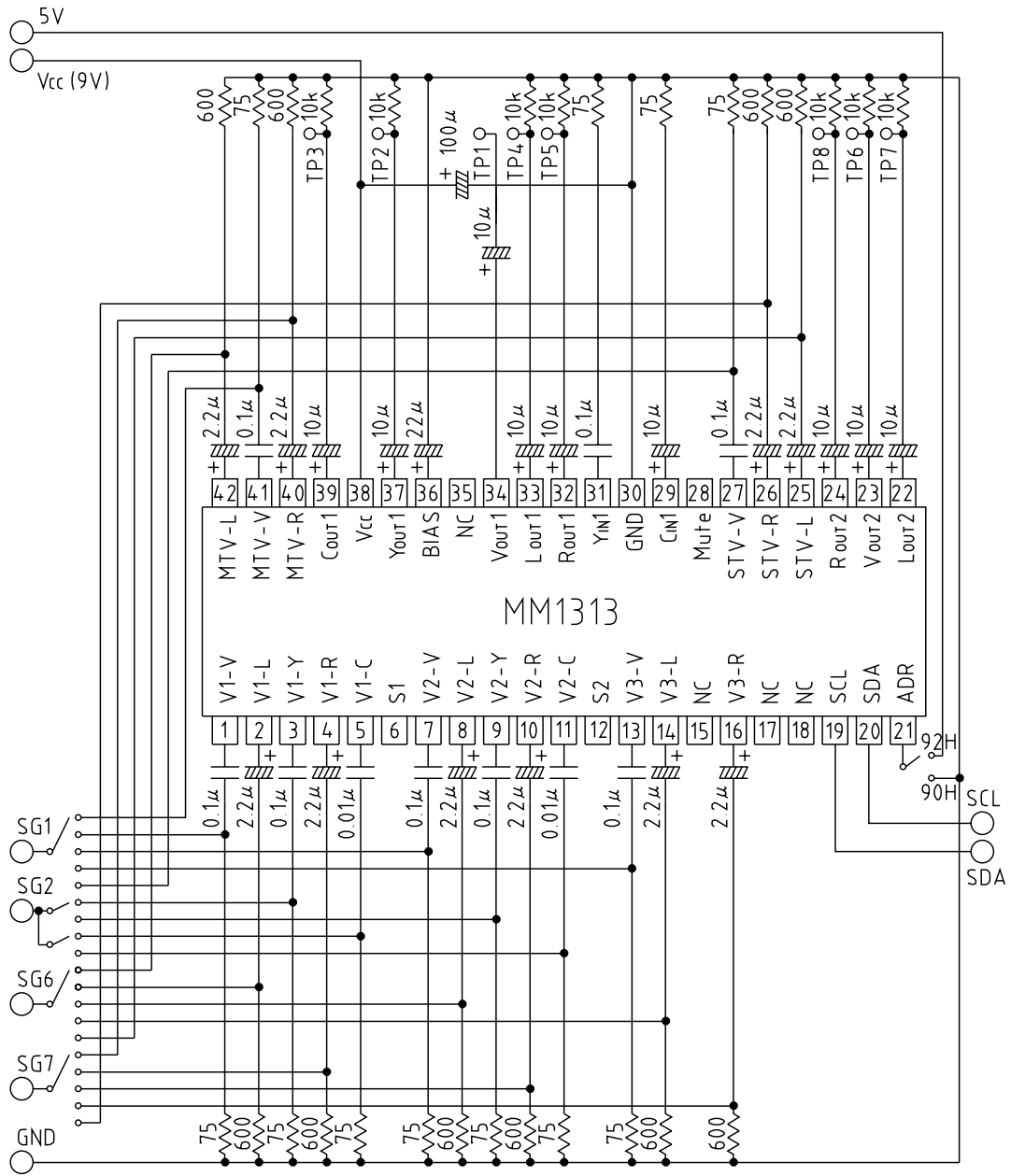


Measurement Circuit

Measurement Circuit 1

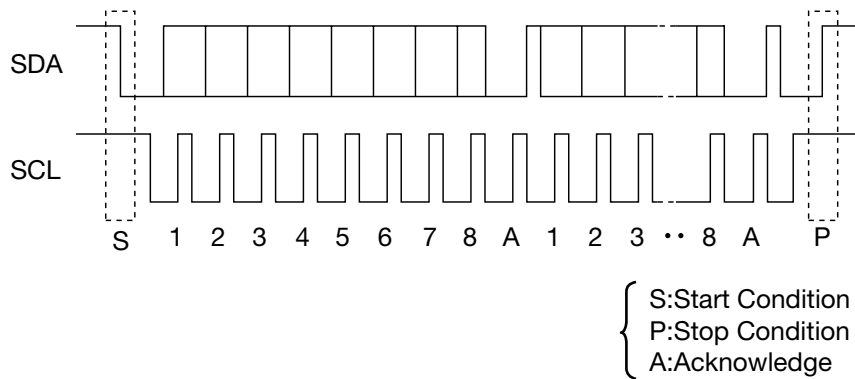


■ Measurement Circuit 2 (Crosstalk measurement)





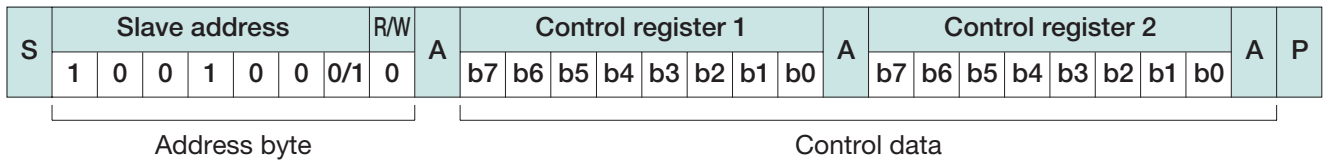
I<sup>2</sup>C BUS



The I<sup>2</sup>C BUS is a BUS system developed by Philips for internal use in equipment. Data transmission is carried out by the two SDA and SCL lines, in byte units, with the MSB first from start condition.

[Control Register]

The control register contains data sent from the master in order to determine the status of each switch.



The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 0 when using as a control register.

The MM1313 slave address can be selected as 90H/92H depending on the status of the ADR pin. When ADR pin is low it is 90H.

The relationship between the control register bits and switch control is as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
Audio	S/Comp	Video-Select			Audio-Select		
Gain	Select						

The control register bits are reset to 0 when power is applied.

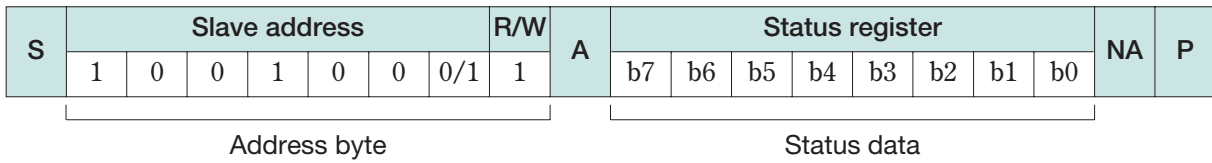
MM1313 control is carried out by the 3-byte structure of the 1 address byte and 2 control data bytes. The first byte in the control data is control data for output 1, and the remaining 1 byte is control data for output 2.

All of the remaining data (fourth byte and after) are ignored.

Refer to the separate tables for details on switch control.

**[Status Register]**

The status register contains data for sending device status to the master.



The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 1 when using as a status register.

The MM1313 slave address can be selected as 91H/93H depending on the status of the ADR pin. When the ADR pin is low it is 91H. However, the confirmation response after completion of the status register should be non-acknowledge.

The status register output data as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

- P-ON RESET : Returns 1 for power on reset. However once data read begins, 0 is returned next.
- S1/S2 OPEN : Returns 0 when the S1/S2 pin is not open, and returns 1 when the S1/S2 pin is open
- S1/S2 SEL : Returns 0 when the S1/S2 pin is not grounded, and returns 1 when the S1/S2 pin is grounded.

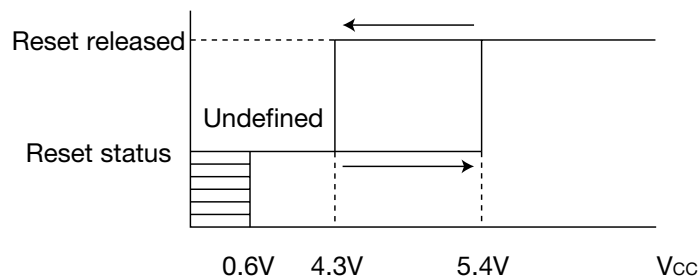
S1/S2 OPEN, SEL have 3-value discrimination, and the combinations are as shown below.

S1/S2 pin DC voltage	S1/S2 OPEN	S1/S2 SEL
0.8V or less	0	1
1.3V or more, 3.5V or less	0	0
4.5V or more	1	0

**[Power On Reset]**

Power on reset is built in to reset each control register to 0 when power is turned on.

Power on reset threshold has hysteresis as shown in the figure below. The IC power on reset status can be discriminated by reading the status register P-ON RESET.



**Switch Control Table**

**1. Video Output 1**

b6	b5	b4	b3	Vout1	Yout1	Cout1
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV-V	YIN1	CIN1
0	0	1	0	V1-V	YIN1	CIN1
0	0	1	1	V2-V	YIN1	CIN1
0	1	0	0	V3-V	YIN1	CIN1
0	1	0	1	STV-V	YIN1	CIN1
0	1	1	0	Mute	Mute	Mute
		1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV-V	YIN1	CIN1
1	0	1	0	V1-Y+C	V1-Y	V1-C
1	0	1	1	V2-Y+C	V2-Y	V2-C
1	1	0	0	V3-V	YIN1	CIN1
1	1	0	1	STV-V	YIN1	CIN1
1	1	1	0	Mute	Mute	Mute
		1	1			

**2. Video Output 2**

b6	b5	b4	b3	Vout2
0	0	0	0	Mute
0	0	0	1	MTV-V
0	0	1	0	V1-V
0	0	1	1	V2-V
0	1	0	0	V3-V
0	1	0	1	STV-V
0	1	1	0	Mute
		1	1	
1	0	0	0	Mute
1	0	0	1	MTV-V
1	0	1	0	V1-Y+C
1	0	1	1	V2-Y+C
1	1	0	0	V3-V
1	1	0	1	STV-V
1	1	1	0	Mute
		1	1	

**3. Audio Output 1**

Mute pin	b2	b1	b0	Lout1	Rout1
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV-L	MTV-R
	0	1	0	V1-L	V1-R
	0	1	1	V2-L	V2-R
	1	0	0	V3-L	V3-R
	1	0	1	STV-L	STV-R
	1	1	0	Mute	Mute
	1	1			
3.0V or more	-	-	-	Mute	Mute

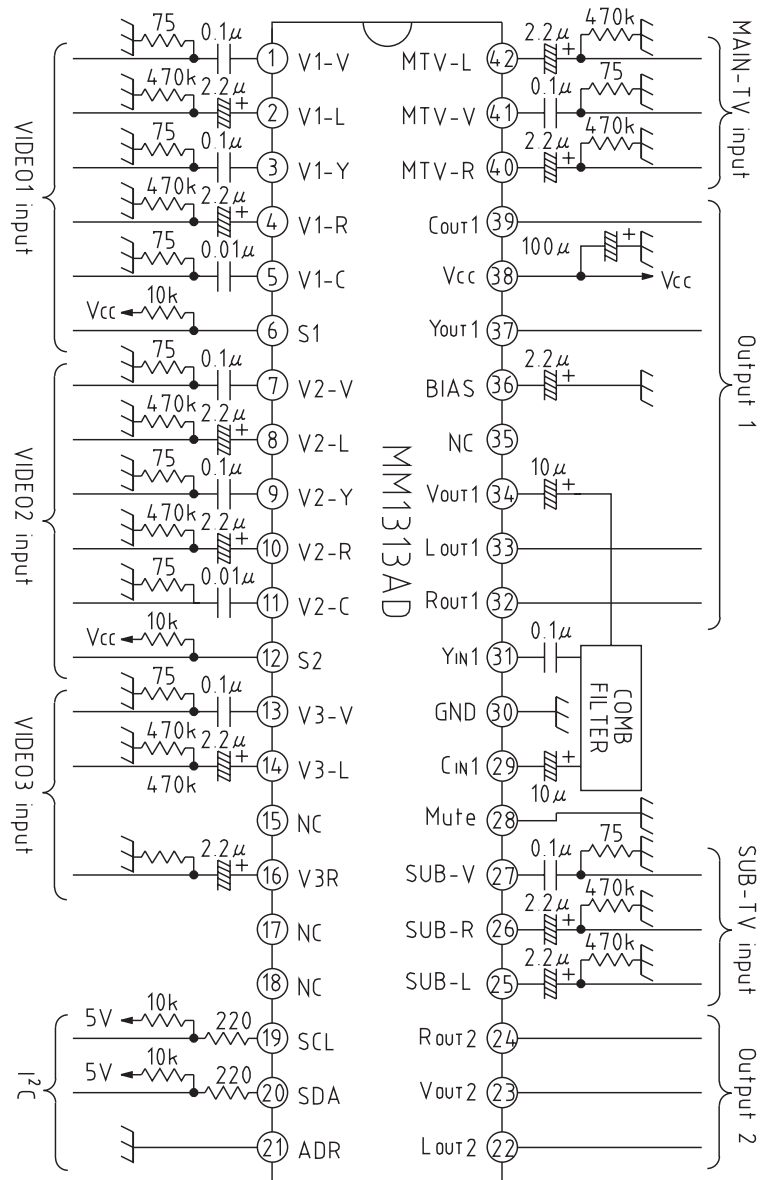
**4. Audio Output 1 Gain Switching**

b7	Output gain
0	-6dB output
1	0dB output

**5. Audio Output 2**

Mute pin	b2	b1	b0	Lout2	Rout2
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV-L	MTV-R
	0	1	0	V1-L	V1-R
	0	1	1	V2-L	V2-R
	1	0	0	V3-L	V3-R
	1	0	1	STV-L	STV-R
	1	1	0	Mute	Mute
	1	1			
3.0V or more	-	-	-	Mute	Mute

Application Circuit



Notes

1. V<sub>OUT</sub> is set at 4.4V and C<sub>IN</sub> at 4.9V

Please note that capacitance polarity may vary depending on comb filter bias.

2. Each audio output can be muted by making pin 19 high. Mute is off when it is open or low.