HD63084

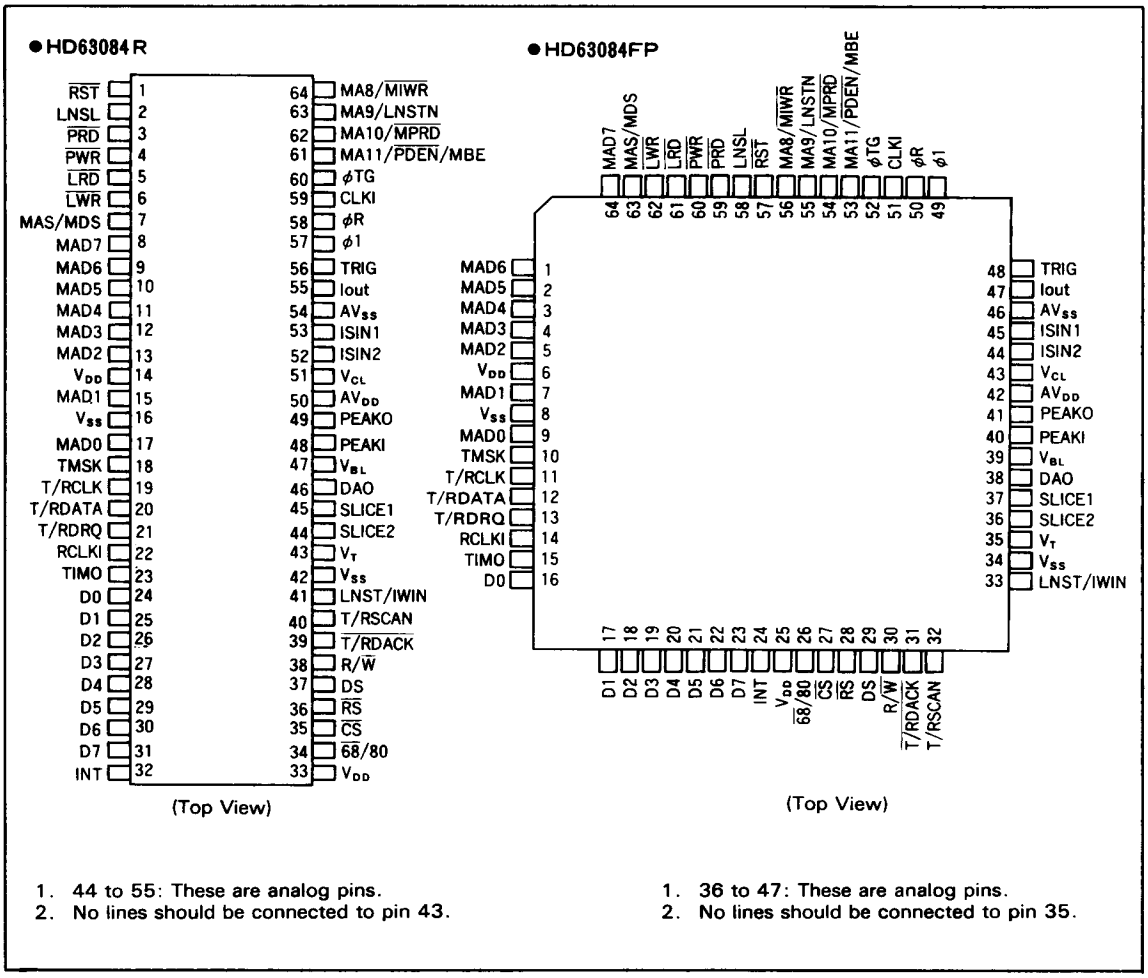
Document Image Pre-Processor (DIPP)

DIPP can read image signals coming from the line sensor of a facsimile apparatus or an image scanner at 5 M pels*/second, and after correcting for optical or shading distortion, converters them into digital signals. Including a peak value detection circuit, a 7-bit A/D and D/A converter for detecting and generating the shading distortion and a 4-bit A/D converter, the DIPP can generate digital image signal with high accurate correction. Also including a sample and hold circuit.

Features

- High speed reading of image signals
  The DIPP can read image signals with a speed of up to 5 M pels per second (when the input clock frequency is 10 MHz). This speed is 5 times faster than that of the VPP.
- Highly accurate processing of image signal
  —The peak to peak voltage of input image signals ranges from 0.1 V to 2 V.
  —The DIPP includes a peak value detection circuit with resolution of 8 bits, 7-bit successive approximation A/D and D/A converters, a 4-bit flash A/D converter, a 4-bit D/A converter and a shading wave RAM to perform highly accurate correction of distortion.
  —The DIPP can perform distortion correction for each pel with a resolution of 1% using an external pel correction RAM.
- Various digitization modes
  The DIPP has three modes to digitize read image data: binary coding, dithered coding and 4-bit coding.
  Binary coding: Converts the read signal to 1 or 0 by using a slice level selected by the user.
  Dithered coding: Generates 16 gradations of dummy halftones by using a 4 × 4 dither pattern specifiifed by the user.
  4-bit coding: Generates 16 gradations of real halftones in the format of 4 bits per pel.
- Wide range of programmable reduction of magnification ratios
  The DIPP can reduce image data in read (T) mode. The reduction ratio is programmable in about 1000 increments from 0.125 to 1.
  The DIPP can magnify image data in receive (R) mode. The magnification ratio is programmable in about 1000 increments from 1 to 8.
- Automatic determination of vertical resolution
  The DIPP counts the amount of changing pels along a scan line or between two scan lines. The result of the counting appears in a flag bit of the internal status register. In response to the status of this flag bit, the user can have the DIPP perform vertical resolution conversion, which allows shortening of the data transmit time.
- Burst DMA transfer of image data
  By using the line memory, the DIPP can transfer a line of digitized data at a stretch in burst DMA mode.
- Internal sensor interface
  The DIPP incorporates a sample and hold circuit which is directly connected to the sensor via coupling capacitor. This LSI also incorporates the sensor timing generator which generates control signals for the sensors.
- Package
  —64 pin plastic shrink DIP (DP-64S)
  —64 pin plastic QFP (FP-64A)

Pin Arrangement



Specifications

Item		Specifications
Input Clock frequency		1 MHz to 10 MHz
Image signal reading frequency (Operating frequency)		500 kHz to 5 MHz
Input image signal Vp-p		0.1 to 2.0 V
Shading distortion correcting range		70% of signal peak
Scan line length		64 to 8191 pels
Sensor driving cycle		8231 clocks per image signal clock
Half tone		16 gradations
Dithered pattern		4 × 4 dithered matrix
Horizontal resolution conversion (reduction & magnification)		0.125 to 8.00 times
Maximum DMA data transfer speed		System bus ..... 0.625 M Byte/sec Memory bus ..... 5 M Byte/sec
Serial data transfer speed		5 M-bit/sec
Interruption of MPU		· At completion of writing the shading waveform detection period · At completion of reading a scan line of image data to the external line memory
Supply voltage		5 V ± 5%
Power consumption		300 mW (Max)
Package	HD63084R	DP-64S
	HD63084FP	FP-64A

Function of DIPP

CCD image sensor or other optical sensing devices used in the image reading block of facsimiles generate shading distortion of data. The DIPP is used to solve this problem.

During reading of image data (that is, in read (T) mode), this LSI takes analog image data via a sensing device, corrects distortion included in the data, digitizes the corrected data, and then transfers the digitized data to the MPU system. The digitized data can be reduced before transferring the data to the MPU system.

When receiving image data via MODEM (that is, in receive (R) mode), the DIPP can also perform transfer of data from the MPU system to the recorder. The data can be magnified before being transferred.

The DIPP performs the above functions in response to the user's program.

Figure 1 shows the functions of the DIPP.

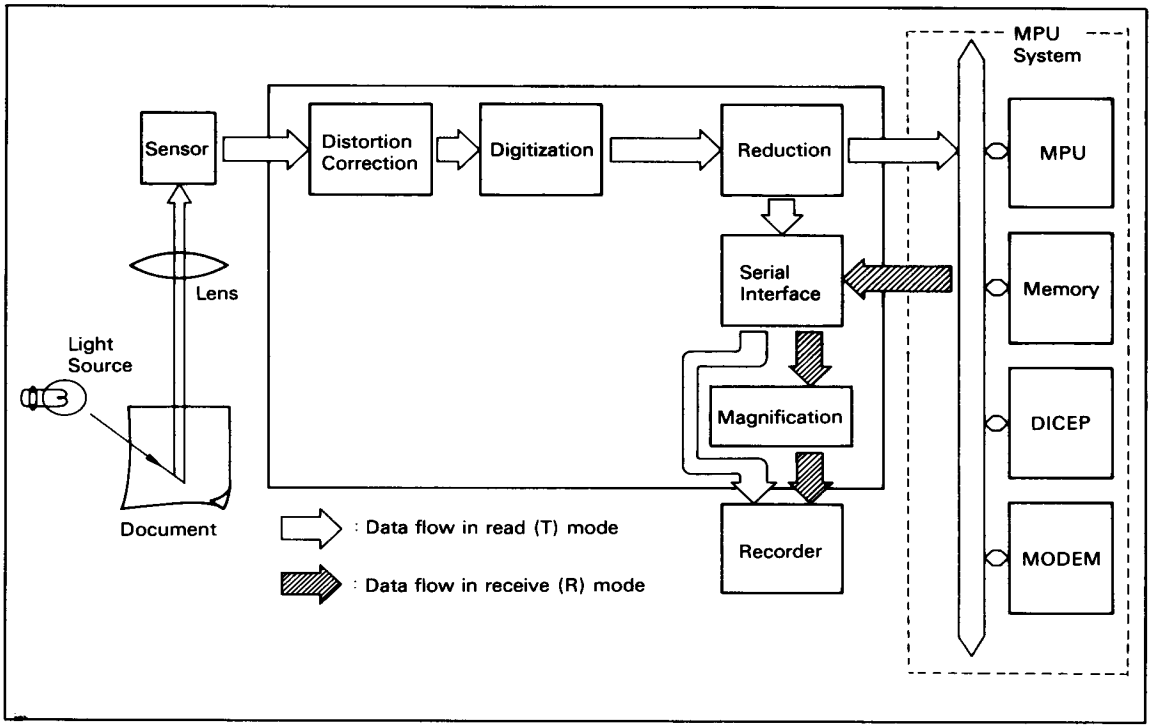


Figure 1 DIPP Function

Registers

The DIPP contains an address register (AR), status register (SR), control registers (R01 to R1D) and DMA registers. All of these registers except for the DMA registers can be accessed by the MPU. The DIPP operates depending on the contents of these registers.

Reg. No.	$\overline{CS}$	$\overline{RS}$	Address Register 4	3	2	1	0	Name	R/W
—	0	0	—	—	—	—	—	Address Register	W
R00	0	1	0	0	0	0	0	Mode Select Register	R/W
R01	0	1	0	0	0	0	1	Work Enable Register	R/W
R02	0	1	0	0	0	1	0	SENS Starting Register	W
R03	0	1	0	0	0	1	1	SENS Ending Register	W
R04	0	1	0	0	1	0	0	IWIN Starting Register (H)	W
R05	0	1	0	0	1	0	1	IWIN Starting Register (L)	W
R06	0	1	0	0	1	1	0	PAPW Starting Register	W
R07	0	1	0	0	1	1	1	PAPW Ending Register	W
R08	0	1	0	1	0	0	0	Resolution Determination Register	W
R09	0	1	0	1	0	0	1	Resolution Determination/Sensor Type Register	W
R0A	0	1	0	1	0	1	0	Peak Value Limit Register	W
R0B	0	1	0	1	0	1	1	Slice Level Setting Register	W
R0C	0	1	0	1	1	0	0	γCorrection Resolution Register	W
R0D	0	1	0	1	1	0	1	m and k Parameter Register	W
R0E	0	1	0	1	1	1	0	l-Parameter Register (1)	W
R0F	0	1	0	1	1	1	1	l-Parameter Register (2)	W
R10	0	1	1	0	0	0	0	Dither Register (1)	R/W
R11	0	1	1	0	0	0	1	Dither Register (2)	R/W
R12	0	1	1	0	0	1	0	Dither Register (3)	R/W
R13	0	1	1	0	0	1	1	Dither Register (4)	R/W
R14	0	1	1	0	1	0	0	Dither Register (5)	R/W
R15	0	1	1	0	1	0	1	Dither Register (6)	R/W
R16	0	1	1	0	1	1	0	Dither Register (7)	R/W
R17	0	1	1	0	1	1	1	Dither Register (8)	R/W
R18	0	1	1	1	0	0	0	Horizontal Resolution Conversion Logic Register	W
R19	0	1	1	1	0	0	1	IWIN Ending Register (H)	W
R1A	0	1	1	1	0	1	0	IWIN Ending Register (L)	W
R1B	0	1	1	1	0	1	1	Peak Value Register	R/W
R1C	0	1	1	1	1	0	0	Initial Value Register	R
R1D	0	1	1	1	1	0	1	Shading Waveform Register	R/W
—	0	0	—	—	—	—	—	Status Register	R
—	1	—	—	—	—	—	—	DMA Read Register	*1
—	1	—	—	—	—	—	—	DMA Write Register	*1

*1: These registers are accessed by DMAC in cycle stealing DMA mode.

Absolute Maximum Rating

Internal Digital Circuits (Voltages referenced to V_{SS} = 0 V. Ta = 25°C)

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage (Digital Input Pins)	V_I	−0.3 to V_{DD}+0.3	V
Input Voltage (Digital I/O Pins)	V_{IT}	−0.3 to V_{DD}+0.3	V

Internal Analog Circuits (Voltages referenced to AV_{SS} = 0 V. Ta = 25°C)

Item	Symbol	Value	Unit
Supply Voltage	AV_{DD}	−0.3 to +7.0	V
Reference Voltage	$V_{2.5}$ V_{CL} V_{BL}	−0.3 to AV_{DD}+0.3	V
Input Voltage (Analog Input Pins)	V_{IA}	−0.3 to AV_{DD}+0.3	V

Common Characteristics between Digital and Analog Circuits

Item	Symbol	Value	Unit
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Power Consumption *1	Pc	500	mW

*1) Ta = 25°C

System Configuration

The following paragraphs provide a description of the pin functions.