Read Data

A set of nine (9) byte words are required to place the FDC37C65C+ into the Read Data Mode. After the Read Data command has been issued, the FDC37C65C+ loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC37C65C+ outputs data (from the data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation". The Read Data Command may be terminated by the receipt of a Terminal count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC37C65C+ stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then, at the end of the sector, terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC37C65C+ depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 16 shows the Transfer Capacity.

Table 16 - Transfer Capacity

MULTI-TRACK MT	MFM/FM MF	BYTES/ SECTOR N	MAXIMUM TRANSFER CAPACITY (Bytes/Sector) X (Number of Sectors)	FINAL SECTOR READ FROM DISKETTE
0	0	00	(128) x (26) = 3,328	26 at Side 0
0	1	01	(256) x (26) = 6,656	or 26 at Side 1
1	0	00	(128) x (52) = 6,656	26 at Side 1
1	1	01	(256) x (52) = 13,312	
0	0	01	(256) x (15) = 3,840	15 at Side 0
0	1	02	(512) x (15) = 7,680	or 15 at Side 1
1	0	01	(256) x (30) = 7,680	15 at Side 1
1	1	02	(512) x (30) = 15,360	
0	0	02	(512) x (8) = 4,096	8 at Side 0
0	1	03	(1024) x (8) = 8,192	or 8 at Side 1
1	0	02	(512) x (16) = 8,192	8 at Side 1
1	1	03	(1024) x (16) = 16,384	

The "multi-track" function (MT) allows the FDC37C65C+ to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector L, Side 0 and completing at Sector L, Side 1 (Sector L is the last sector on the side). Please note that this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC37C65C+ must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC37C65C+ reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexadecimal.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC37C65C+ detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC37C65C+ sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively. After reading the ID and Data Fields in each sector, the FDC37C65C+ checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC37C65C+ sets the DC (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC37C65C+ also sets the DD (Data Error in Data field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

If the FDC37C65C+ reads a Deleted Data Address Mark from the diskette, and the SK bit (bit D5 in the first Command Word is not set (SK = 0) then the FDC37C65C+ sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC37C65C+ skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC37C65C+ and the processor, via the data bus the FDC37C65C+ must be serviced within the time calculated using the equation shown in the section "Format Control Register", or the FDC37C65C+ sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 17 shows the value for C, H, R, and N, when the processor terminates the Command.

Table 17 - ID Information in Processor - Terminated Command

MT	HD	FINAL SECTOR TRANSFERRED TO PROCESSOR	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

NOTES: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes are required to set the FDC37C65C+ into the Write Data mode. After the Write Data command has been issued, the FDC37C65C+ loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the specify command), and begins reading ID Fields. When all four bytes loaded during the Command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC37C65C+ takes data from the processor byte-by-byte via the data bus, and outputs it to the drive.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written. The FDC37C65C+ continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC37C65C+, it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with 00 (zeros).

The FDC37C65C+ reads the ID field of each sector and checks the CRC bytes. If the FDC37C65C+ detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this, the FDC37C65C+ sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. Status register 0 also has bit 7 and 6 set to 0 and 1 respectively.

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC37C65C+ detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, the FDC37C65C+ skips the sector with the Data Address Mark and reads the next sector.

Read a Track

This command is similar to the READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC37C65C+ starts reading all data fields on the track, as continuous blocks of data. If the FDC37C65C+ finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC37C65C+ compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC37C65C+ does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC37C65C+ stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette before the INDEX HOLE is encountered for the second time, the MA (Missing Address Mark) flag in Status Register 1 is set to a "1" (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a "1" (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to "0" and "1" respectively. During this command there is no data transfer between FDC37C65C+ and the CPU except during the result phase.

Format a Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette. Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; four data requests per sector are

made by the FDC37C65C+ for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC37C65C+ for each sector on the track. If the FDC37C65C+ is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register are incremented by one after each sector is formatted. The R register therefore contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC37C65C+ encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the drive at the end of a write operation, then the FDC37C65C+ sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also, the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 18 shows the relationship between N, SC, GPL for various sector sizes. (See Table 19 for recommended IBM PC and PC/AT compatible programming parameters.)

Table 18

FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2][3]
8" Standard Floppy					
FM Mode	128 Bytes/Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode [4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF

FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2][3]
5¼" Minifloppy					
FM Mode	128 Bytes/Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode [4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	09	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk®					
FM Mode	128 Bytes/Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024[5]	3	05	35	74

NOTES:
(1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
(2) Suggested values of GPL in format command.
(3) All values except sector size and hexadecimal.
(4) In MFM mode FDC37C65C + cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00)
(5) 1 Mbit/s vertical mode.

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC37C65C + compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of:

$$D_{FDD} = D_{PROCESSOR}, D_{FDD} \leq D_{PROCESSOR}, \text{ or}$$

$$D_{FDD} \geq D_{PROCESSOR}$$

The hexadecimal byte of FF either from memory or from the drive can be used as a mask byte because it always meets the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur:

1. The conditions for scan are met (equal, low, or high), or,
2. The last sector on the track is reached (EOT), or
3. The terminal count signal is received.

If the conditions for scan are met, then the FDC37C65C+ sets the SH (Scan Hit) flag of Status Register 2 to a "1" (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC37C65C+ sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC37C65C+ to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 19 shows the status of bits SH and SN under various conditions of SCAN.

Table 19

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 (SN)	BIT 3 (SH)	
Scan Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	1	0	$D_{FDD} \neq D_{PROCESSOR}$
Scan Low or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} < D_{PROCESSOR}$
	1	0	$D_{FDD} > D_{PROCESSOR}$
Scan High or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} > D_{PROCESSOR}$
	1	0	$D_{FDD} < D_{PROCESSOR}$

If the FDC37C65C+ encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC37C65C+ skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC37C65C+ sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read, or the MT (Multi-Track) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21, the following will

happen: Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped, and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC37C65C+ ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the drive is moved from cylinder to cylinder under control of the Seek Command. FDC37C65C+ has four independent Present Cylinder Registers for each drive. They are clear only after the Recalibrate command. The FDC37C65C+ compares the PCN (Present Cylinder Number), which is the current head position, with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to drive set to a 1 (high),and Step Pulses are issued (Step In).

PCN > NCN: Direction signal to drive set to a 0 (low), and Step Pulses are issued (Step Out).

The rate at which Step Pulses are issued is controlled by the SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued, NCN is compared against PCN; when NCN = PCN, the SE (Seek End) flag in Status Register 0 is set to a 1 (high), and the command is terminated. At this point the FDC37C65C+ interrupt goes high. Bits DB0 - DB3 in the Main Status Register are set during the seek operation and are cleared by the Sense Interrupt Status Command.

During the Command Phase of the Seek operation, the FDC37C65C+ is in the FDC37C65C+ BUSY state, but during the Execution Phase it is in the NON-BUSY state. While the FDC37C65C+ is in the NON BUSY state, another seek Command may be issued, and in this manner parallel Seek Operations may be performed on up to 4 Drives at once. No other command can be issued for as long as the FDC37C65C+ is in process of sending Step Pulses to any drive.

If a drive is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between the first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the drive to the Track 0 position. The FDC37C65C+ clears the contents of the PCN counter, and checks the status of the Track 0 signal from the drive. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 255 Step Pulses have been issued, the FDC37C65C+ sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1's

(highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to overlap RECALIBRATE Commands to multiple drives and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal will be generated by the FDC37C65C + for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of drive changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in the NON-DMA Mode, DB5 in the Main Status Register is high. Upon entering the Result Phase this bit is cleared.

Reasons 1 and 4 do not require a Sense Interrupt Status command. The interrupt is cleared by reading or writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register, 0 identifies the cause of the interrupt. See Table 20.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Issuing the Sense Interrupt Status Command without an interrupt pending is treated as an invalid command.

Table 20

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms, ... 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between the Head Load signal going high and the Read/Write operation starting. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms,... 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK1 or XTAL1). Times indicated above are for a 16 MHz clock; if the clock is reduced to 8 MHz then the time intervals are increased by a factor of two. If the clock is increased to 32 MHz then all time intervals are decreased by a factor of two.

The choice of DMA or non-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1), the non-DMA mode is selected, and when ND = 0, the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the drives. Status Register 3 contains the Drive Status information stored internally in the FDC37C65C+ registers.

Return Version

The Return Version command identifies the type of chip in use. A value of A0H is returned as the result byte. No interrupts are generated.

Invalid

If an invalid command is sent to the FDC37C65C+ (a command not defined above), then the FDC37C65C+ will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC37C65C+ during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC37C65C+ is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0, it will find an 80 hex indicating an invalid command was received. A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC37C65C+ will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC37C65C+ in a standby or no operation state.

Recording Format

When bit D7 of the Format Control Register is reset to "0", the FDC37C65C+ will default to the standard single density or double density formats as shown below. The FDC37C65C+ will implement the Toshiba Vertical Recording Format when bit D7 of the Format Control Register is set. The vertical recording format will have a gap 2 length of 41 bytes for 1

megabit operation, and a gap 2 length of 22 bytes for 500 kbits/s operation. At 1 Mbps, A FORMAT command will therefore format 41 bytes of gap 2; a READ command for 1 Mbps will skip over 42 bytes before searching for the sync field. The WRITE DATA command will skip 3 bytes after the CRC and will then write 38 bytes of 4E before writing 12 bytes of 00. At 500 kbps, A FORMAT command will therefore format 22 bytes of gap 2; a READ command will skip over 23 bytes before searching for the sync field. The WRITE DATA command will skip 3 bytes after the CRC and will then write 19 bytes of 4E before writing 12 bytes of 00.

FLOPPY DISK FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA	DATA	C	GAP3	GAP 4b
80x	12x			50x	12x			Y	D	E	O	R	22x	12x	AM		R		
4E	00	3x C2	FC	4E	00	3x A1	FE	L		C		C	4E	00	3x A1	FB F8	C		

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	C	H	S	N	C	GAP2	SYNC	DATA	DATA	C	GAP3	GAP 4b
40x	6x		26x	6x		Y	D	E	O	R	11x	6x	AM		R		
FF	00	FC	FF	00	FE	L		C		C	FF	00	FB or F8		C		

TOSHIBA VERTICAL RECORDING FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA	DATA	C	GAP3	GAP 4b
80x	12x			50x	12x			Y	D	E	O	R	41x	12x	AM		R		
4E	00	3x C2	FC	4E	00	3x A1	FE	L		C		C	4E	00	3x A1	FB F8	C		

Table 21 - Comparison: FDC37C65C & FDC37C65C+

FDC37C65C	FDC37C65C+
Max Data Rate: 1 Mbps	Max Data Rate: 1 Mbps
Max Clock: 32 MHz	Max Clock: 32 MHz
Power Down Mode	Power Down Mode
Recalibrate (Restore) Command will issue up to 77 pulses	Recalibrate Command will issue up to 255 step pulses
Longitudinal Recording only	Vertical or Longitudinal recording
No FIFO	FIFO included
Return Version = 90H	Return Version = A0H
	Requires Verify bit