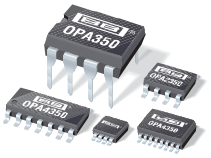


SBOS099C − SEPTEMBER 2000 − REVISED JANUARY 2005

High-Speed, Single-Supply, Rail-to-Rail OPERATIONAL AMPLIFIERS

*Micro*Amplifier™ Series

FEATURES

- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 10mV)
- WIDE BANDWIDTH: 38MHz
- HIGH SLEW RATE: 22V/μs
- LOW NOISE: 5nV/√Hz
- LOW THD+NOISE: 0.0006%
- UNITY-GAIN STABLE
- *Micro*SIZE PACKAGES
- SINGLE, DUAL, AND QUAD

APPLICATIONS

- CELL PHONE PA CONTROL LOOPS
- DRIVING A/D CONVERTERS
- VIDEO PROCESSING
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- COMMUNICATIONS
- ACTIVE FILTERS
- TEST EQUIPMENT

DESCRIPTION

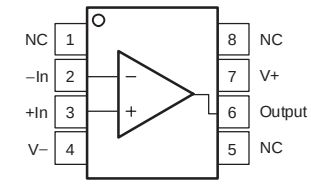
The OPA350 series rail-to-rail CMOS operational amplifiers are optimized for low voltage, single-supply operation. Rail-to-rail input/output, low noise (5nV/√Hz), and high speed operation (38MHz, 22V/μs) make them ideal for driving sampling Analog-to-Digital (A/D) converters. They are also well suited for cell phone PA control loops and video processing (75Ω drive capability) as well as audio and general purpose applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

The OPA350 series operates on a single supply as low as 2.5V with an input common-mode voltage range that extends 300mV below ground and 300mV above the positive supply. Output voltage swing is to within 10mV of the supply rails with a 10kΩ load. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

The single (OPA350) and dual (OPA2350) come in the miniature MSOP-8 surface mount, SO-8 surface mount, and DIP-8 packages. The quad (OPA4350) packages are the space-saving SSOP-16 surface mount and SO-14 surface mount. All are specified from −40°C to +85°C and operate from −55°C to +150°C.

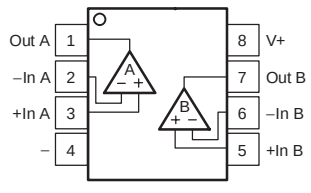
SPICE model available at www.ti.com

OPA350



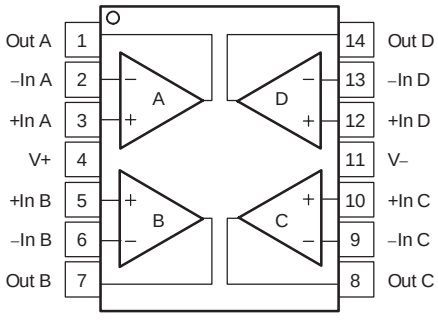
DIP−8, SO−8, MSOP−8

OPA2350



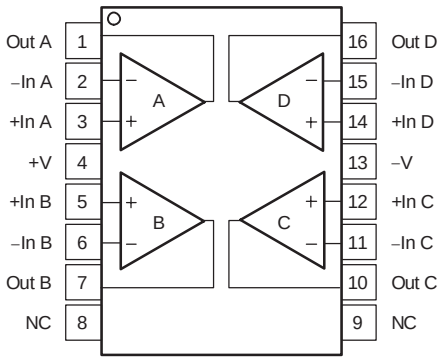
DIP−8, SO−8, MSOP−8

OPA4350



SO−14

OPA4350



SSOP−16

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	7.0V
Signal Input Terminals(2), Voltage	(V−) − 0.3V to (V+) + 0.3V
Current	10mA
Open Short-Circuit Current(3)	Continuous
Operating Temperature Range	−55°C to +150°C
Storage Temperature Range	−55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
SINGLE						
OPA350EA	MSOP-8	DGK	−40°C to +85°C	C50	OPA350EA/250	Tape and Reel, 250
					OPA350EA/2K5	Tape and Reel, 2500
OPA350UA	SO-8	D	−40°C to +85°C	OPA350UA	OPA350UA	Rails
					OPA350UA/2K5	Tape and Reel, 2500
OPA350PA	DIP-8	P	−40°C to +85°C	OPA350PA	OPA350PA	Rails
DUAL						
OPA2350EA	MSOP-8	DGK	−40°C to +85°C	D50	OPA2350EA/250	Tape and Reel, 250
					OPA2350EA/2K5	Tape and Reel, 2500
OPA2350UA	SO-8	D	−40°C to +85°C	OPA2350UA	OPA2350UA	Rails
					OPA2350UA/2K5	Tape and Reel, 2500
OPA2350PA	DIP-8	P	−40°C to +85°C	OPA2350PA	OPA2350PA	Rails
QUAD						
OPA4350EA	SSOP-16	DBQ	−40°C to +85°C	OPA4350EA	OPA4350EA/250	Tape and Reel, 250
					OPA4350EA/2K5	Tape and Reel, 2500
OPA4350UA	SO-14	D	−40°C to +85°C	OPA4350UA	OPA4350UA	Rails
					OPA4350UA/2K5	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the temperature range, **T_A = −40°C to +85°C**. V_S = 5V.

All specifications at T_A = +25°C, R_L = 1kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA350, OPA2350, OPA4350 MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 5V		±150	±500	µV
T_A = −40°C to +85°C					**±1**	mV
vs Temperature		**T_A = −40°C to +85°C**		**±4**		µV/°C
vs Power-Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5V, V_{CM} = 0V		40	150	µV/V
T_A = −40°C to +85°C		**V_S = 2.7V to 5.5V, V_{CM} = 0V**			**175**	µV/V
Channel Separation (dual, quad)		dc		0.15		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.5	±10	pA
vs Temperature				See Typical Characteristics		
Input Offset Current	I_{OS}			±0.5	±10	pA
NOISE						
Input Voltage Noise, f = 100Hz to 400kHz				4		µVrms
Input Voltage Noise Density, f = 10kHz	e_n			7		nV/√Hz
Input Current Noise Density, f = 100kHz				5		nV/√Hz
Current Noise Density, f = 10kHz	i_n			4		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	**T_A = −40°C to +85°C**	**−0.1**		**(V+) + 0.1**	V
Common-Mode Rejection Ratio	CMRR	V_S = 2.7V, −0.1V < V_{CM} < 2.8V	66	84		dB
		V_S = 5.5V, −0.1V < V_{CM} < 5.6V	74	90		dB
T_A = −40°C to +85°C		**V_S = 5.5V, −0.1V < V_{CM} < 5.6V**	**74**			dB
INPUT IMPEDANCE						
Differential				10^{13} ‖ 2.5		Ω ‖ pF
Common-Mode				10^{13} ‖ 6.5		Ω ‖ pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 10kΩ, 50mV < V_O < (V+) −50mV	100	122		dB
T_A = −40°C to +85°C		**R_L = 10kΩ, 50mV < V_O < (V+) −50mV**	**100**			dB
		R_L = 1kΩ, 200mV < V_O < (V+) −200mV	100	120		dB
T_A = −40°C to +85°C		**R_L = 1kΩ, 200mV < V_O < (V+) −200mV**	**100**			dB
FREQUENCY RESPONSE		C_L = 100pF				
Gain-Bandwidth Product	GBW	G = 1		38		MHz
Slew Rate	SR	G = 1		22		V/µs
Settling Time: 0.1%		G = ±1, 2V Step		0.22		µs
0.01%		G = ±1, 2V Step		0.5		µs
Overload Recovery Time		V_{IN} • G = V_S		0.1		µs
Total Harmonic Distortion + Noise	THD+N	R_L = 600Ω, V_O = 2.5V_{PP}(2), G = 1, f = 1kHz		0.0006		%
Differential Gain Error		G = 2, R_L = 600Ω, V_O = 1.4V(3)		0.17		%
Differential Phase Error		G = 2, R_L = 600Ω, V_O = 1.4V(3)		0.17		deg

(1) V_S = +5V.
(2) V_{OUT} = 0.25V to 2.75V.
(3) NTSC signal generator used. See Figure 6 for test circuit.
(4) Output voltage swings are measured between the output and power supply rails.
(5) See typical characteristic curve, *Output Voltage Swing vs Output Current*.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V (continued)

Boldface limits apply over the temperature range, **T_A = −40°C to +85°C**. V_S = 5V.

All specifications at T_A = +25°C, R_L = 1kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

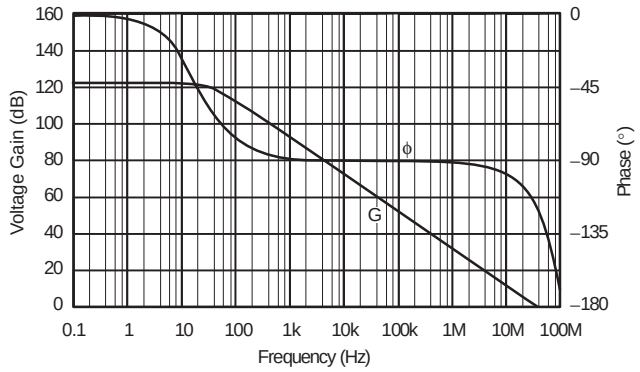
PARAMETER		TEST CONDITIONS	OPA350, OPA2350, OPA4350 MIN	TYP(1)	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail(4)	V_{OUT}	R_L = 10kΩ, A_{OL} ≥ 100dB		10	50	mV
T_A = −40°C to +85°C		**R_L = 10kΩ, A_{OL} ≥ 100dB**			**50**	mV
		R_L = 1kΩ, A_{OL} ≥ 100dB		25	200	mV
T_A = −40°C to +85°C		**R_L = 1kΩ, A_{OL} ≥ 100dB**			**200**	mV
Output Current	I_{OUT}			±40(5)		mA
Short-Circuit Current	I_{SC}			±80		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
POWER SUPPLY						
Operating Voltage Range	V_S	**T_A = −40°C to +85°C**	**2.7**		**5.5**	V
Minimum Operating Voltage				2.5		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		5.2	7.5	mA
T_A = −40°C to +85°C		I_O = 0			**8.5**	mA
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range			−55		+150	°C
Storage Range			−55		+150	°C
Thermal Resistance	θ_{JA}					
MSOP-8 Surface Mount				150		°C/W
SO-8 Surface Mount				150		°C/W
DIP-8				100		°C/W
SO-14 Surface Mount				100		°C/W
SSOP-16 Surface Mount				100		°C/W

(1) V_S = +5V.
(2) V_{OUT} = 0.25V to 2.75V.
(3) NTSC signal generator used. See Figure 6 for test circuit.
(4) Output voltage swings are measured between the output and power supply rails.
(5) See typical characteristic curve, *Output Voltage Swing vs Output Current*.

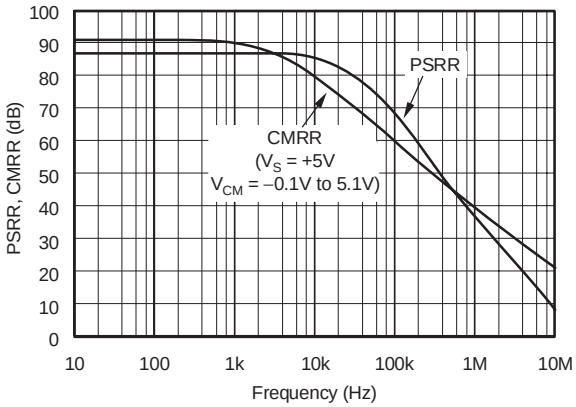
TYPICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

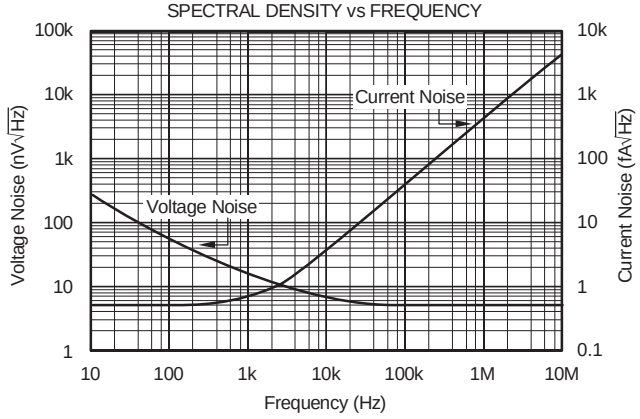
OPEN-LOOP GAIN/PHASE vs FREQUENCY



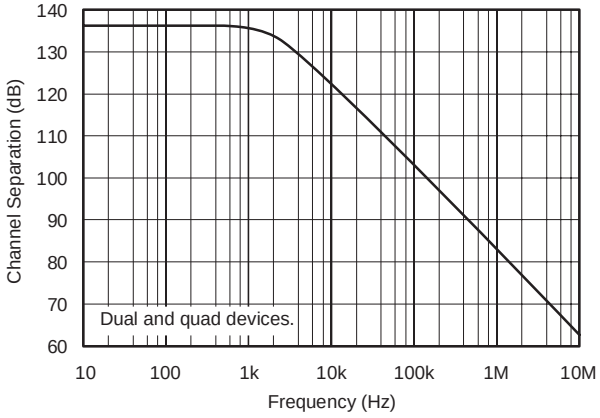
POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



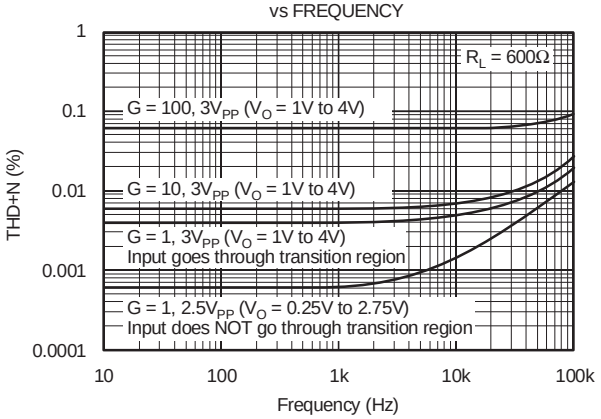
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



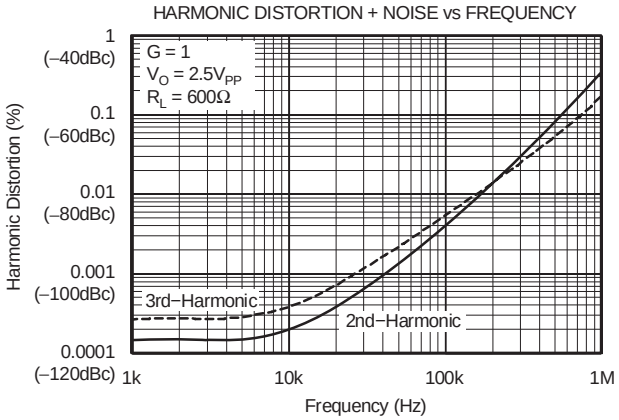
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



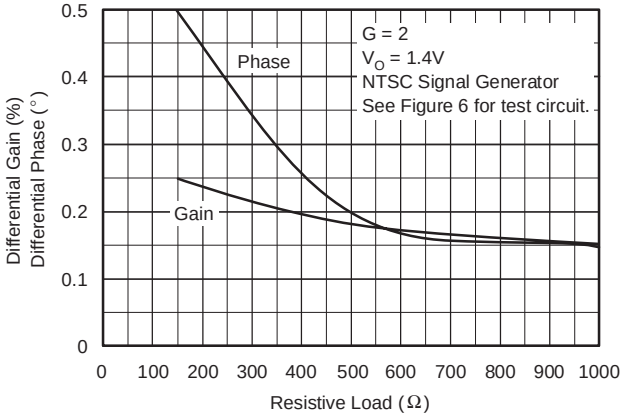
HARMONIC DISTORTION + NOISE vs FREQUENCY



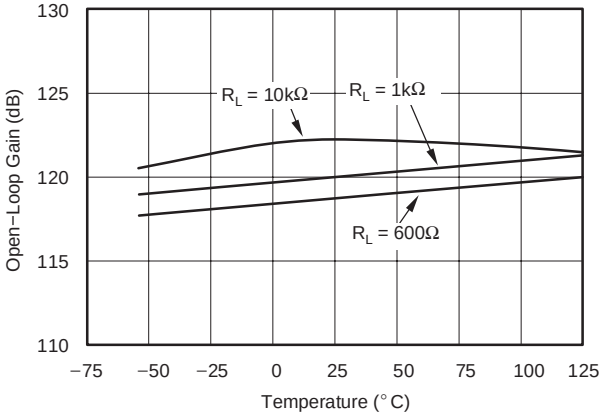
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

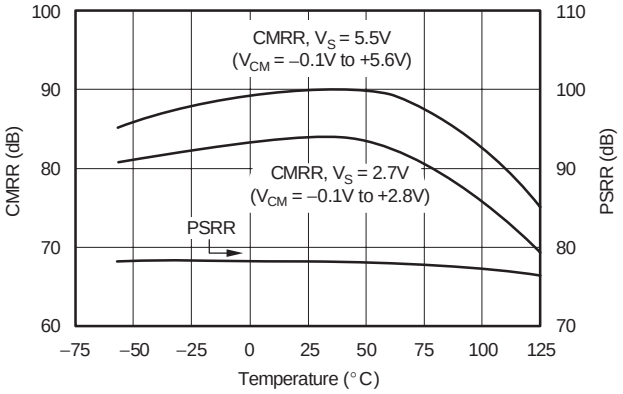
DIFFERENTIAL GAIN/PHASE vs RESISTIVE LOAD



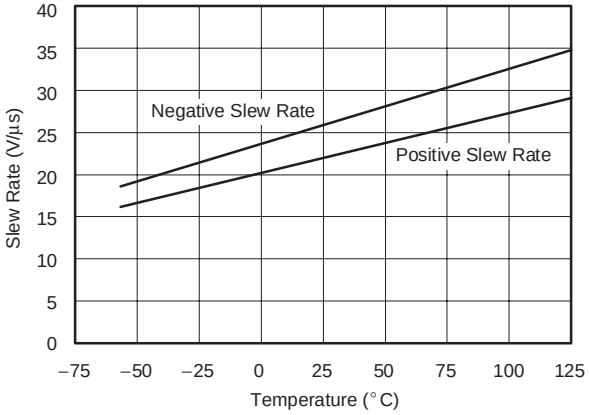
OPEN−LOOP GAIN vs TEMPERATURE



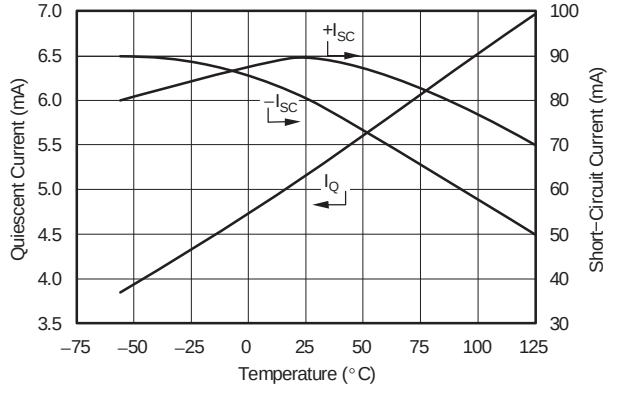
COMMON−MODE AND POWER−SUPPLY REJECTION RATIO vs TEMPERATURE



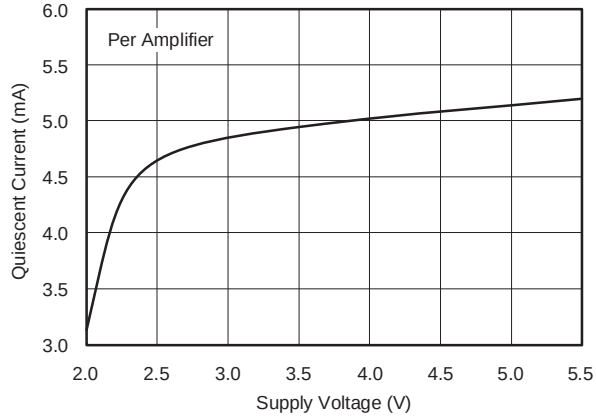
SLEW RATE vs TEMPERATURE



QUIESCENT CURRENT AND SHORT−CIRCUIT CURRENT vs TEMPERATURE



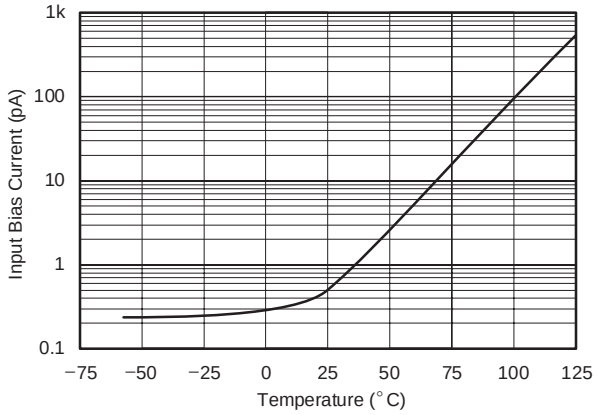
QUIESCENT CURRENT vs SUPPLY VOLTAGE



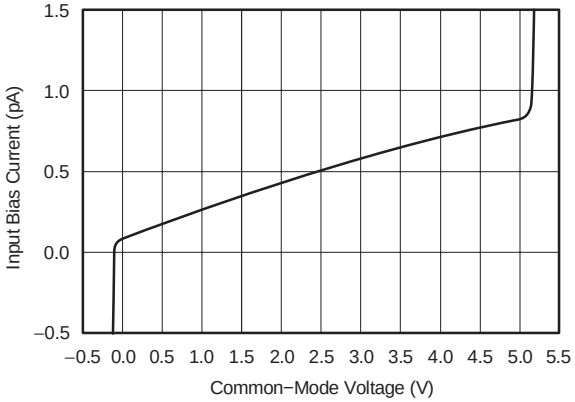
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

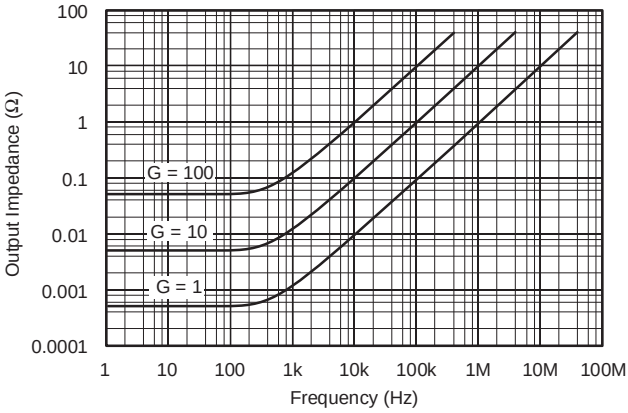
INPUT BIAS CURRENT vs TEMPERATURE



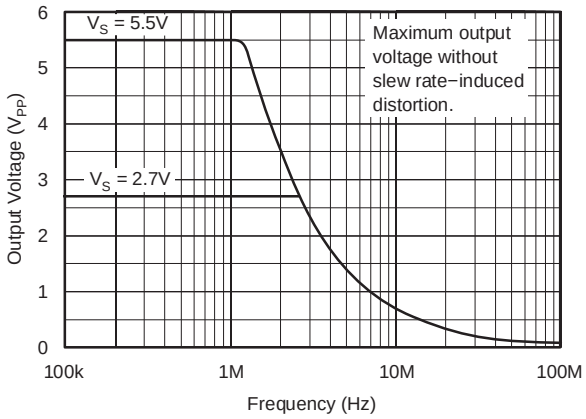
INPUT BIAS CURRENT
vs INPUT COMMON−MODE VOLTAGE



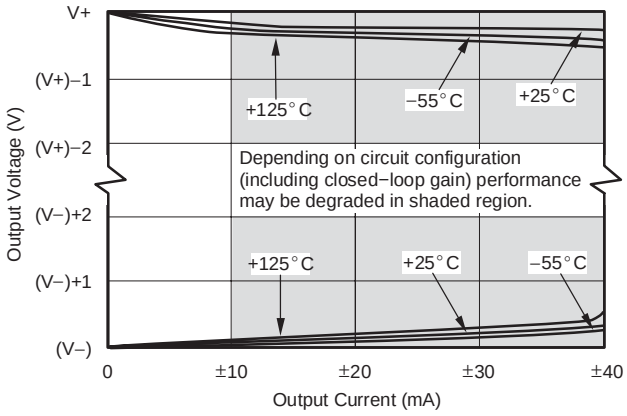
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



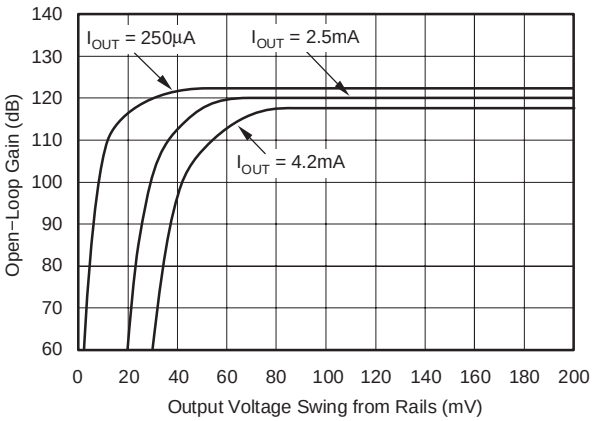
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



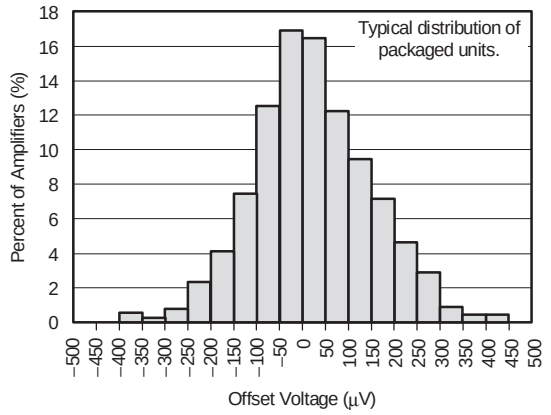
OPEN−LOOP GAIN vs OUTPUT VOLTAGE SWING



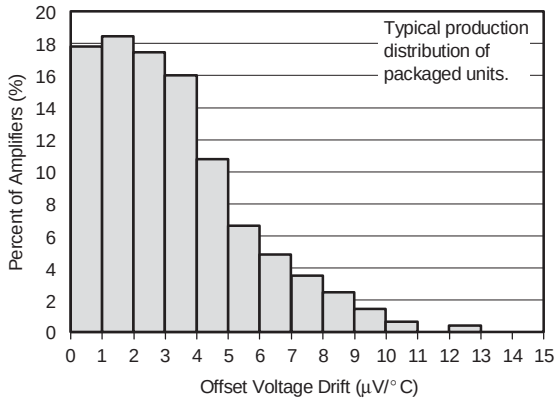
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_S = +5V, and R_L = 1kΩ connected to V_S/2, unless otherwise noted.

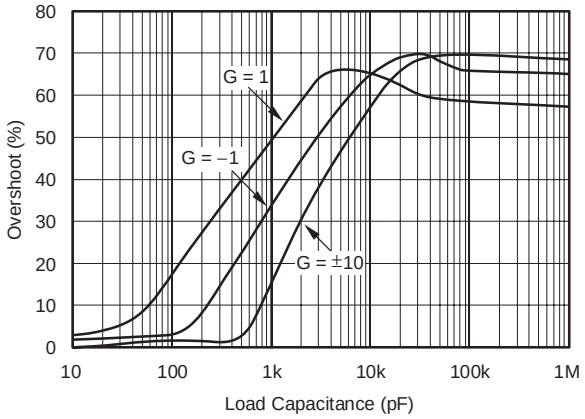
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



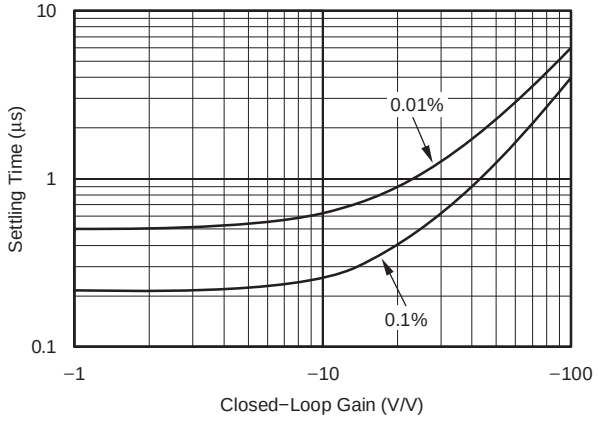
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



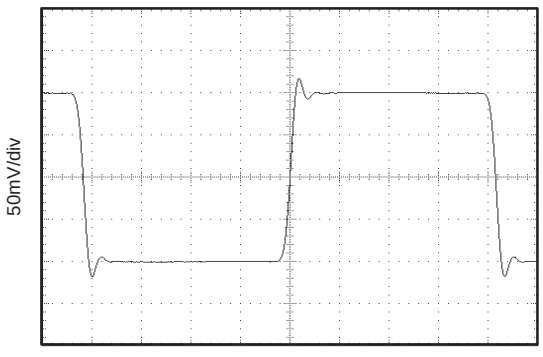
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



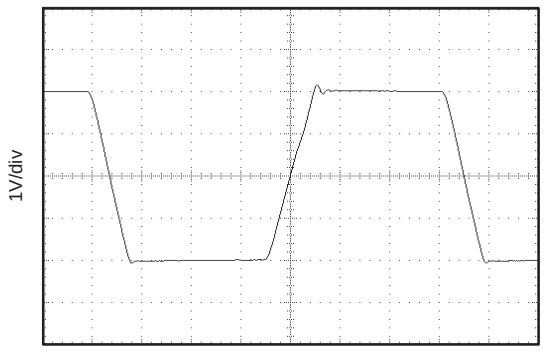
SETTLING TIME vs CLOSED−LOOP GAIN



SMALL−SIGNAL STEP RESPONSE
C_L = 100pF



LARGE−SIGNAL STEP RESPONSE
C_L = 100pF



APPLICATIONS INFORMATION

OPA350 series op amps are fabricated on a state-of-the-art 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input/output make them ideal for driving sampling A/D converters. They are also well-suited for controlling the output power in cell phones. These applications often require high speed and low noise. In addition, the OPA350 series offers a low-cost solution for general-purpose and consumer video applications (75Ω drive capability).

Excellent ac performance makes the OPA350 series well-suited for audio applications. Their bandwidth, slew rate, low noise (5nV/√Hz), low THD (0.0006%), and small package options are ideal for these applications. The class AB output stage is capable of driving 600Ω loads connected to any point between V+ and ground.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low voltage supply applications. Figure 1 shows the input and output waveforms for the OPA350 in unity-gain configuration. Operation is from a single +5V supply with a 1kΩ load connected to $V_S/2$. The input is a $5V_{PP}$ sinusoid. Output voltage swing is approximately $4.95V_{PP}$.

Power supply pins should be bypassed with 0.01µF ceramic capacitors.

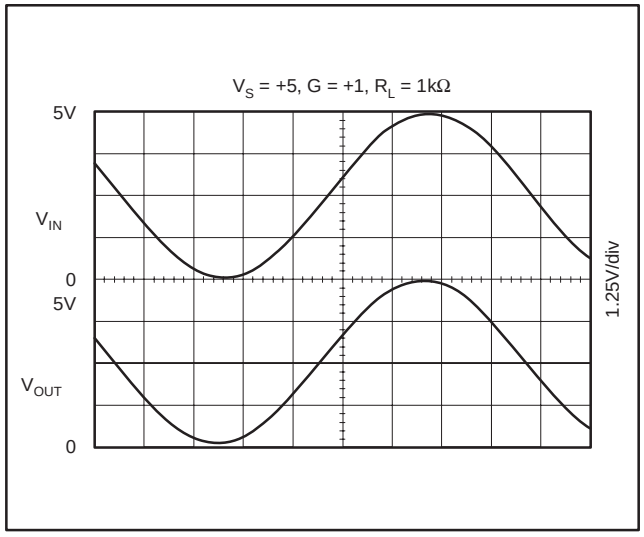


Figure 1. Rail-to-Rail Input and Output

OPERATING VOLTAGE

OPA350 series op amps are fully specified from +2.7V to +5.5V. However, supply voltage may range from +2.5V to +5.5V. Parameters are tested over the specified supply range—a unique feature of the OPA350 series. In addition, many specifications apply from −40°C to +85°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage or temperature are shown in the typical characteristics.

RAIL-TO-RAIL INPUT

The tested input common-mode voltage range of the OPA350 series extends 100mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 2. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.8V to 100mV above the positive supply, while the P-channel pair is on for inputs from 100mV below the negative supply to approximately (V+) – 1.8V. There is a small transition region, typically (V+) – 2V to (V+) – 1.6V, in which both pairs are on. This 400mV transition region can vary ±400mV with process variation. Thus, the transition region (both input stages on) can range from (V+) – 2.4V to (V+) – 2.0V on the low end, up to (V+) – 1.6V to (V+) – 1.2V on the high end.

OPA350 series op amps are laser-trimmed to reduce offset voltage difference between the N-channel and P-channel input stages, resulting in improved common-mode rejection and a smooth transition between the N-channel pair and the P-channel pair. However, within the 400mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 500fA. However, large inputs (greater than 300mV beyond the supply rails) can turn on the OPA350's input protection diodes, causing excessive current to flow in or out of the input pins. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 3. Many input signals are inherently current-limited to less than 10mA; therefore, a limiting resistor is not required.

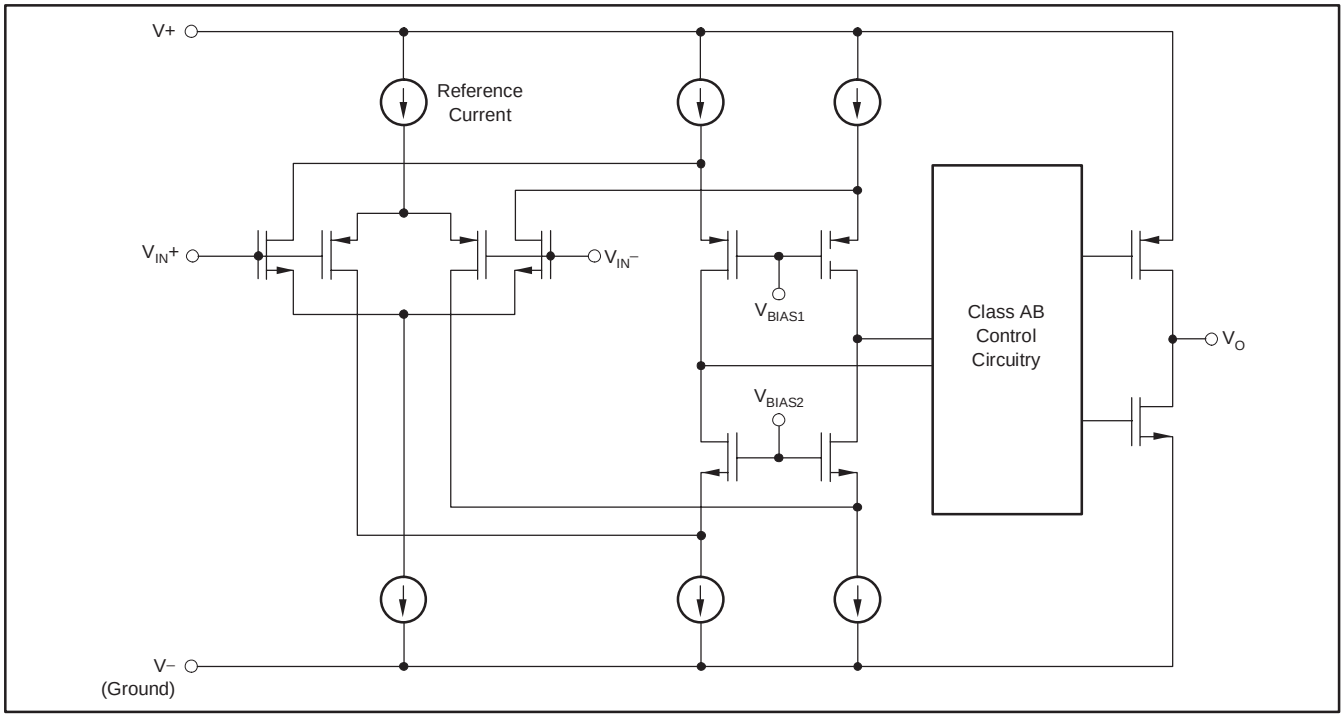


Figure 2. Simplified Schematic

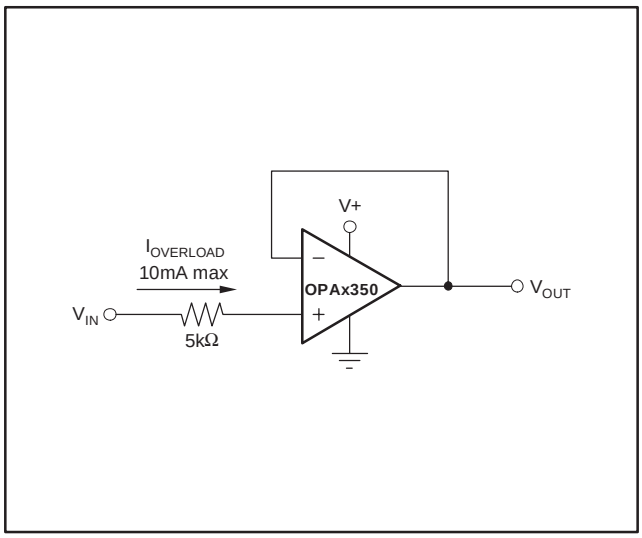


Figure 3. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (>10kΩ), the output voltage swing is typically ten millivolts from the supply rails. With heavier resistive loads (600Ω to 10kΩ), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain. See the typical characteristics *Output Voltage Swing vs Output Current* and *Open-Loop Gain vs Output Voltage*.

CAPACITIVE LOAD AND STABILITY

OPA350 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the op amp's output impedance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin.

In unity gain, OPA350 series op amps perform well with very large capacitive loads. Increasing gain enhances the amplifier's ability to drive more capacitance. The typical characteristic *Small-Signal Overshoot vs Capacitive Load* shows performance with a 1kΩ resistive load. Increasing load resistance improves capacitive load drive capability.

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 4. This capacitor compensates for the zero created by the feedback network impedance and the OPA350's input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.

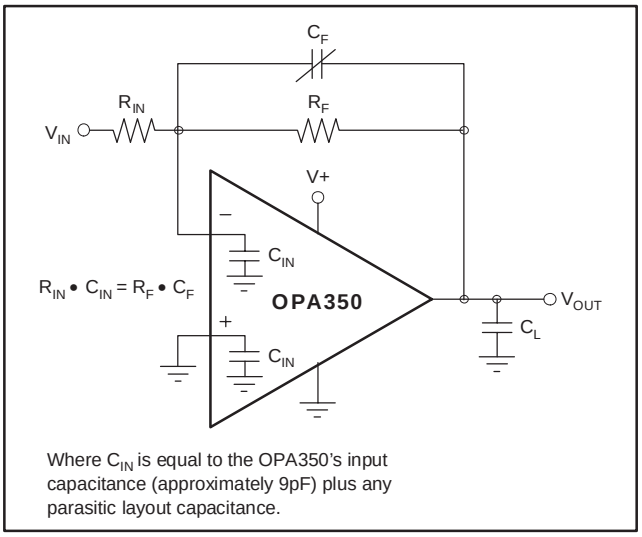


Figure 4. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor since input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 4, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA350 (typically 9pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{IN} \cdot C_{IN} = R_F \cdot C_F$$

where C_{IN} is equal to the OPA350's input capacitance (sum of differential and common-mode) plus the layout capacitance. The capacitor can be varied until optimum performance is obtained.

DRIVING A/D CONVERTERS

OPA350 series op amps are optimized for driving medium speed (up to 500kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The OPA350 series provides an effective means of buffering the A/D's input capacitance and resulting charge injection while providing signal gain.

Figure 5 shows the OPA350 driving an ADS7861. The ADS7861 is a dual, 500kHz, 12-bit sampling converter in the tiny SSOP-24 package. When used with the miniature package options of the OPA350 series, the combination is ideal for space-limited applications. For further information, consult the ADS7861 data sheet (SBAS110A).

OUTPUT IMPEDANCE

The low frequency open-loop output impedance of the OPA350's common-source output stage is approximately 1kΩ. When the op amp is connected with feedback, this value is reduced significantly by the loop gain of the op amp. For example, with 122dB of open-loop gain, the output impedance is reduced in unity-gain to less than 0.001Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount which results in a ten-fold increase in effective output impedance (see the typical characteristic, *Output Impedance vs Frequency*).

At higher frequencies, the output impedance will rise as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive due to parasitic capacitance. This prevents the output impedance from becoming too high, which can cause stability problems when driving capacitive loads. As mentioned previously, the OPA350 has excellent capacitive load drive capability for an op amp with its bandwidth.

VIDEO LINE DRIVER

Figure 6 shows a circuit for a single supply, G = 2 composite video line driver. The synchronized outputs of a composite video line driver extend below ground. As shown, the input to the op amp should be ac-coupled and shifted positively to provide adequate signal swing to account for these negative signals in a single-supply configuration.

The input is terminated with a 75Ω resistor and ac-coupled with a 47μF capacitor to a voltage divider that provides the dc bias point to the input. In Figure 6, this point is approximately (V−) + 1.7V. Setting the optimal bias point requires some understanding of the nature of composite video signals. For best performance, one should be careful to avoid the distortion caused by the transition region of the OPA350's complementary input stage. Refer to the discussion of rail-to-rail input.

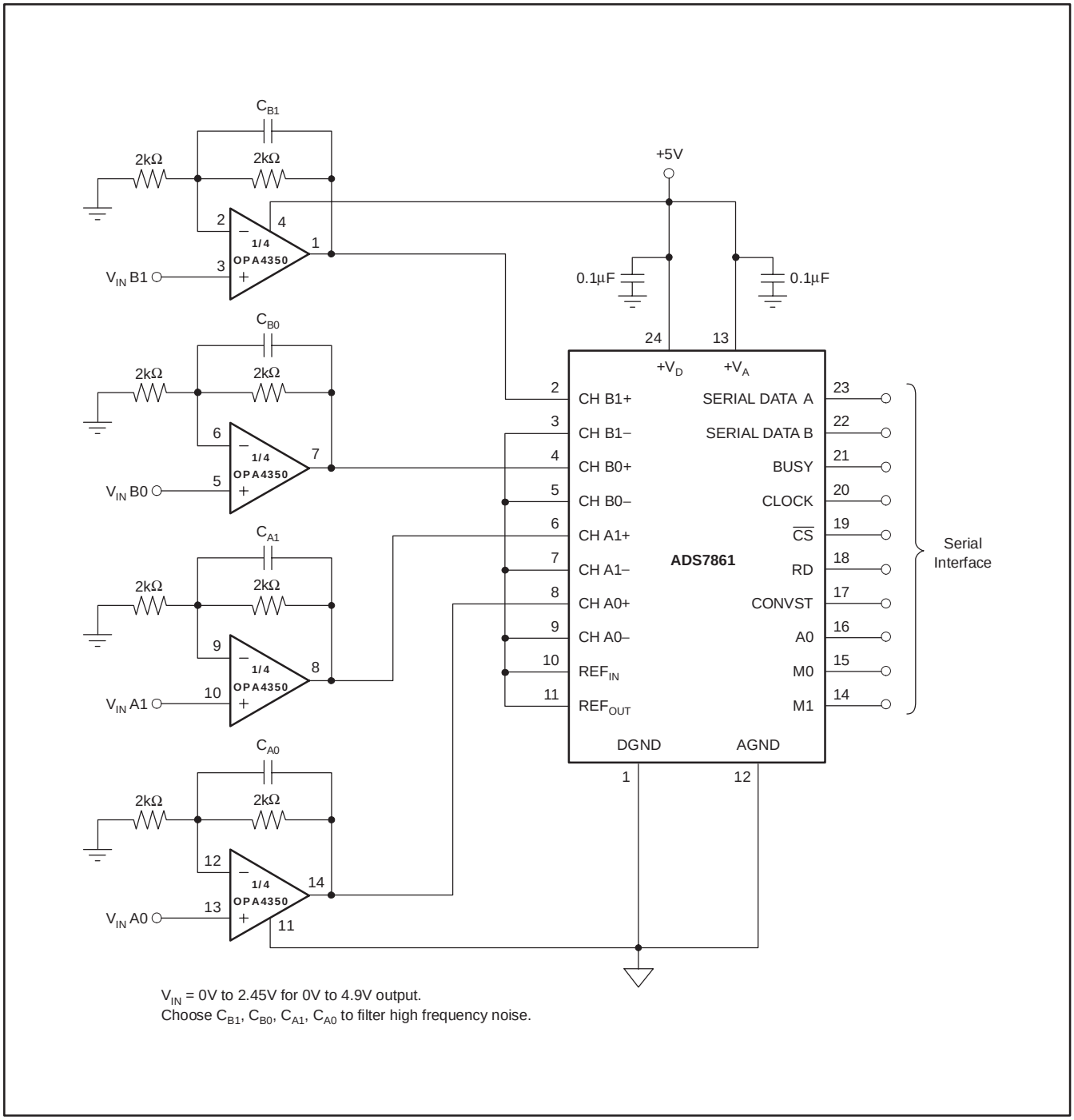


Figure 5. OPA4350 Driving Sampling A/D Converter

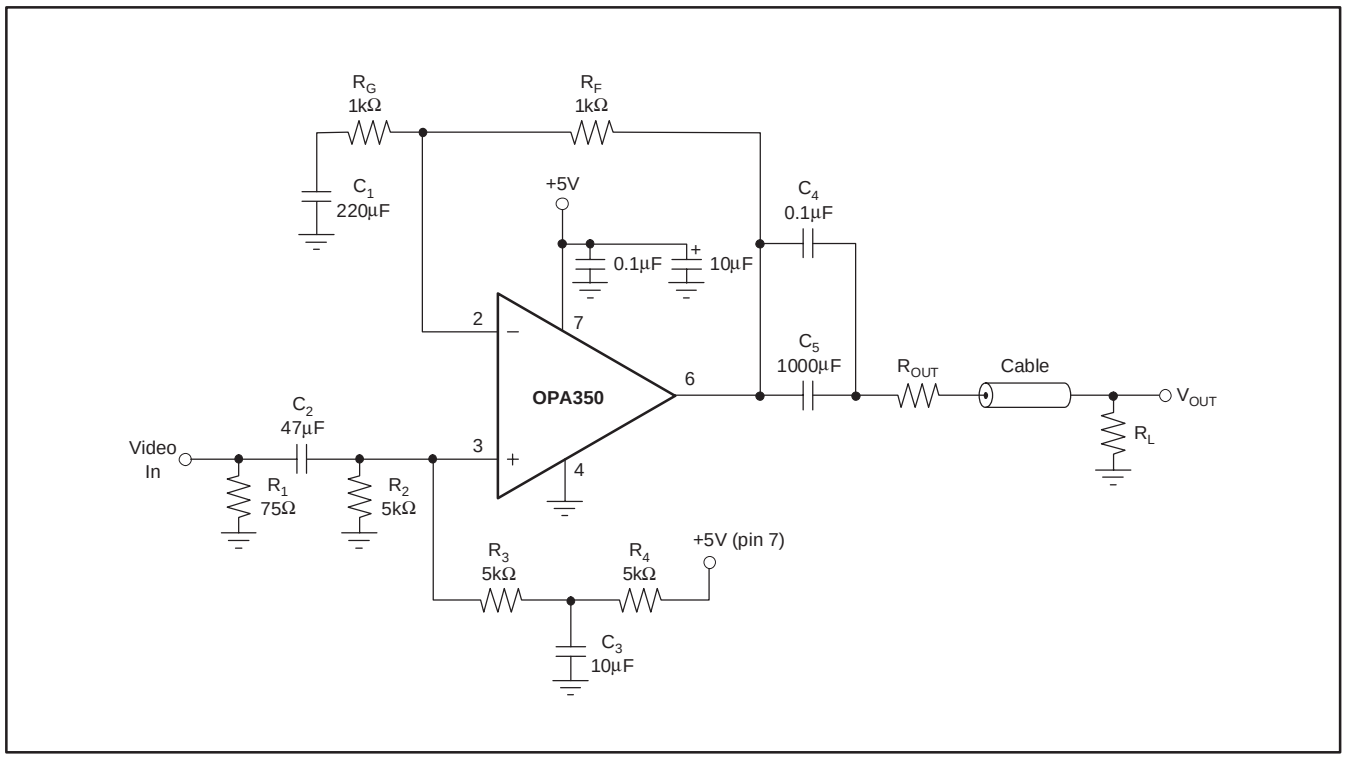


Figure 6. Single-Supply Video Line Driver

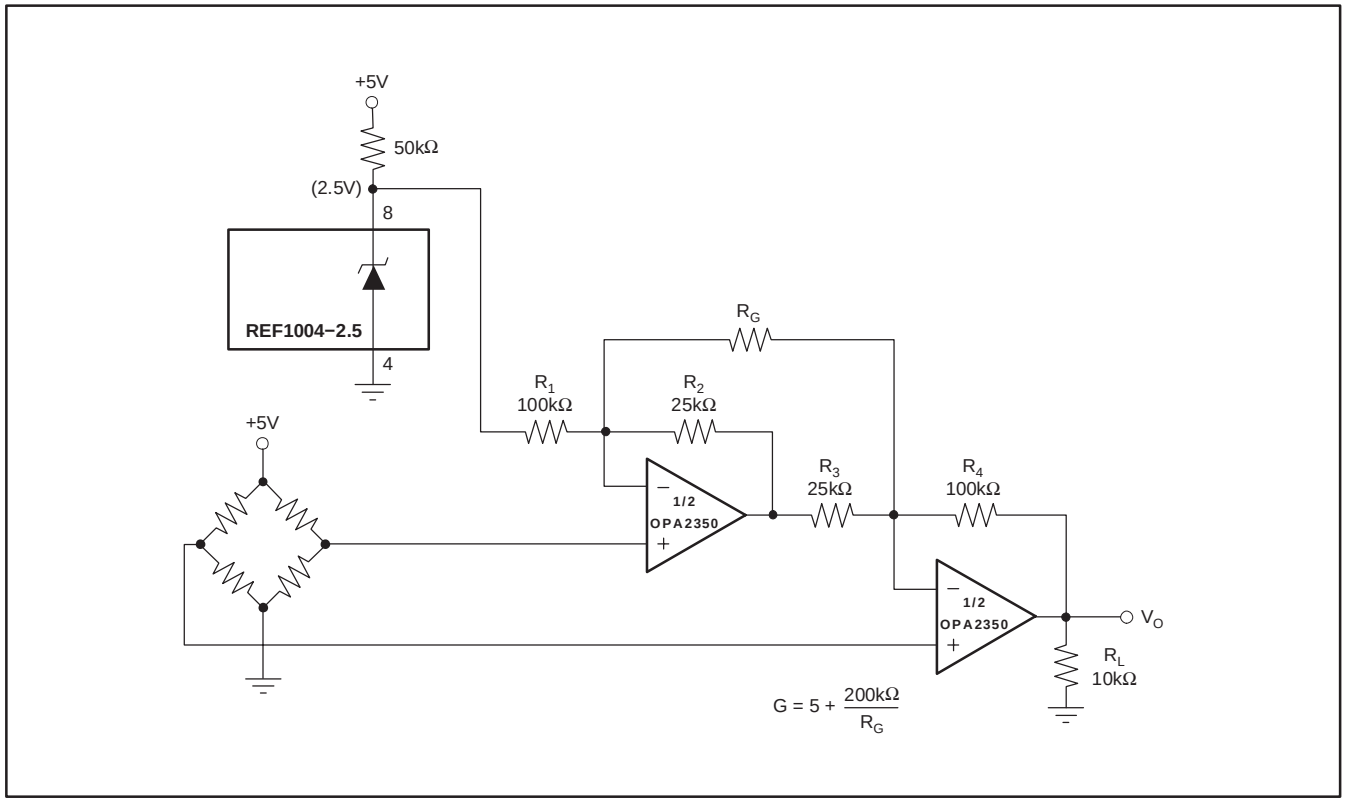


Figure 7. Two Op-Amp Instrumentation Amplifier With Improved High Frequency Common-Mode Rejection

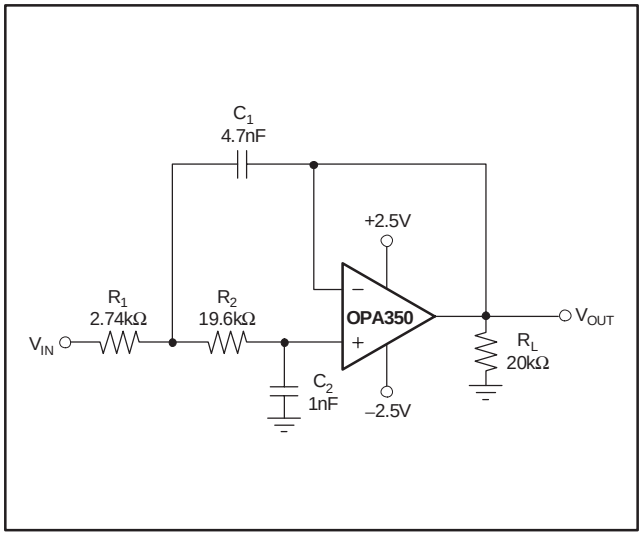


Figure 8. 10kHz Low-Pass Filter

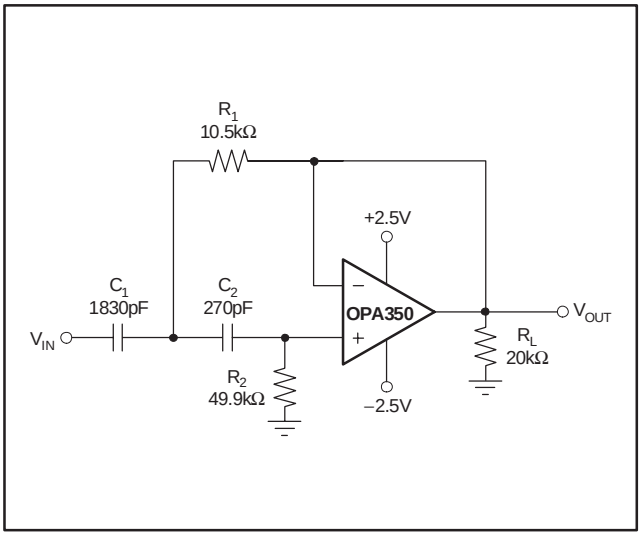


Figure 9. 10kHz High-Pass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2350EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50	Samples
OPA2350EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50	Samples
OPA2350EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50	Samples
OPA2350EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50	Samples
OPA2350PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2350PA	Samples
OPA2350PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2350PA	Samples
OPA2350UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA	Samples
OPA2350UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA	Samples
OPA2350UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA	Samples
OPA2350UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA	Samples
OPA350EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C50	Samples
OPA350EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C50	Samples
OPA350EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C50	Samples
OPA350EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C50	Samples
OPA350PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA350PA	Samples
OPA350PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA350PA	Samples
OPA350UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA350UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA	Samples
OPA350UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA	Samples
OPA350UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA	Samples
OPA4350EA/250	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 4350EA	Samples
OPA4350EA/250G4	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 4350EA	Samples
OPA4350EA/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4350EA	Samples
OPA4350EA/2K5G4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4350EA	Samples
OPA4350UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA4350UA	Samples
OPA4350UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA4350UA	Samples
OPA4350UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA4350UA	Samples
OPA4350UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA4350UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

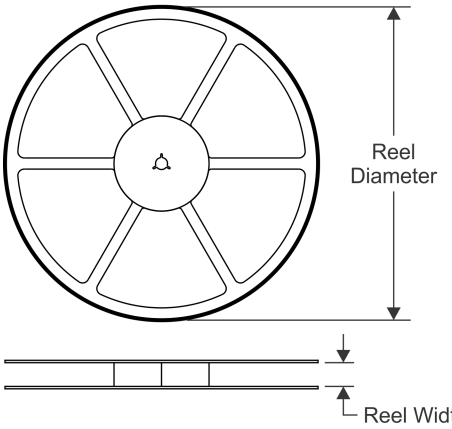
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

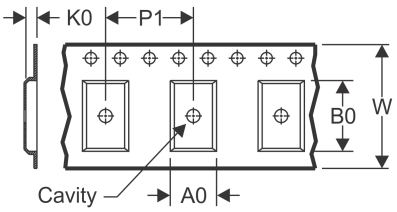
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

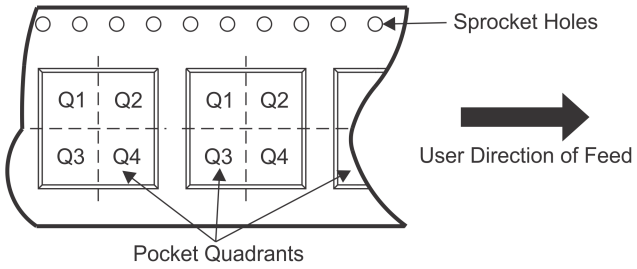


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

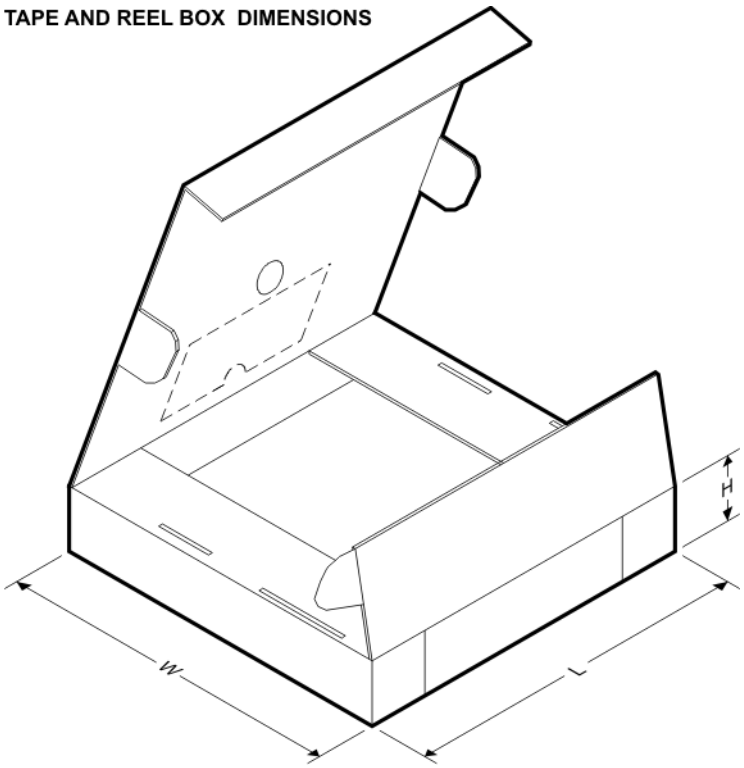
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2350EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2350EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

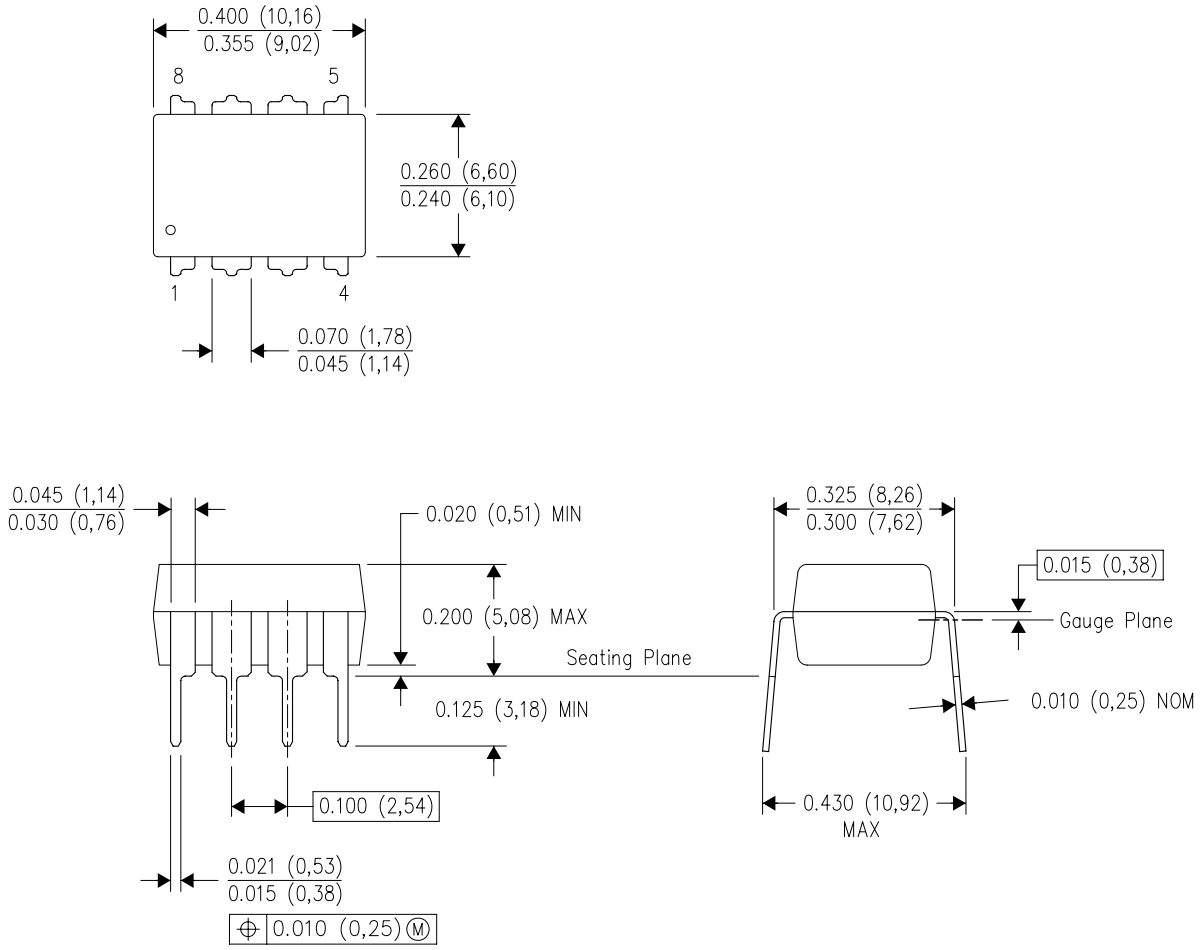
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

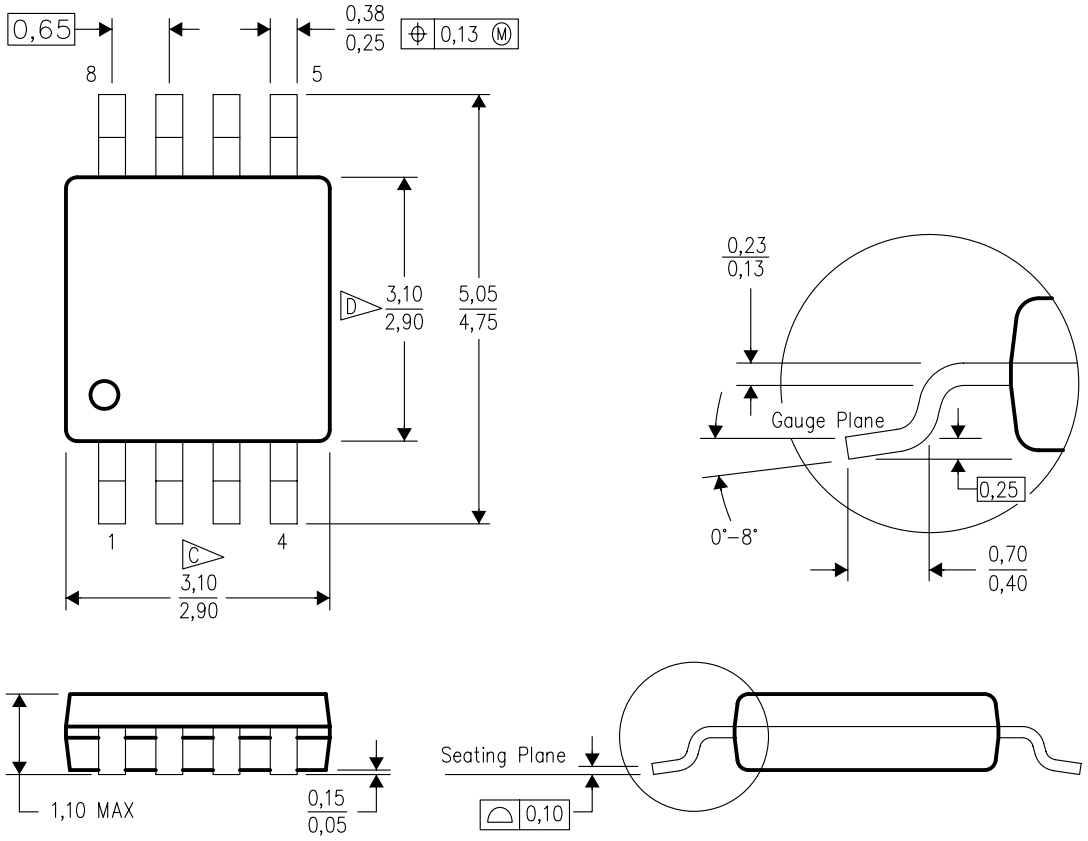
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2350EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2350EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA350EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA350UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4350EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA4350EA/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0
OPA4350UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

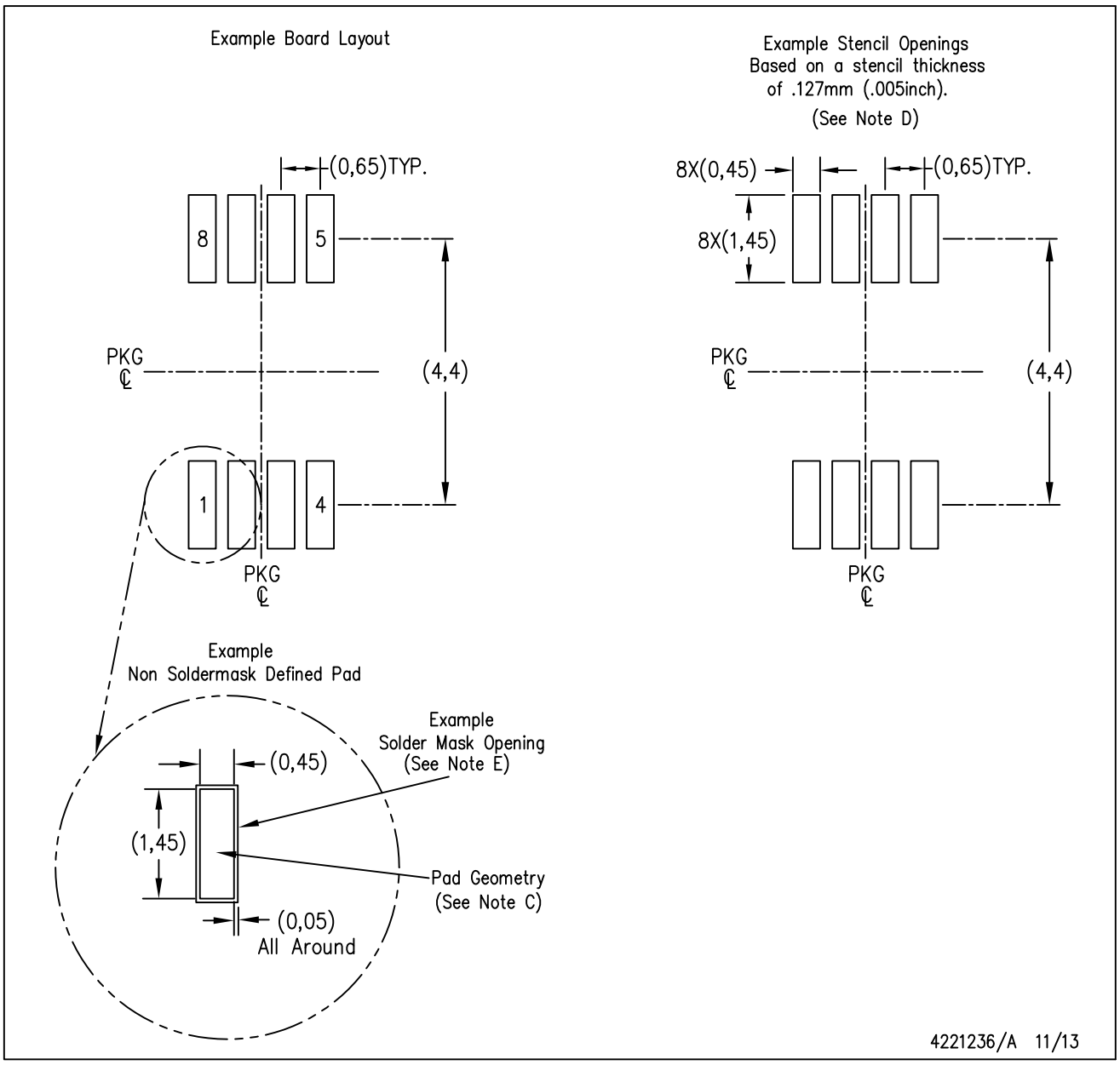
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

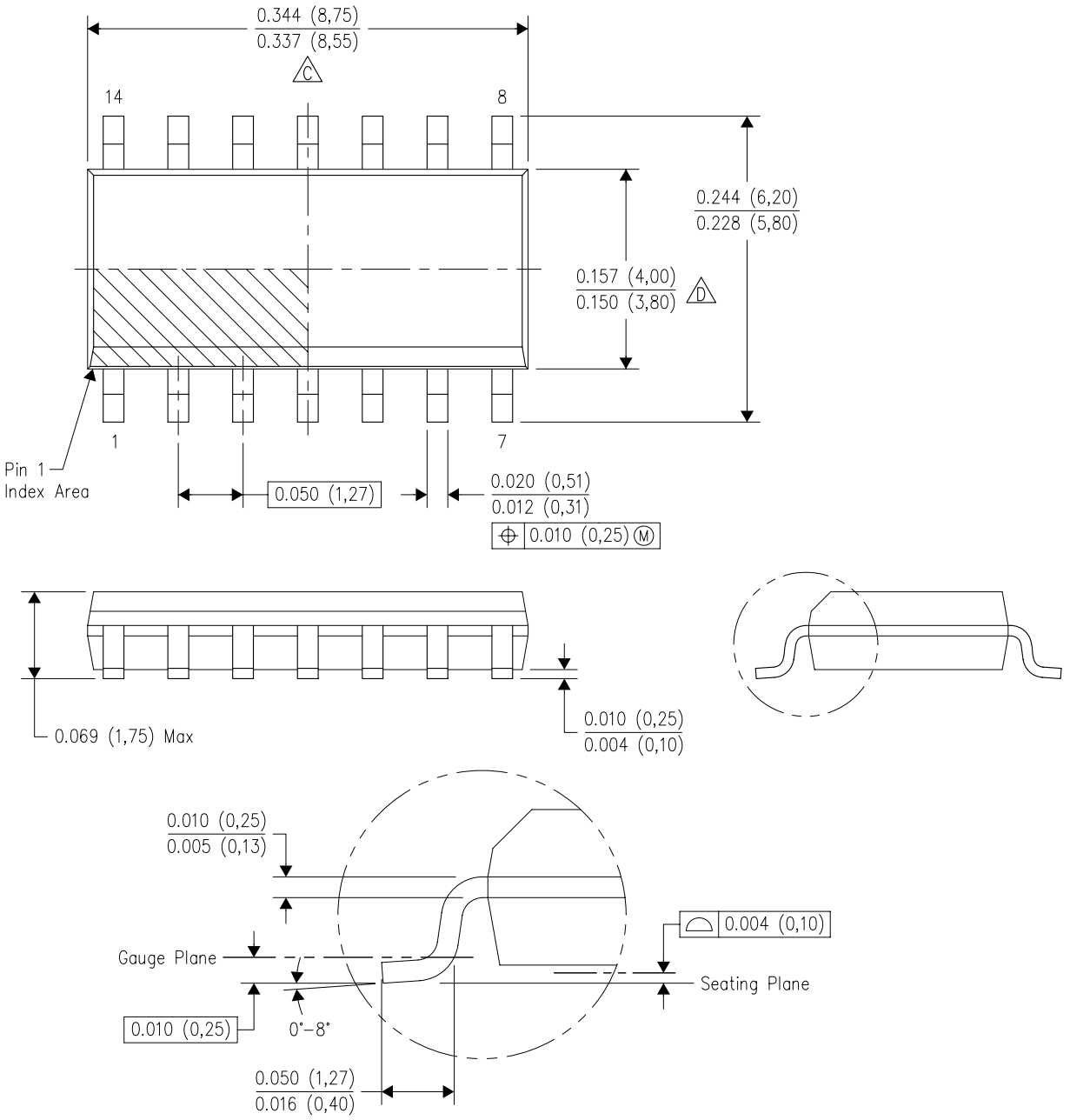
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

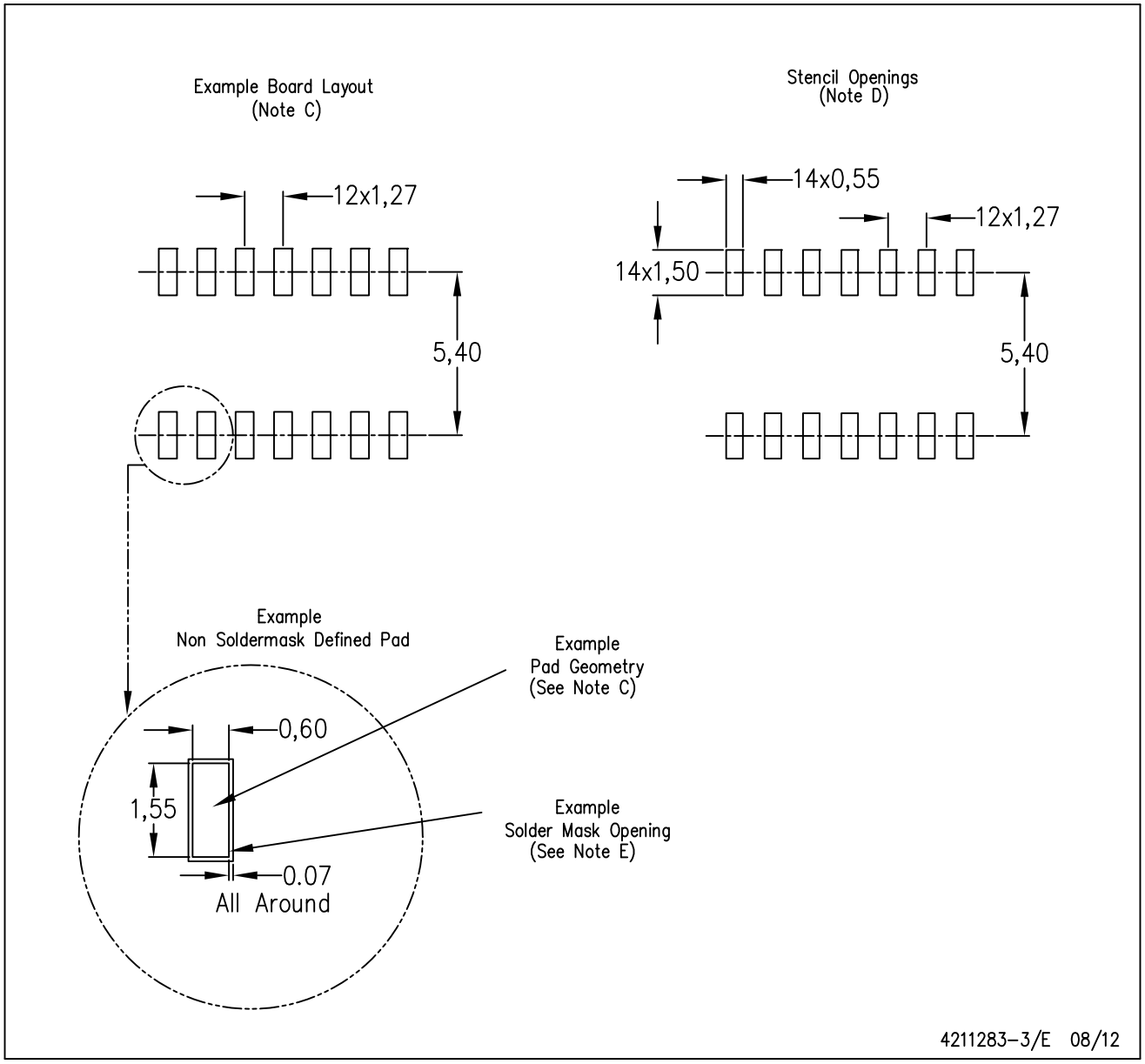
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

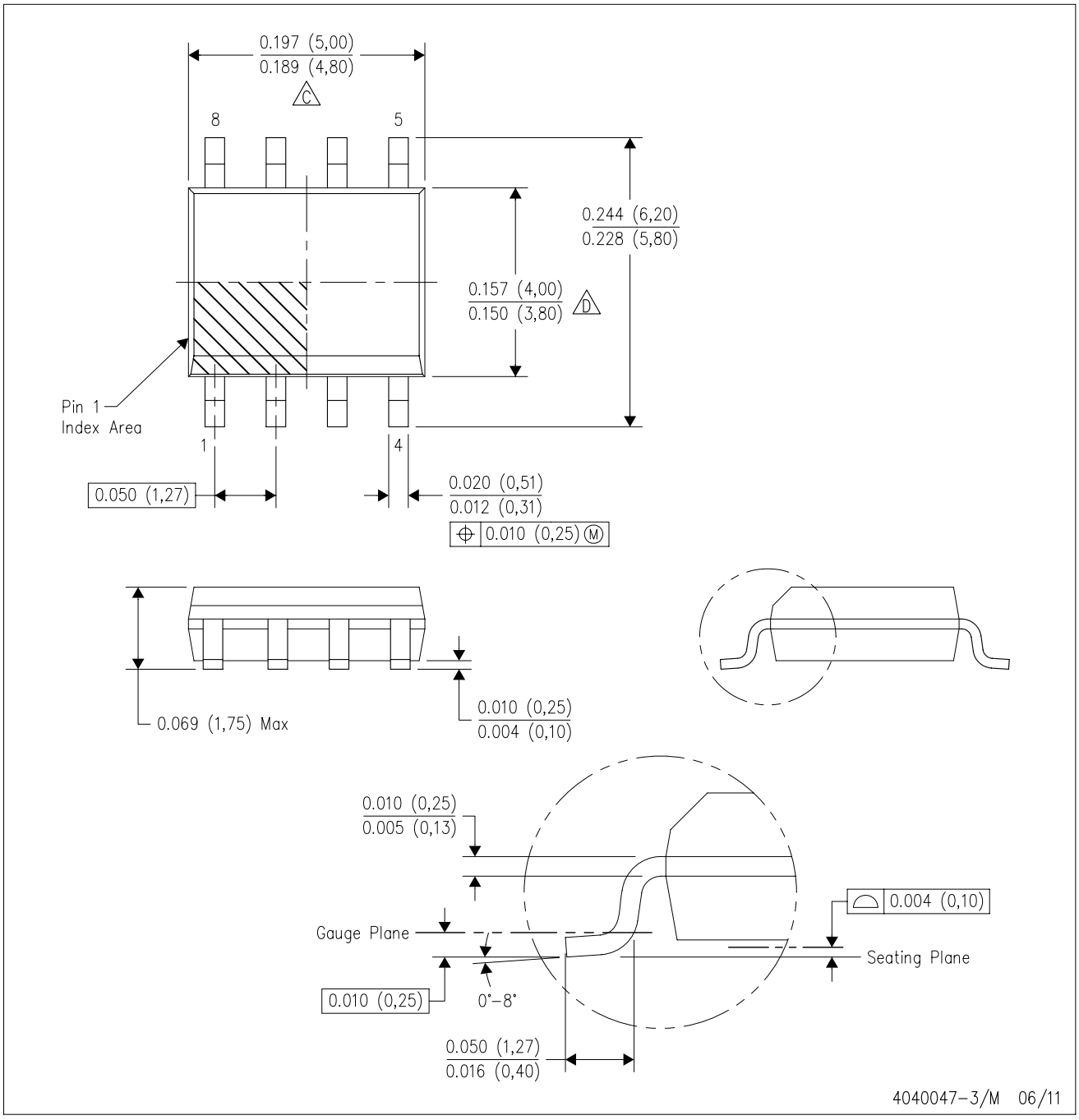
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



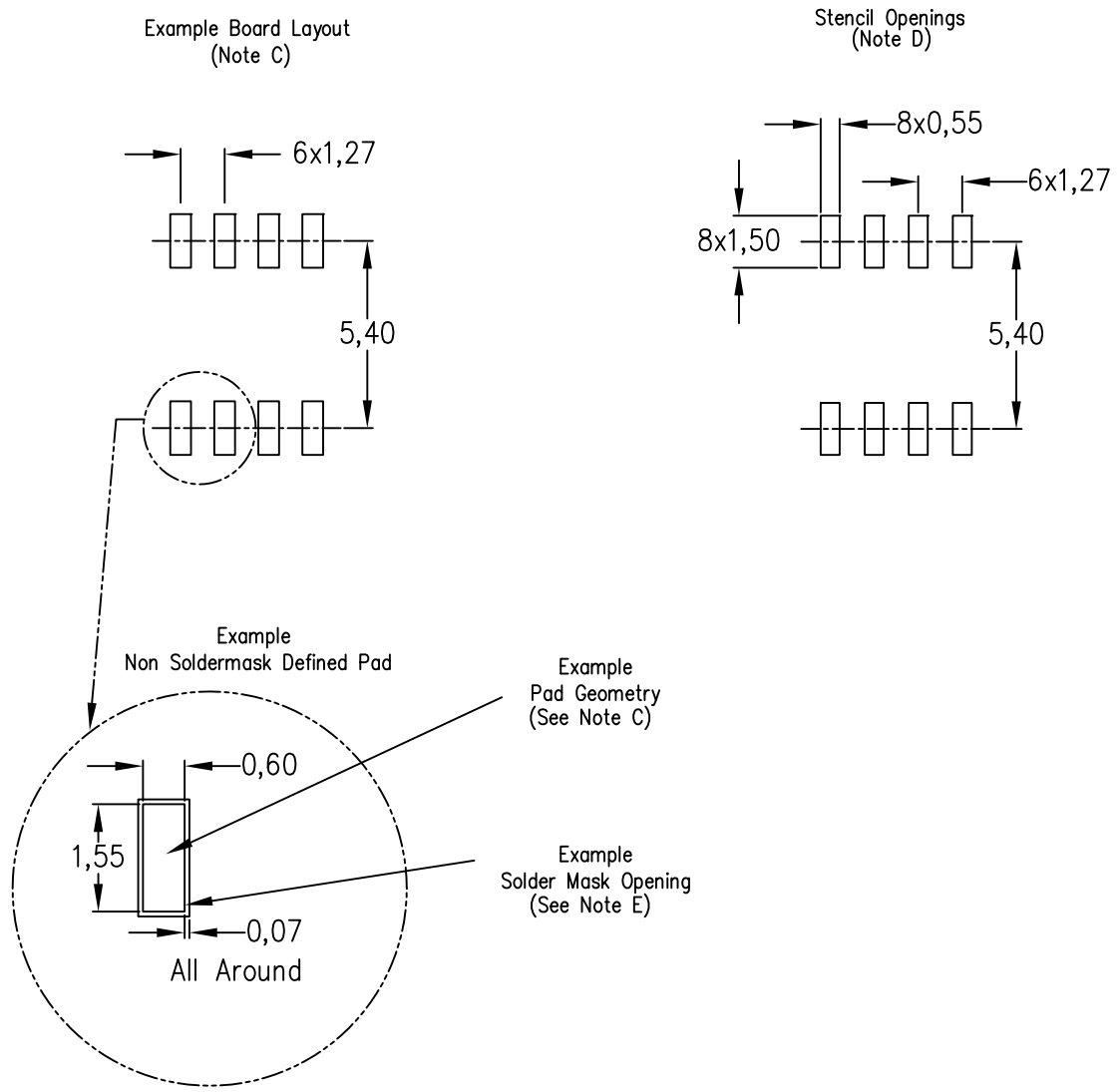
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



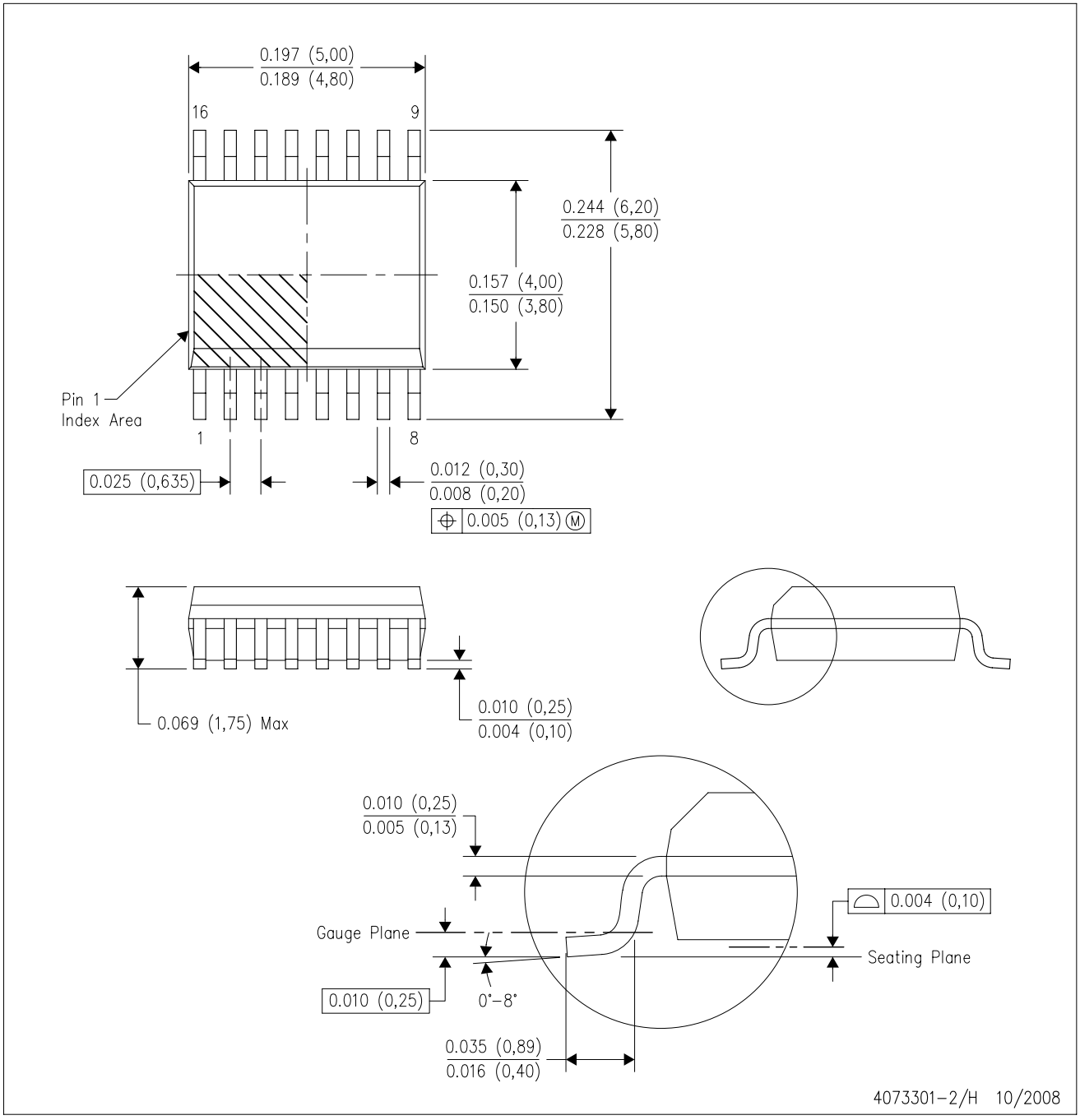
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



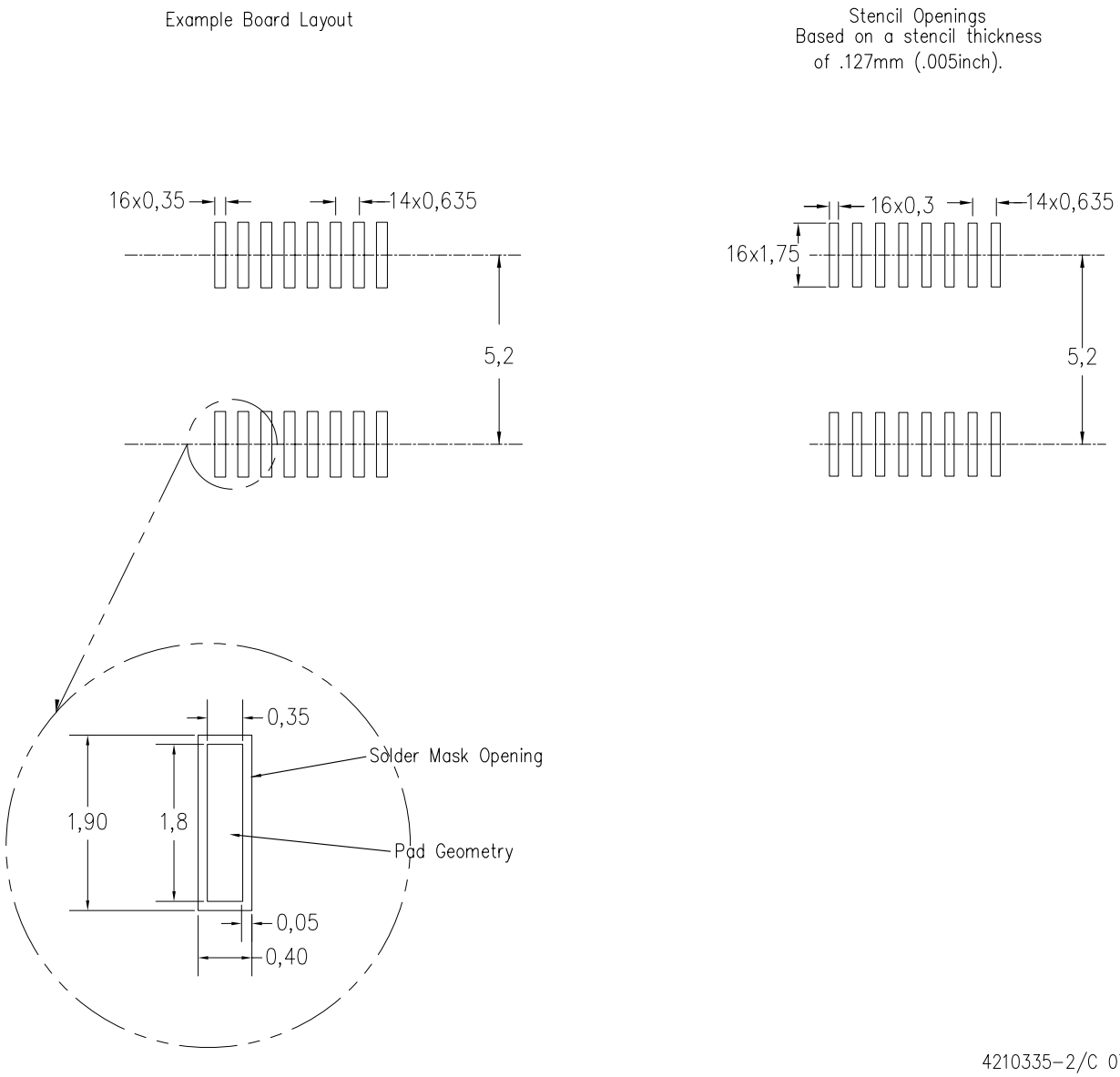
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.