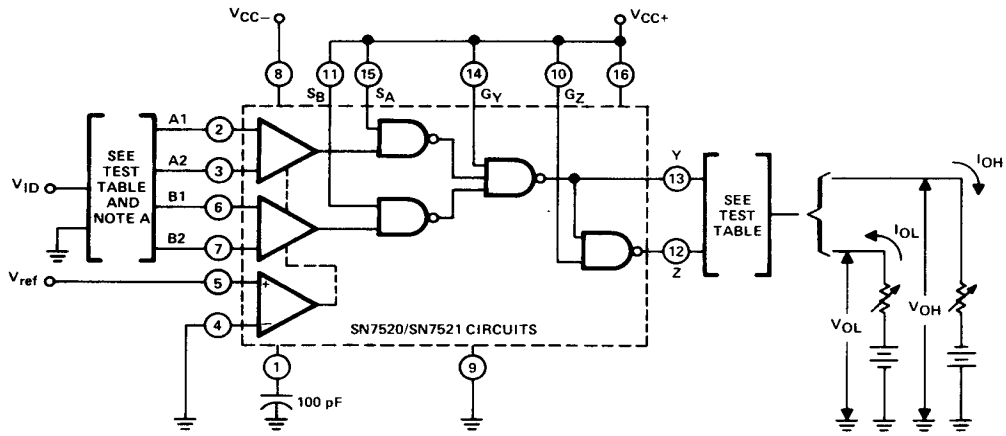
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7520	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
SN7521	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 1–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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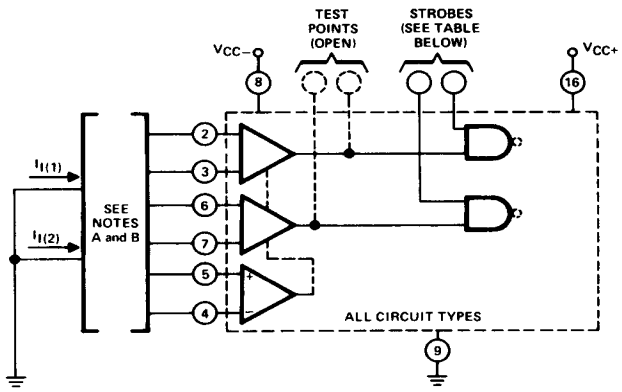
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	100 pF to GND	APPLY V_{CC+}	APPLY GND	LEAVE OPEN	OTHER
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z (14) (10)	S_A, S_B (15) (11)	Y, Z (13) (12)	
SN7522, SN7523	C_{ext} (1)	G (14)	S_A, S_B, GND 2 (15) (11) (13)		R_L, Y (10) (12)
SN7524, SN7525	C_{ext} (1)		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)	
SN7526, SN7527		PRESET, CLEAR (10) (14)	S_A, S_B (15) (11)	Q, $\bar{Q}$ (12) (13)	
SN7528, SN7529	C_{ext} (1)		1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)	
SN75232, SN75233, SN75234, SN75235			1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)	
SN75238, SN75239			1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)	

FIGURE 2–I_{IB}, I_{IO}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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d-c test circuits† (continued)

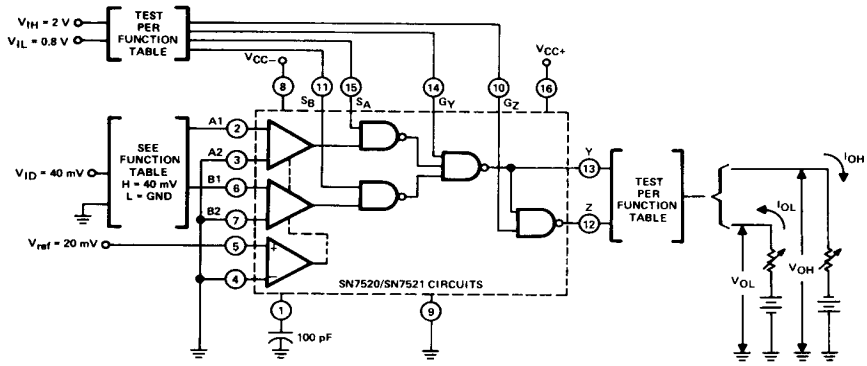
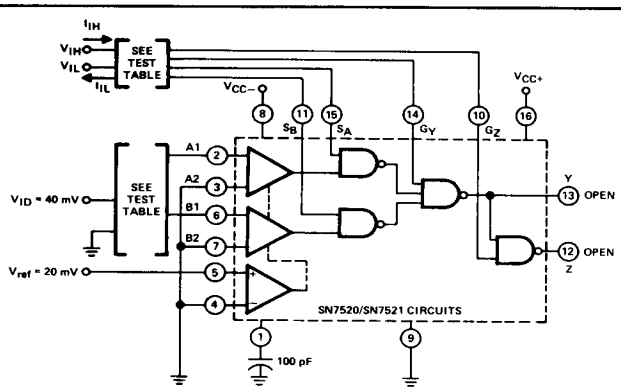


FIGURE 3–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

FIGURE 4–I_{IH}, I_{IL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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d-c test circuits† (continued)

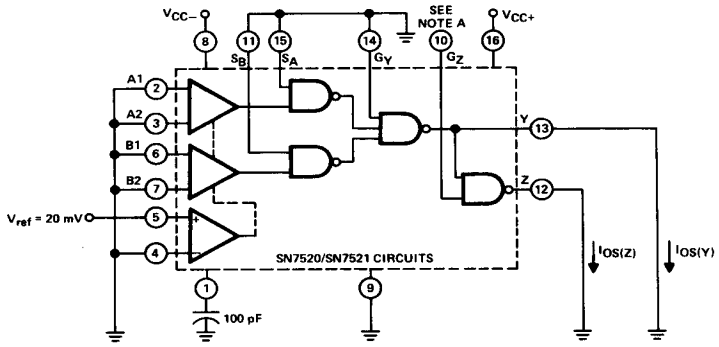
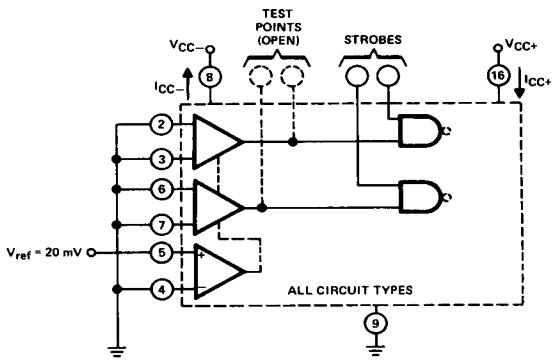


FIGURE 5–I_{OS}

NOTE A: When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	100 pF to GND	APPLY GND	LEAVE OPEN
SN7520, SN7521	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14) (10) (15) (11)	Y, Z (13) (12)
SN7522, SN7523	C_{ext} (1)	G, S_A, S_B, GND 2 (14) (15) (11) (13)	R_L, Y (10) (12)
SN7524, SN7525	C_{ext} (1)	1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN7526, SN7527		S_A, S_B (15) (11)	PRESET, CLEAR, Q, $\overline{Q}$ (10) (14) (12) (13)
SN7528, SN7529	C_{ext} (1)	1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)
SN75234, SN75235		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN75238, SN75239		1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)

FIGURE 6–I_{CC+}, I_{CC-}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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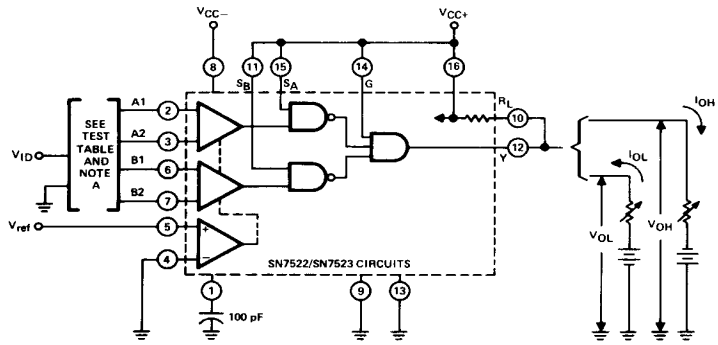
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7522	A1-A2 or B1-B2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≤0.4 V		16 mA
SN7523	A1-A2 or B1-B2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 7–V_T

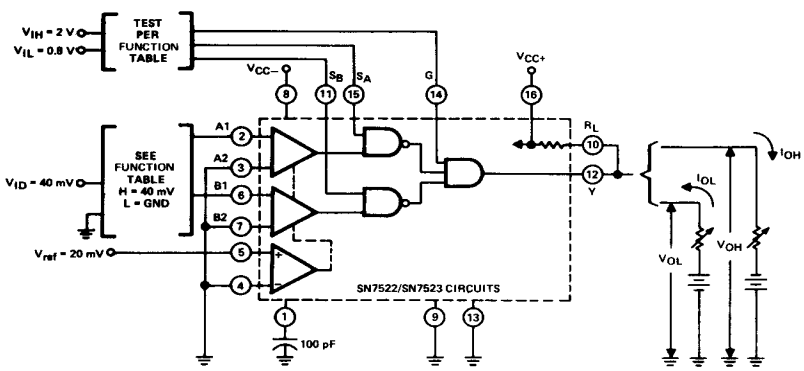


FIGURE 8–V_{IH}, V_{IL}, V_{OH}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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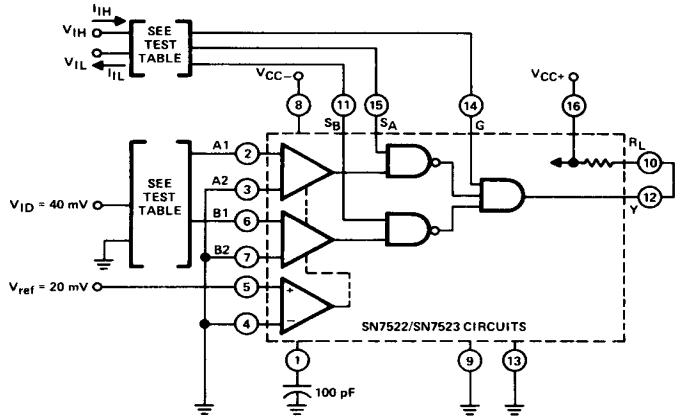
d-c test circuits† (continued)



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IH}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IH}
I_{IH} at GATE	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IH}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IH}
I_{IL} at GATE	GND	GND	V_{IL}	V_{IL}	V_{IL}

FIGURE 9–I_{IH}, I_{IL}

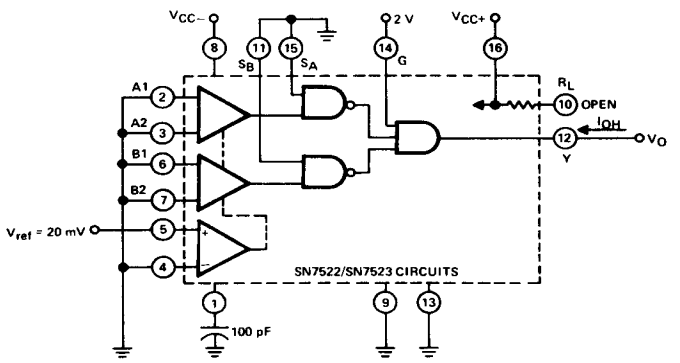


FIGURE 10–I_{OH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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d-c test circuits† (continued)

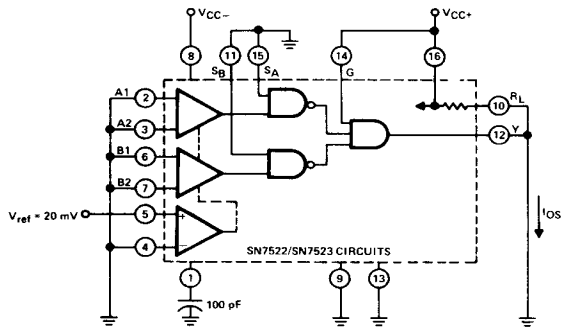
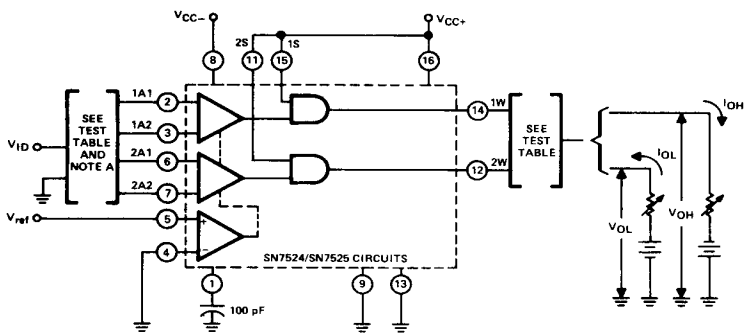


FIGURE 11–I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7524	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
SN7525	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 12–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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d-c test circuits† (continued)

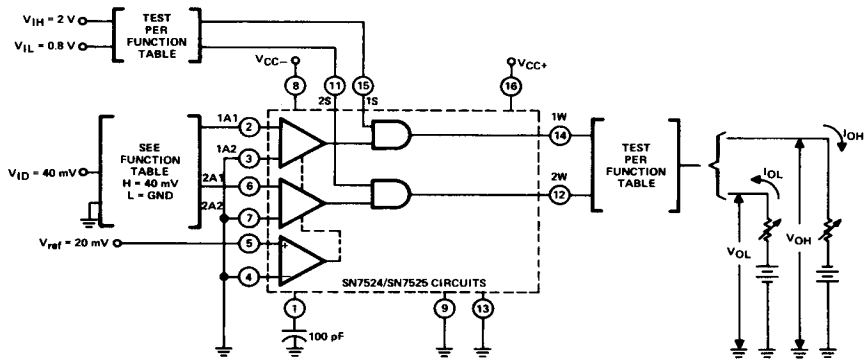
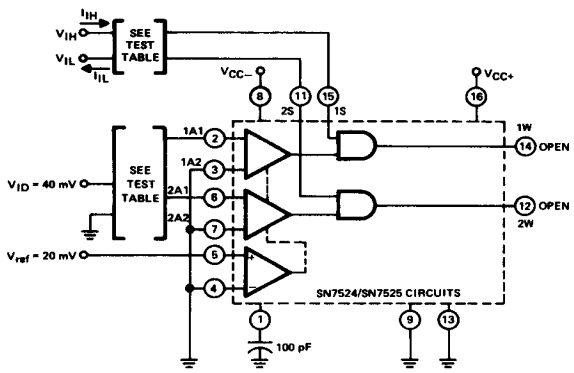


FIGURE 13–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 14–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

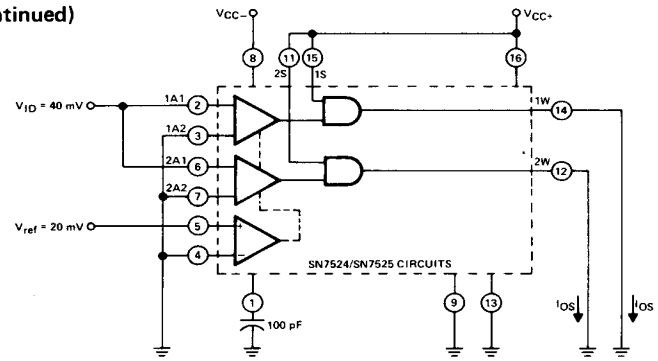
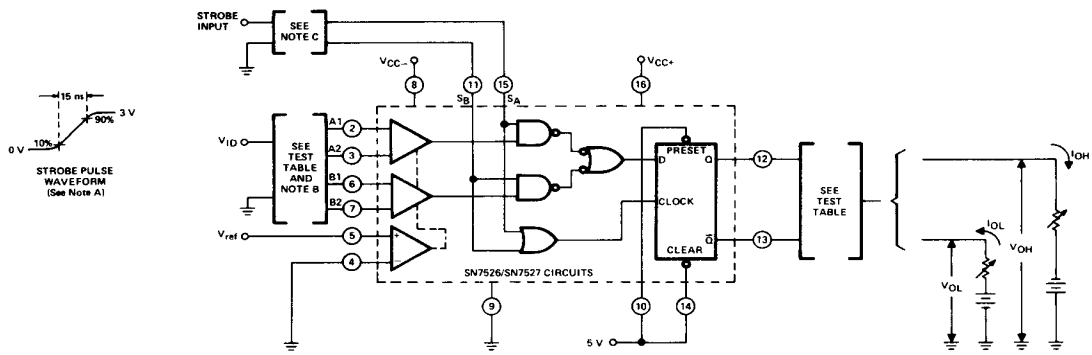


FIGURE 15—I_{OS}



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Q			OUTPUT $\bar{Q}$		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN7526	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
SN7527	A1-A2 or B1-B2	15 mV	≤ 8 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	15 mV	≥22 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≤33 mV	≤0.4 V		16 mA	≥2.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≥47 mV	≥2.4 V	−400 μA		≤0.4 V	−400 μA	

NOTES: A. The strobe input pulse is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_w = 500 ns, PRR = 1 MHz.
B. Each pair of differential inputs is tested separately with the other pair grounded.
C. Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested and to Strobe B when inputs B1-B2 are being tested. In each case, the other strobe input is grounded.

FIGURE 16—V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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d-c test circuits† (continued)

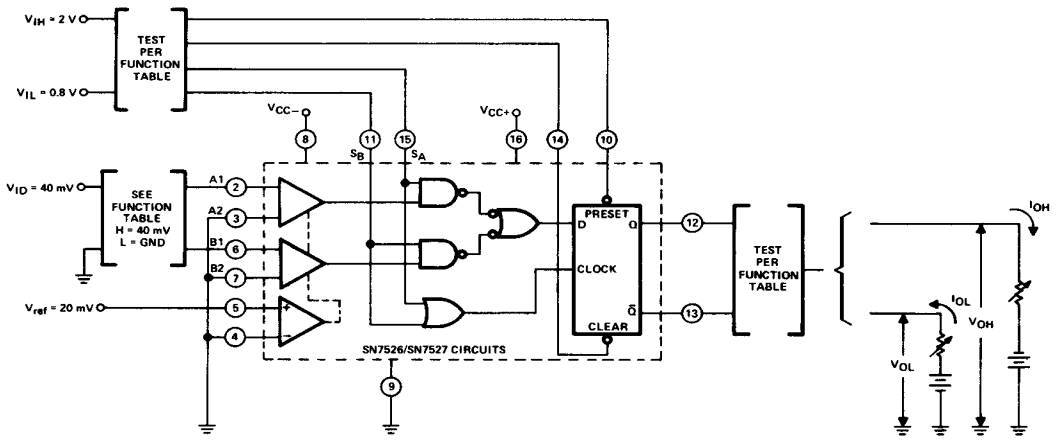
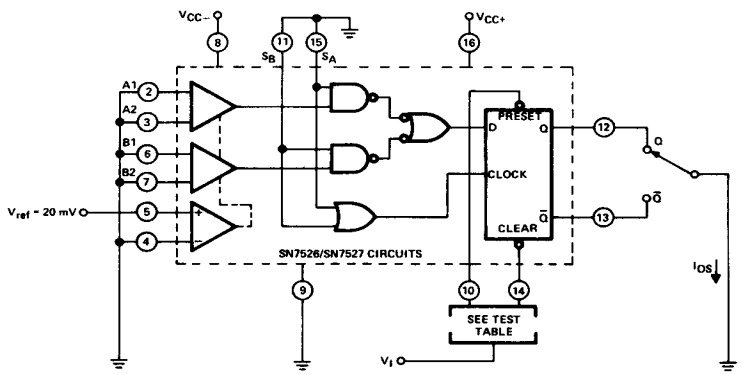


FIGURE 17–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

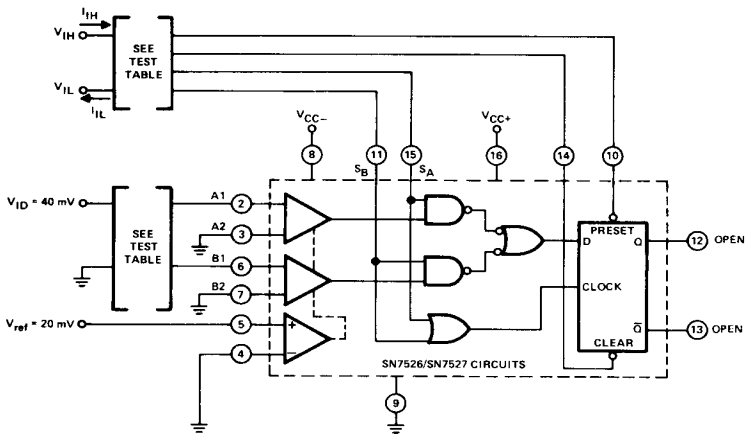
PARAMETER	PRESET	CLEAR
I_{OS} at OUTPUT Q	V_{IL}	V_{IH}
I_{OS} at OUTPUT $\bar{Q}$	V_{IH}	V_{IL}

FIGURE 18–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

PARAMETER	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	PRESET	CLEAR
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	OPEN	OPEN
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IH} at PRESET	GND	V_{ID}	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IH} at CLEAR	GND	GND	V_{IL}	NOTE B	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IH}	OPEN	OPEN
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IH}	V_{IL}	OPEN	OPEN
I_{IL} at PRESET	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at PRESET	V_{ID}	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at CLEAR	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

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NOTES: A. Each input is tested separately.
B. Momentary ground, then V_{IH}.

FIGURE 19–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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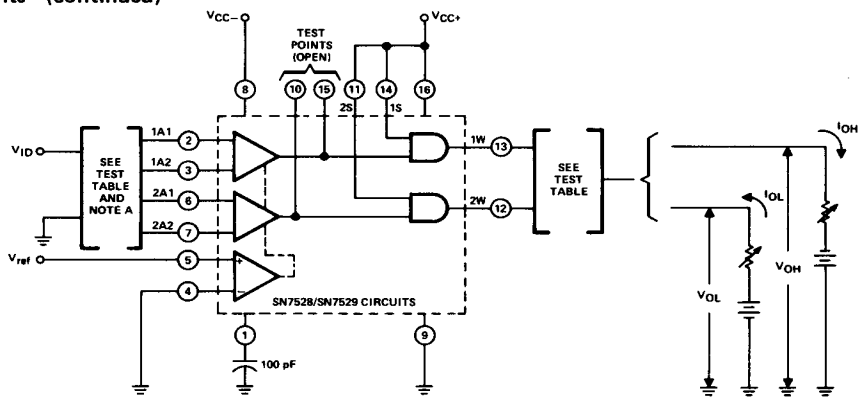
d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN7528	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	
SN7529	A1-A2	15 mV	≤ 8 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥22 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤33 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥47 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 20–V_T

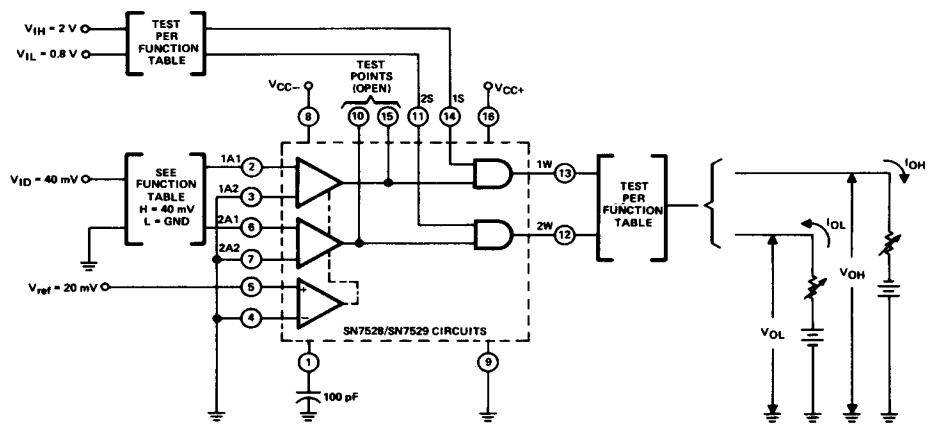


FIGURE 21–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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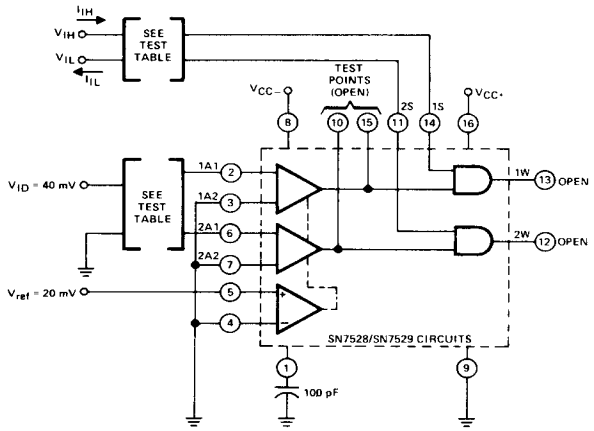
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 22–I_{IH}, I_{IL}

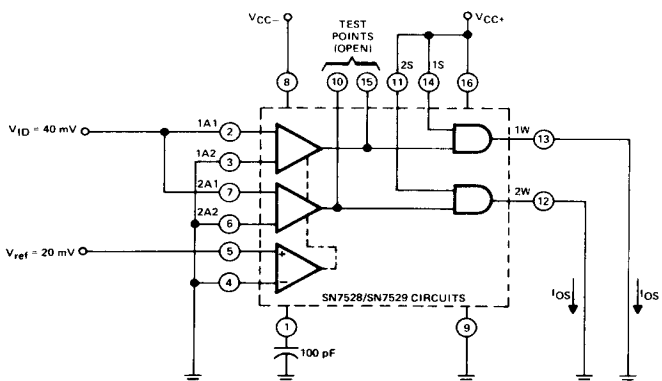


FIGURE 23–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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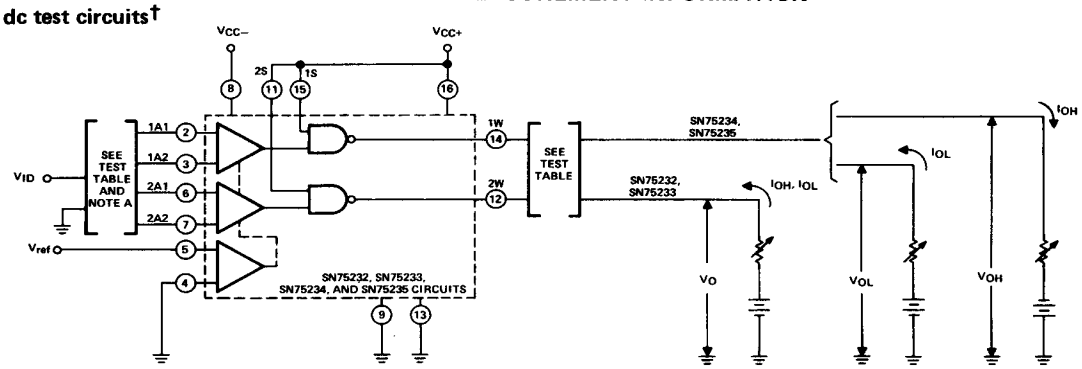
PARAMETER MEASUREMENT INFORMATION

dc test circuits†



CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS					
				SN75232, SN75233			SN75234, SN75235		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN75232, SN75234	A1-A2	15 mV	≤11 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤ 0.4 V		16 mA	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤ 0.4 V		16 mA	≤0.4 V		16 mA
SN75233, SN75235	A1-A2	15 mV	≤8 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤ 0.4 V		16 mA	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	5.25 V	≤250 μA		≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤ 0.4 V		16 mA	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 24–V_T

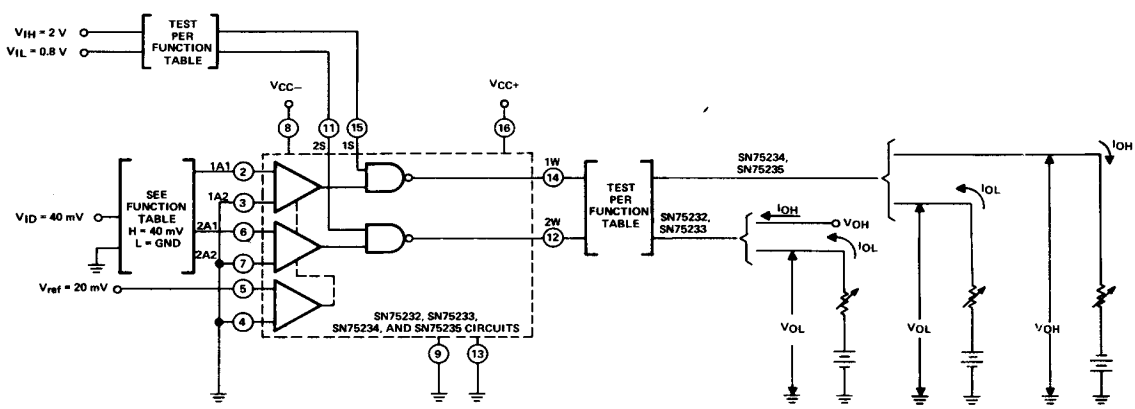


FIGURE 25–V_{IH}, V_{IL}, I_{OH}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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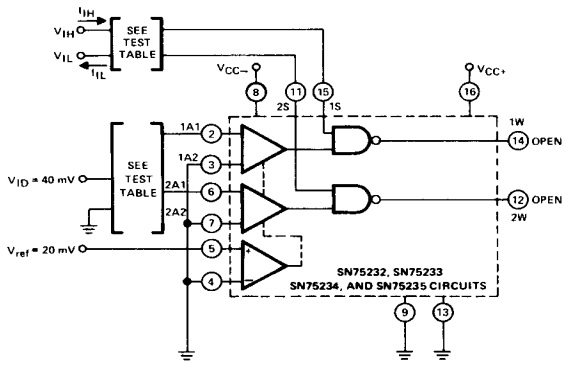
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 26–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

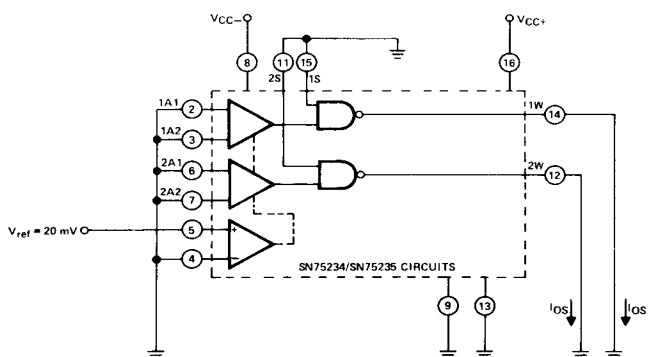


FIGURE 27–I_{OS}

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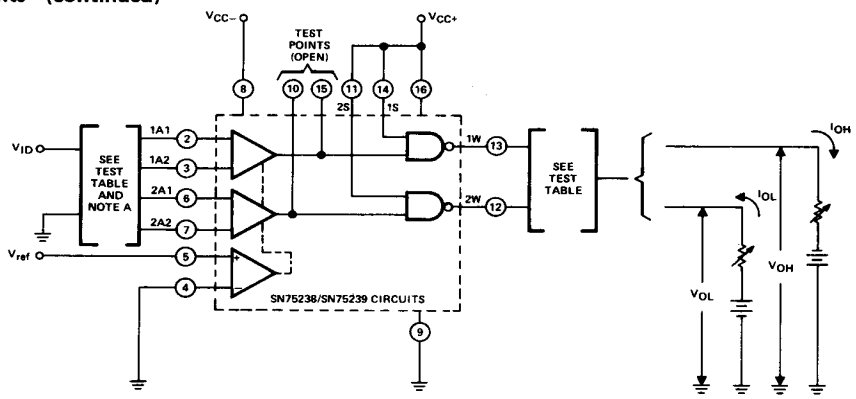
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN75238	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA
SN75239	A1-A2	15 mV	≤ 8 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥22 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤33 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥47 mV	≤0.4 V		16 mA

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 28–V_T

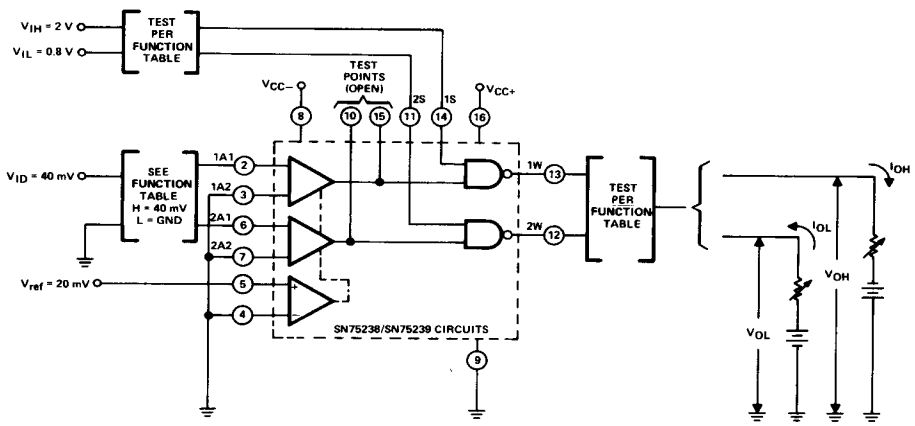
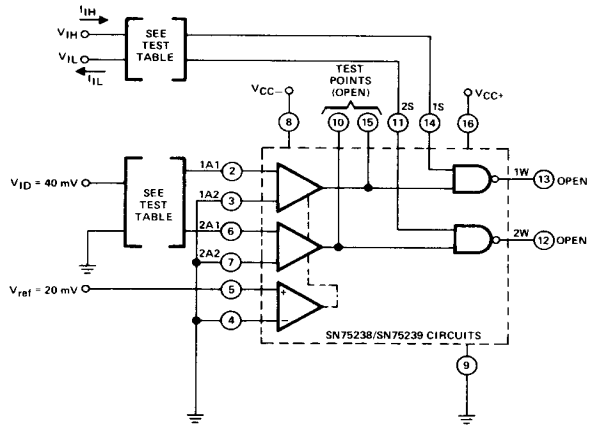


FIGURE 29–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 30–I_{IH}, I_{IL}

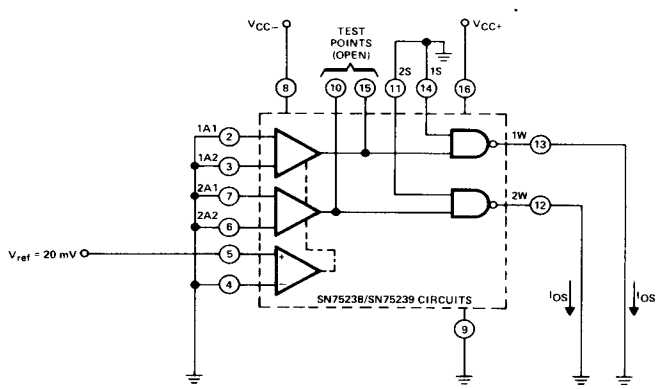


FIGURE 31–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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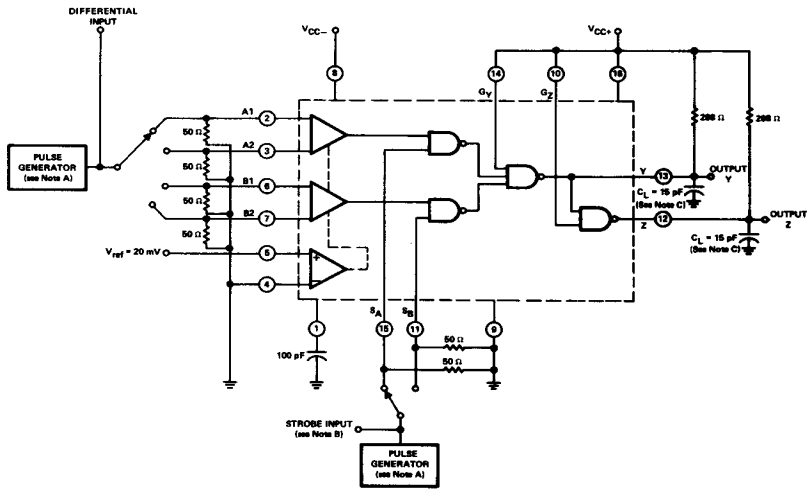
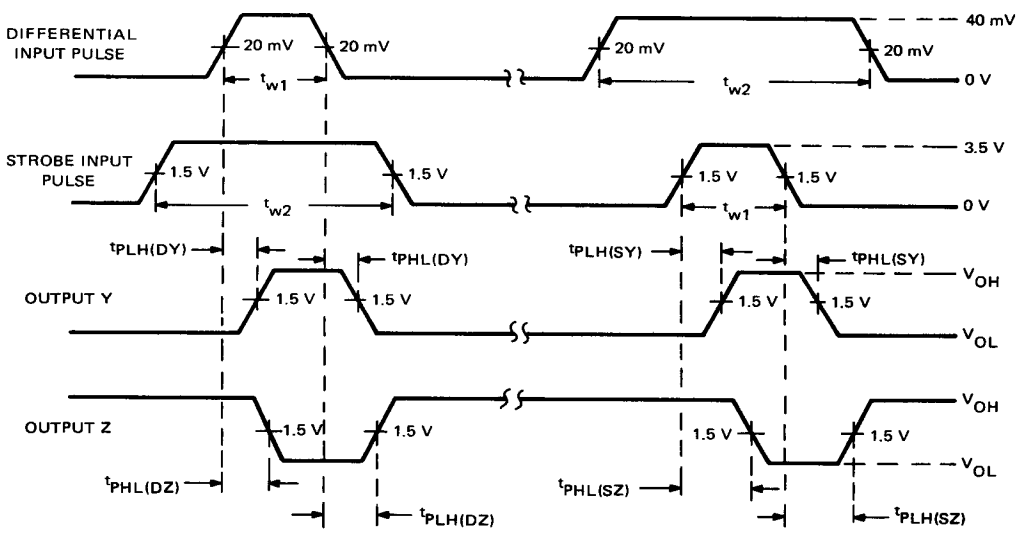
switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.
C. C_L includes probe and jig capacitance.

FIGURE 32—SN7520/SN7521 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

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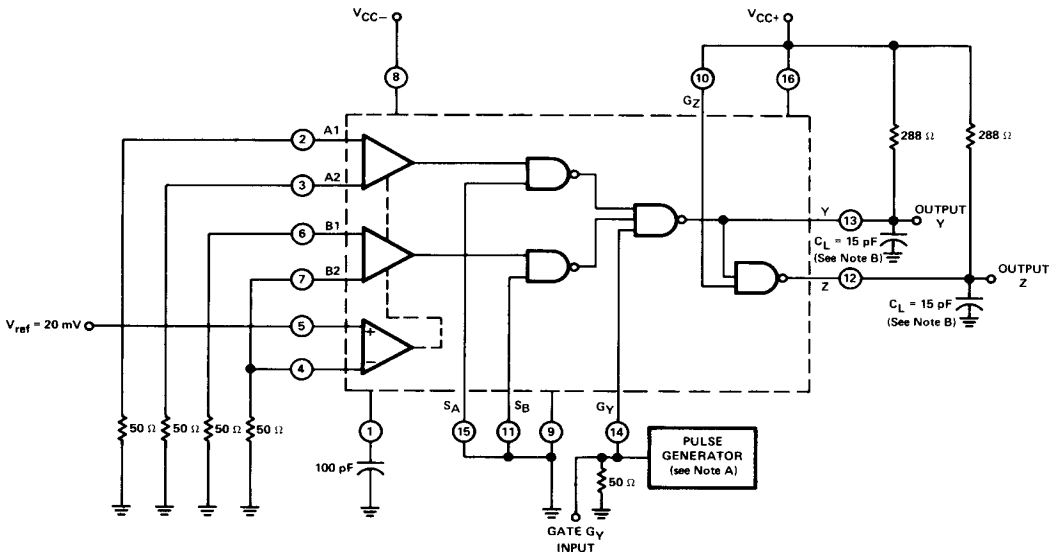
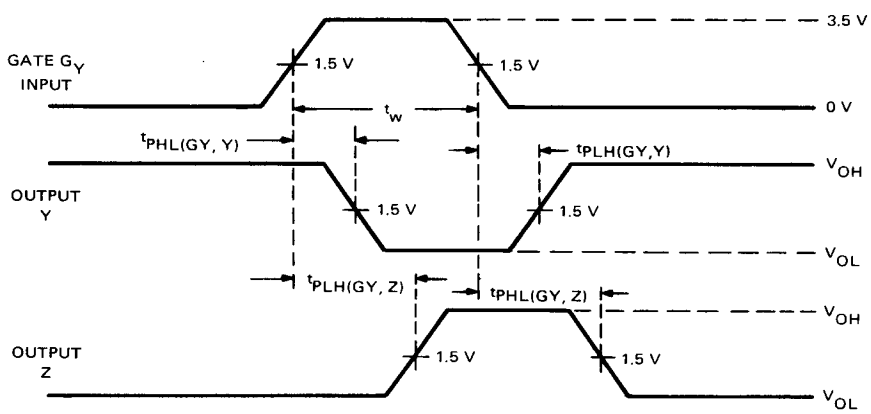
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 33—SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE G_Y

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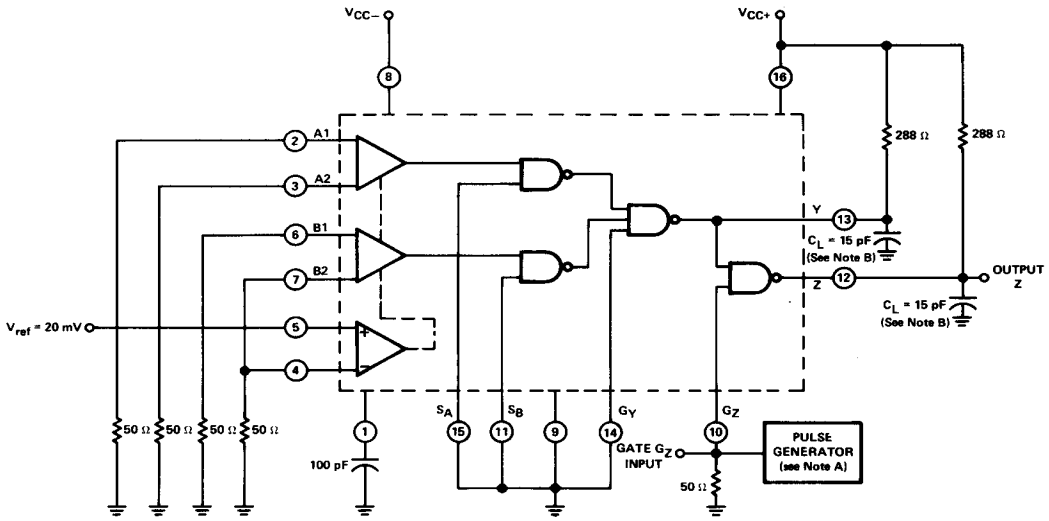
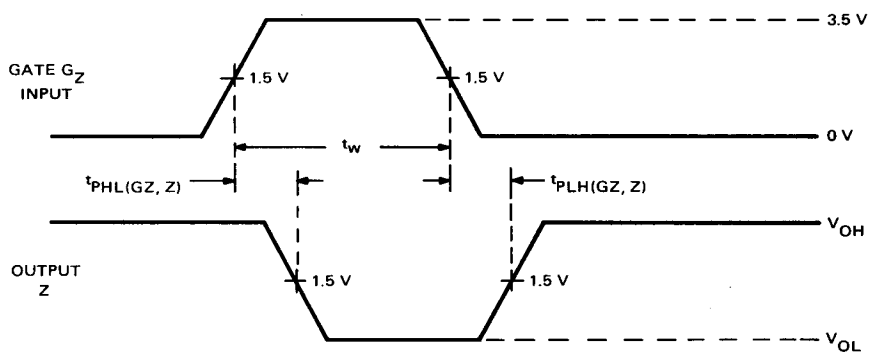
switching characteristics (continued)



TEST CIRCUIT



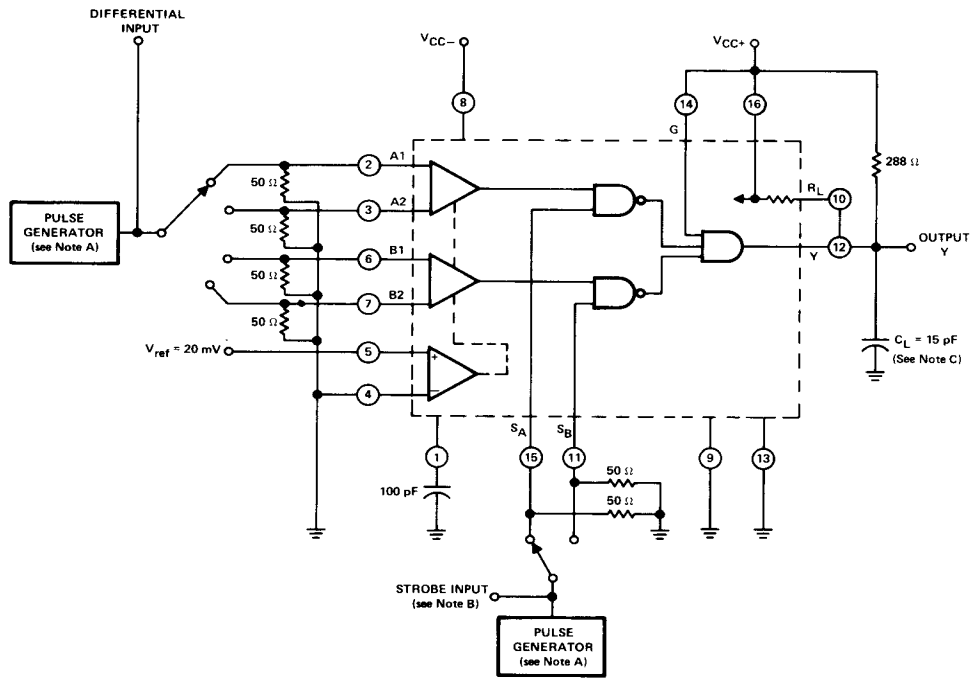
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

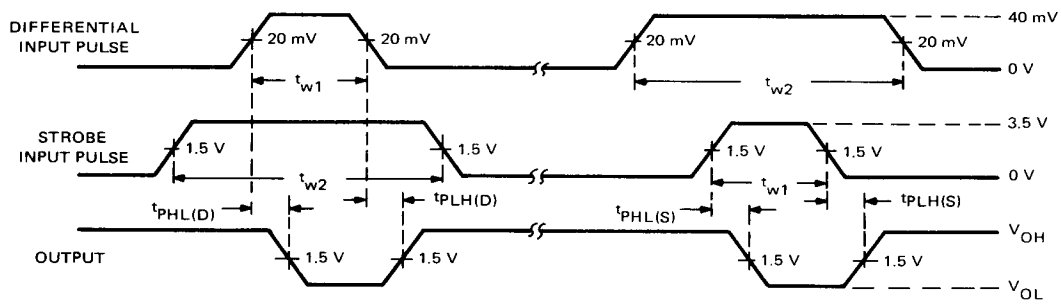
FIGURE 34–SN7520/SN7521 PROPAGATION DELAY TIMES FROM GATE G_Z

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, $t_r = t_f = 15 \pm 5$ ns, $t_{w1} = 100$ ns, $t_{w2} = 300$ ns, PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe S_A when testing inputs A1-A2 and to Strobe S_B when testing inputs B1-B2.
C. C_L includes probe and jig capacitance.

FIGURE 35–SN7522/SN7523 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

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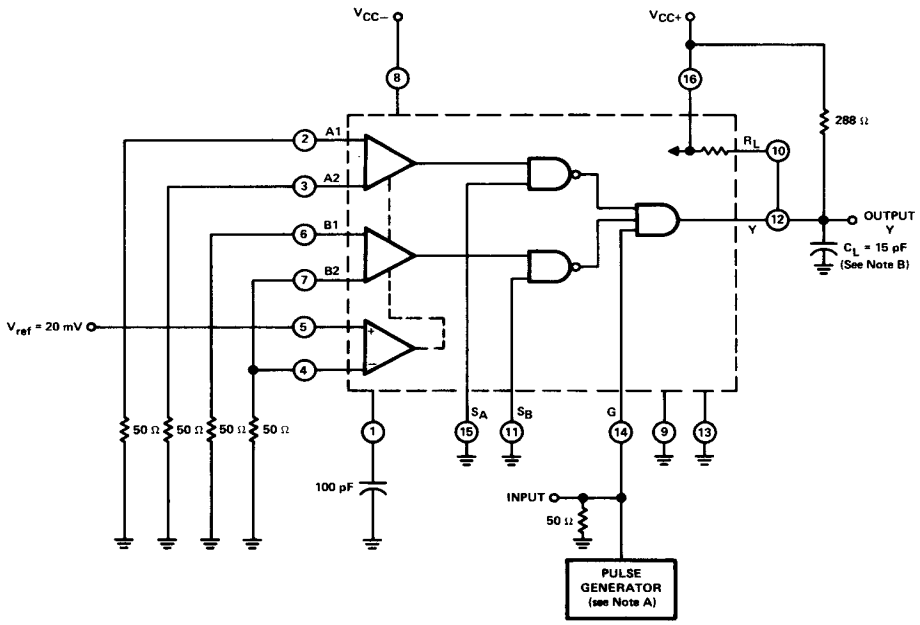
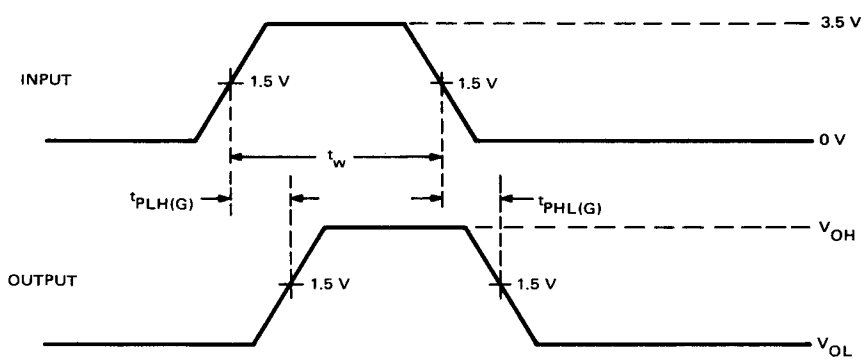
switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_r = 15 \pm 5$ ns, $t_f = 15 \pm 5$ ns, $t_w = 100$ ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 36–SN7522/SN7523 PROPAGATION DELAY TIMES FROM GATE INPUT

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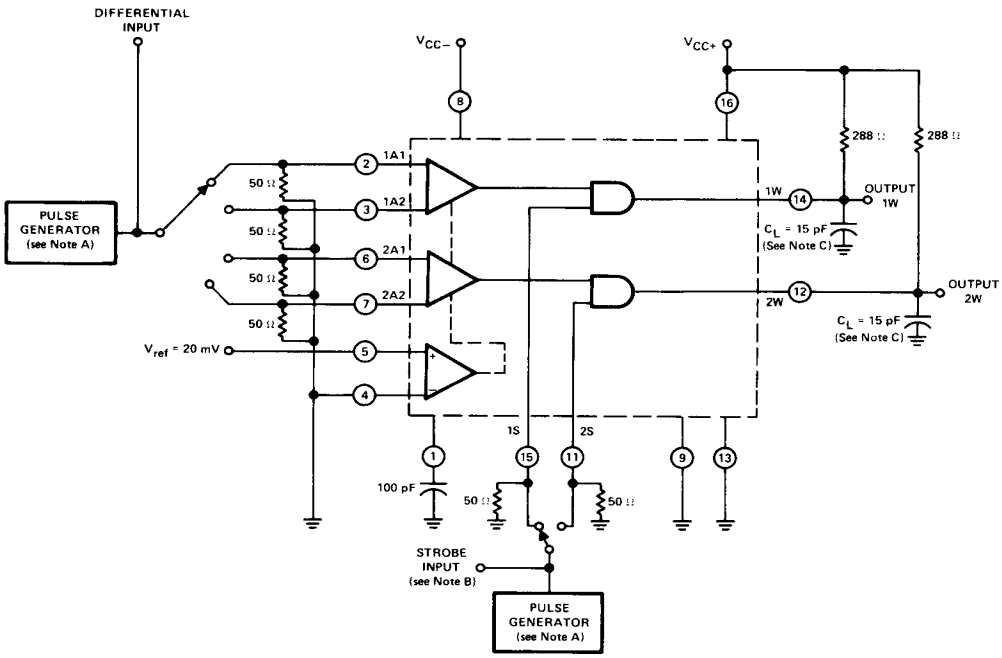
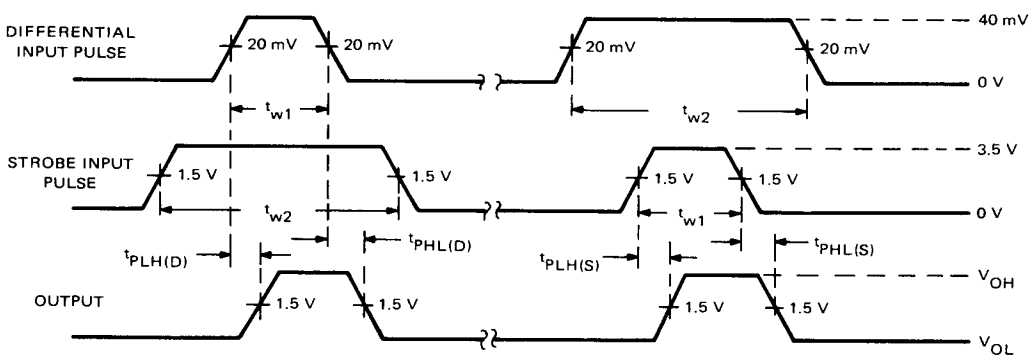
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
C. C_L includes probe and jig capacitance.

FIGURE 37–SN7524/SN7525 PROPAGATION DELAY TIMES

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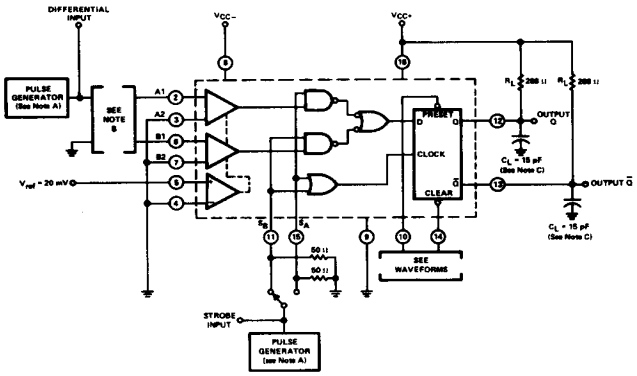
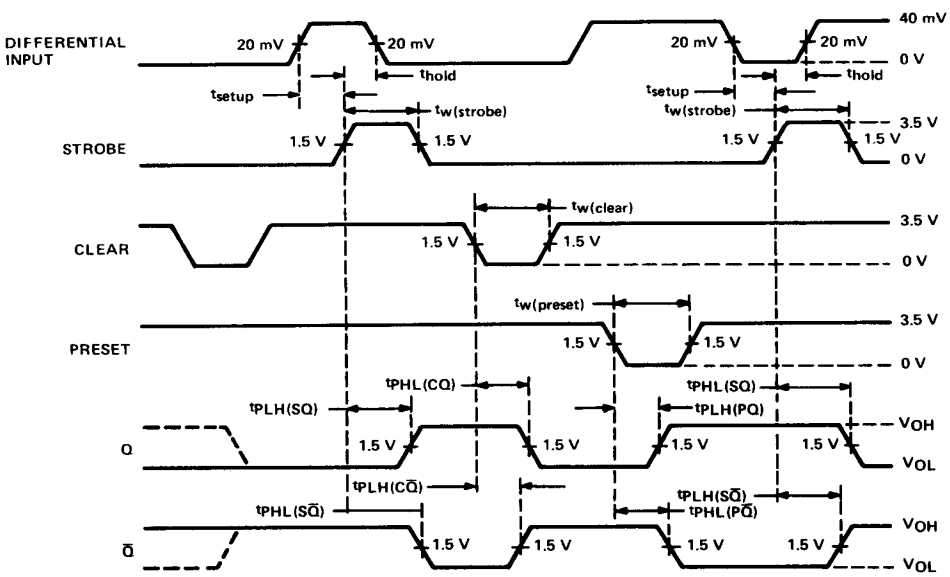
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_W = 50 ns, and PRR = 1 MHz.
B. Each preamplifier is tested separately. Apply 40-mV pulse to input A1 when testing Strobe S_A and to B1 when testing Strobe S_B.
C. C_L includes probe and jig capacitance.

FIGURE 38—SN7526/SN7527 PROPAGATION DELAY TIMES

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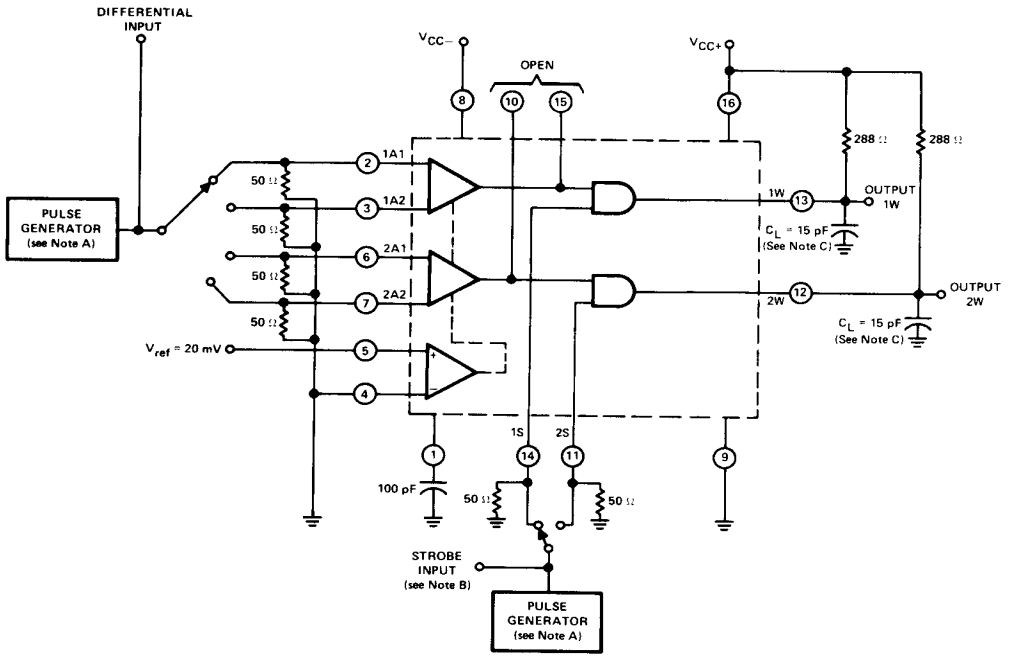
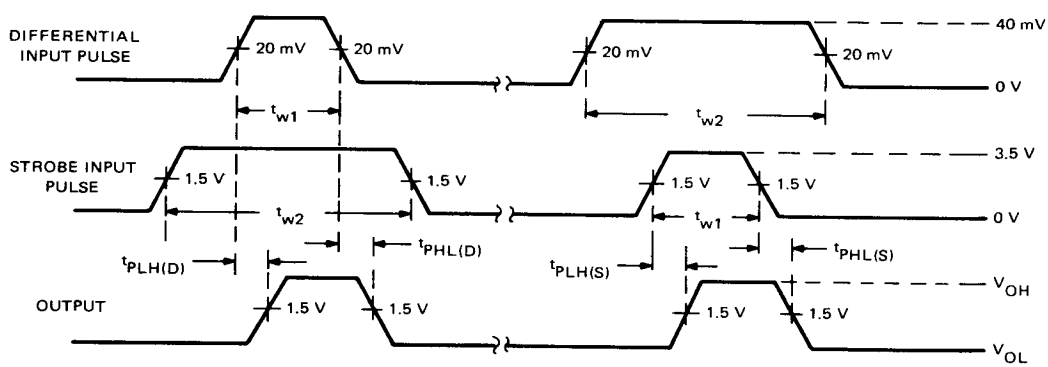
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.
C. C_L includes probe and jig capacitance.

FIGURE 39—SN7528/SN7529 PROPAGATION DELAY TIMES

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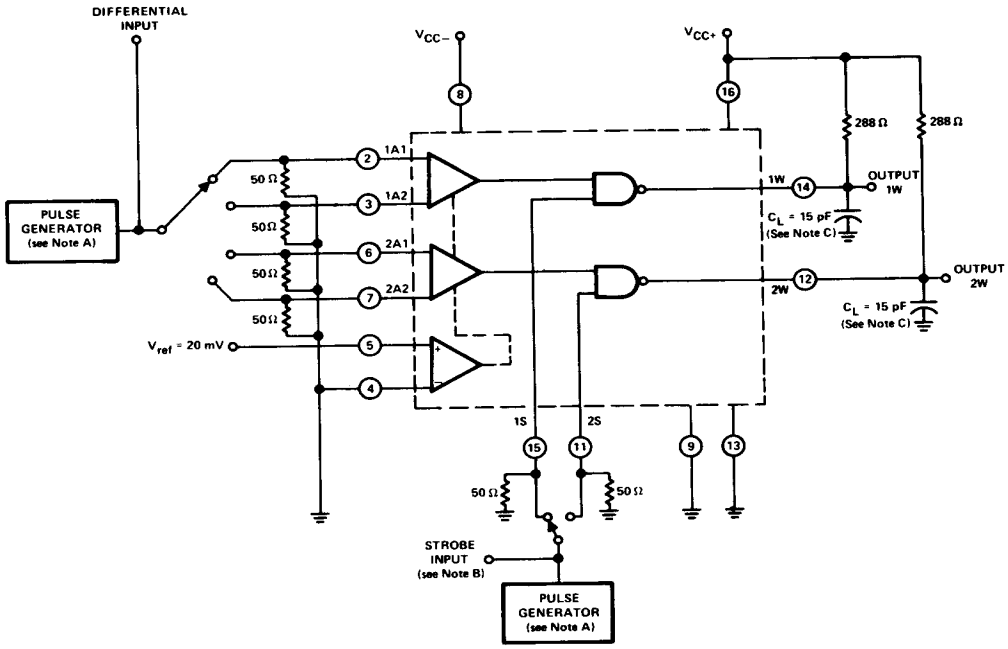
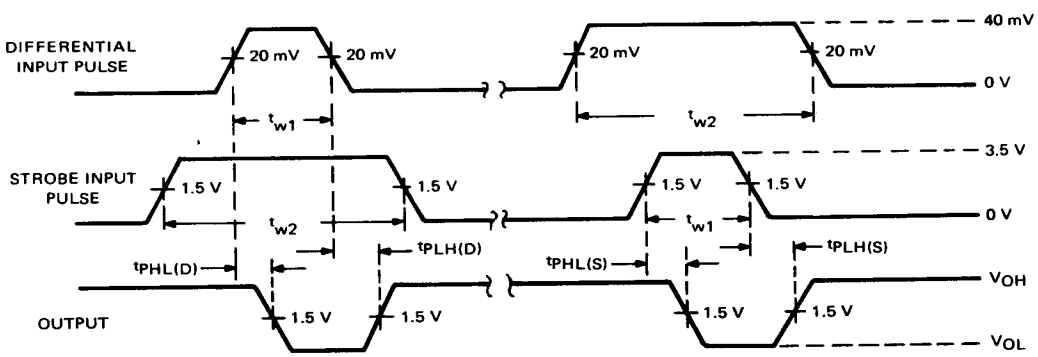
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



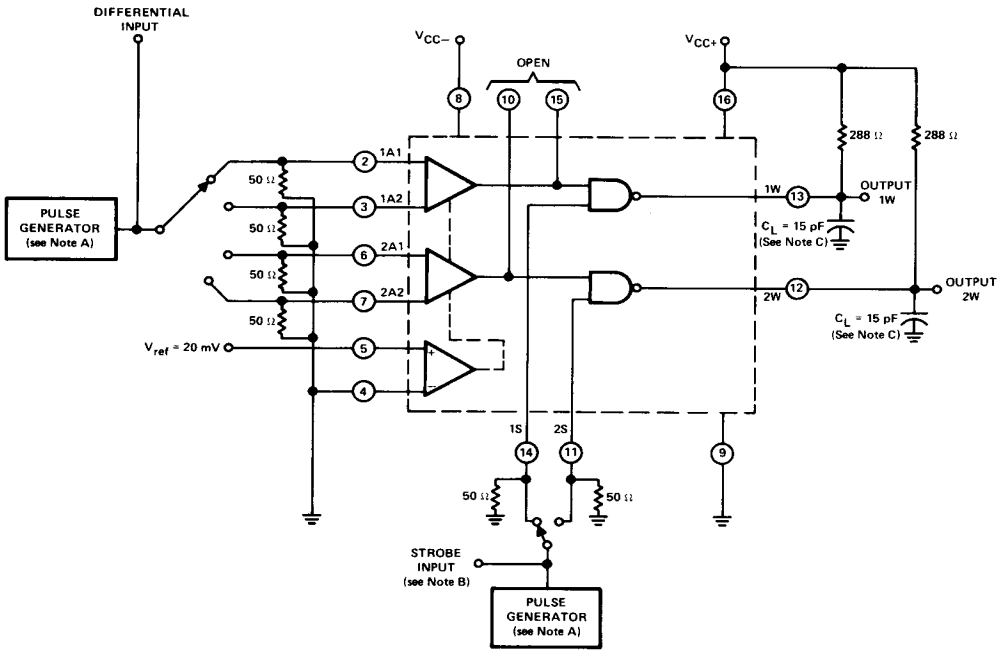
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
C. C_L includes probe and jig capacitance.

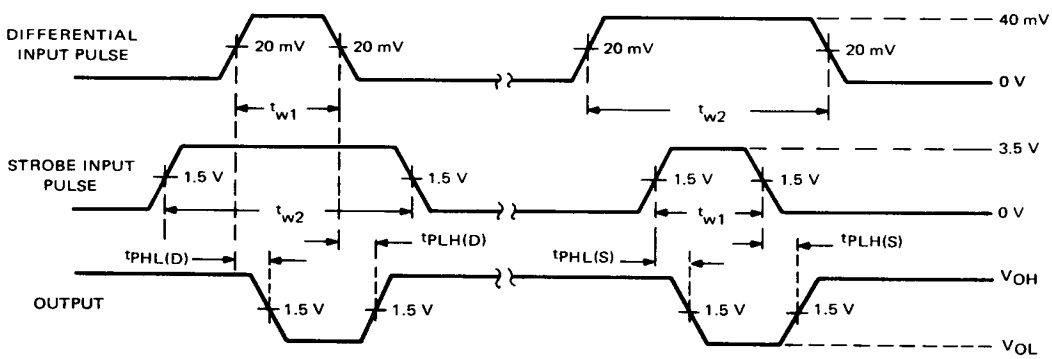
FIGURE 40—SN75232, SN75233, SN75234, and SN75235 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 41—SN75238/SN75239 PROPAGATION DELAY TIMES

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TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
REFERENCE VOLTAGE

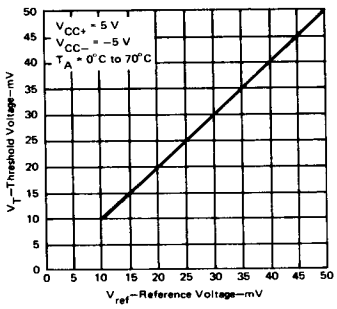

FIGURE 42

THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

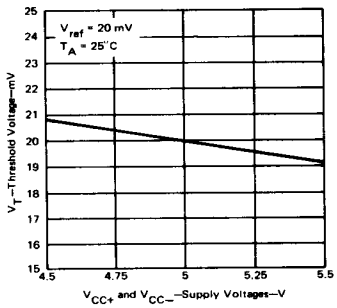

FIGURE 43

NORMALIZED THRESHOLD VOLTAGE
vs
PULSE REPETITION RATE

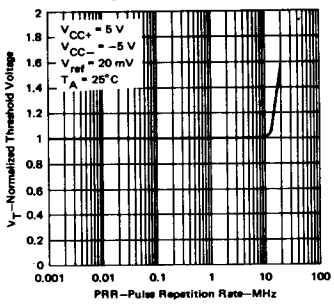

FIGURE 44

COMMON-MODE FIRING VOLTAGE
vs
FREE-AIR TEMPERATURE

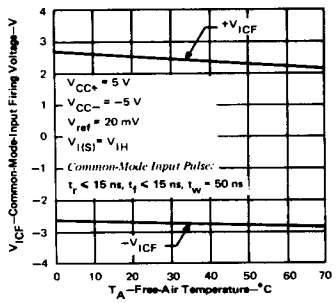

FIGURE 45

DIFFERENTIAL-INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

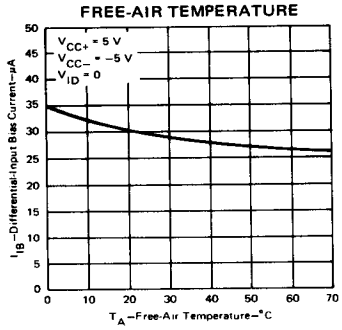

FIGURE 46

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

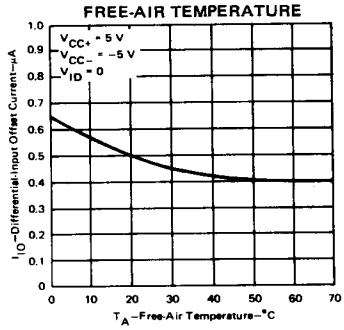

FIGURE 47

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TYPICAL CHARACTERISTICS

HIGH-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

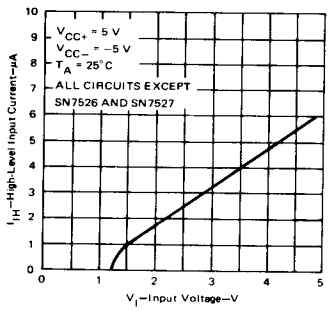

FIGURE 48

LOW-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

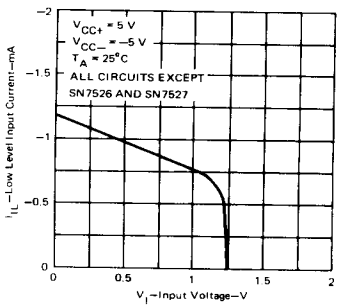

FIGURE 49

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

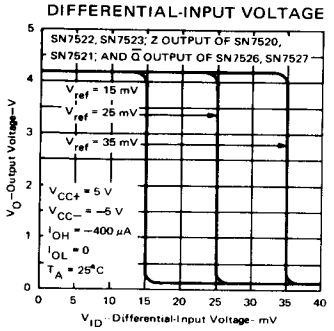

FIGURE 50

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

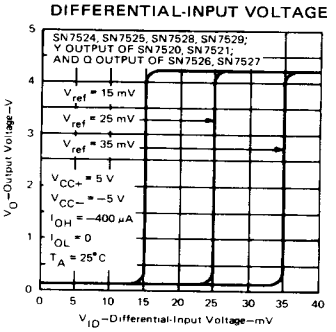

FIGURE 51

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

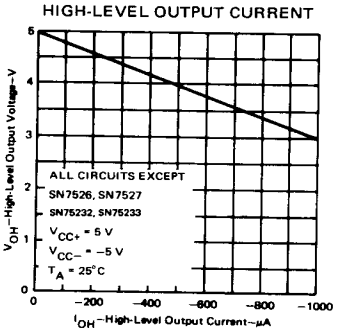

FIGURE 52

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

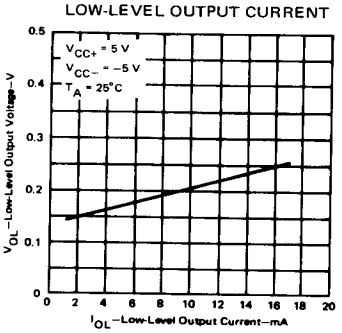

FIGURE 53

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APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54/74 loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54/74 loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the current.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure I)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\,min}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\,min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of TTL loads.

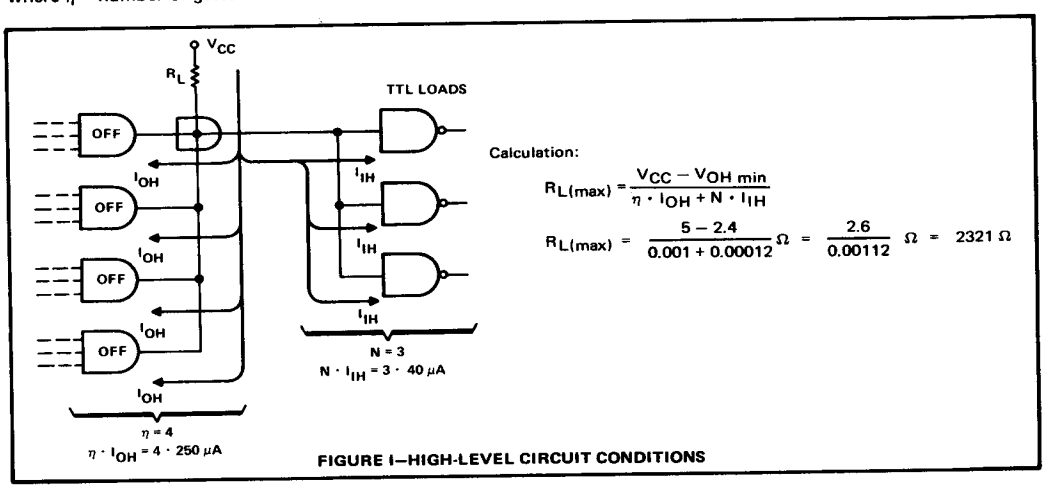

FIGURE I—HIGH-LEVEL CIRCUIT CONDITIONS

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APPLICATION DATA

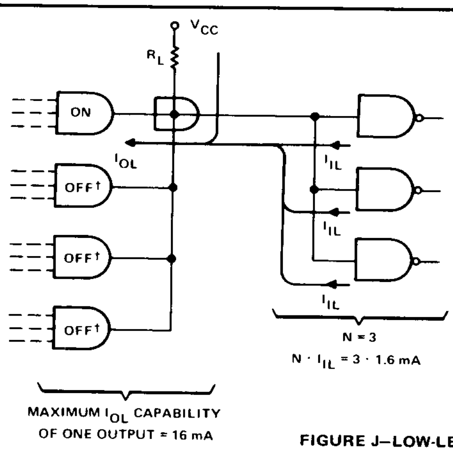
low-level (on-state) circuit calculations (see figure J)

The current through the resistor must be limited to the maximum sink-current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 16 mA, the maximum current which will ensure a low-level maximum of 0.4 volt.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL}\ \text{capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL}\ \text{capability} - N \cdot I_{OL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE J—LOW-LEVEL CIRCUIT CONDITIONS

driving series 54/74 loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54/74 loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54/74 loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4-kΩ resistor in this case will satisfy the high-level condition and limit the low level to less than 0.43 volt.

TABLE 1

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3201	2500	2015	1898	1462	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2966	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2738	2166	1793	1528	1333	575
6	5306	3513	2628	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1698	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

‡—All values shown in the table are based on:
High-level conditions: $V_{CC} = 5\ V$, $V_{OH\ min} = 2.4\ V$
Low-level conditions: $V_{CC} = 5\ V$, $V_{OL\ max} = 0.4\ V$
X—Not recommended or not possible.
§—The theoretical value is ∞. See explanation in text.

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TYPICAL APPLICATIONS

small memory systems

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel SN7524 or SN7525 sense amplifiers, see Figure K. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

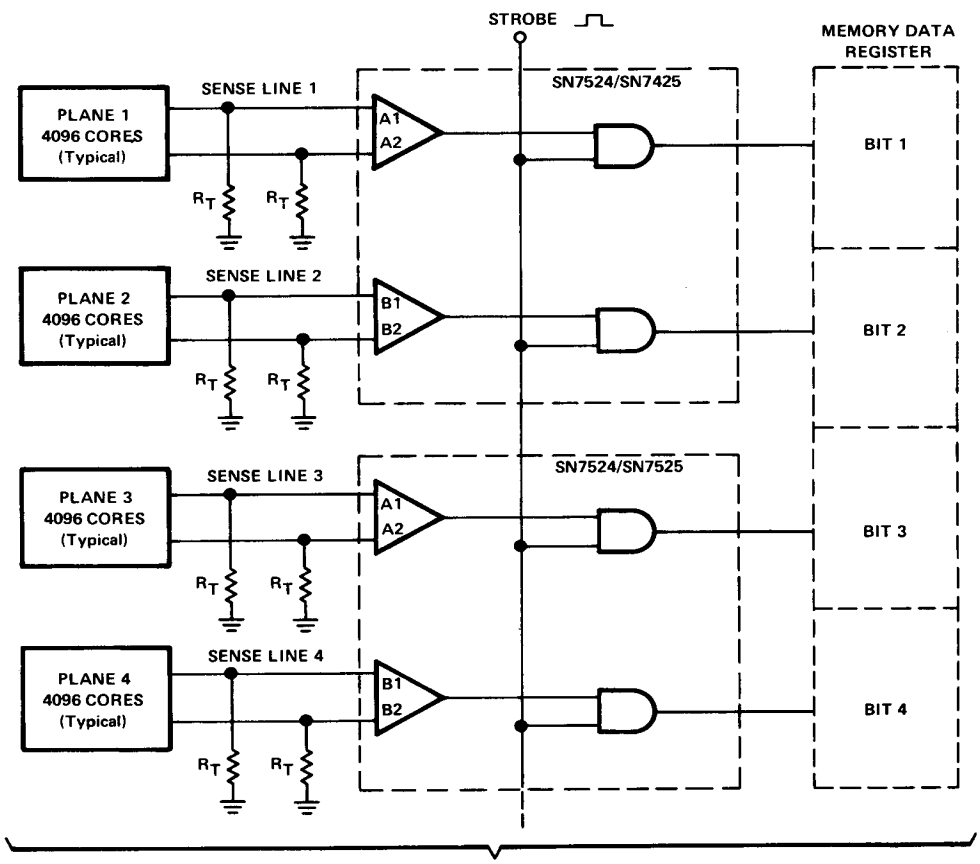

FIGURE K–SENSING SMALL MEMORY SYSTEMS

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TYPICAL APPLICATIONS (continued)

large memory systems

This application demonstrates an improved method of sensing data from large memory systems. The signal-to-noise ratio can be increased by sectioning the large core planes as illustrated in Figure L. Two segments, usually consisting of 4096 cores each, can be interfaced by each of the dual-input channels of the SN7420/SN7421 or SN7422/SN7423 sense amplifiers. The cascaded output gates of the SN7520/SN7521 circuits may be connected to serve as the memory data register (MDR). A number of SN7522/SN7523 sense amplifiers may be wire-AND connected to expand the input function of the MDR to interface all the segments of the plane. Complementary outputs, clear, and preset functions are provided for the MDR. Rules for combined fan-out and wire-AND capabilities must be observed.

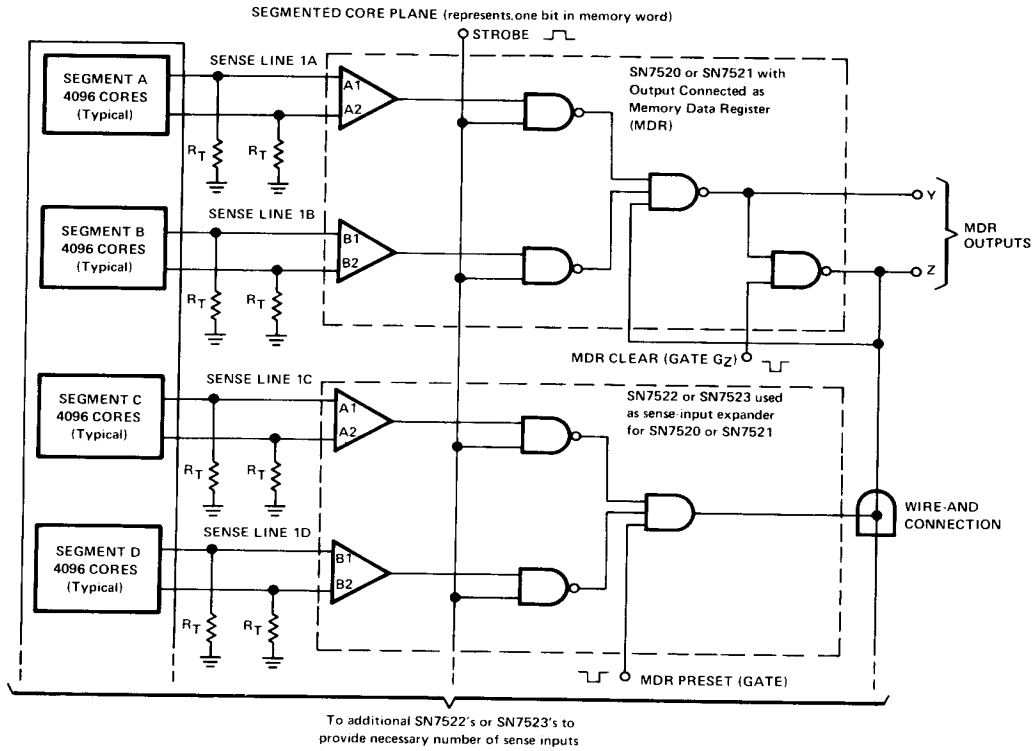

FIGURE L—SENSING LARGE MEMORY SYSTEMS

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