

LF147/LF347

Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

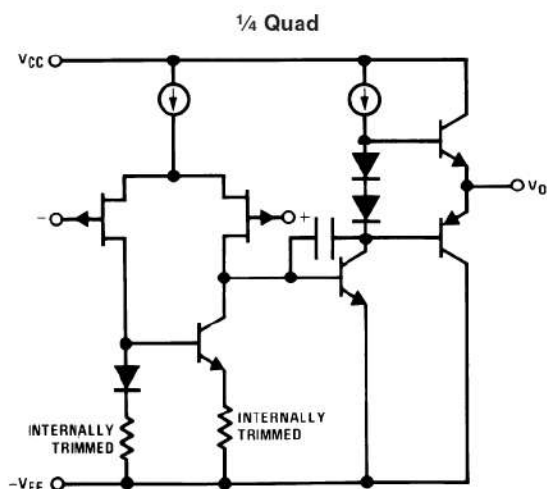
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

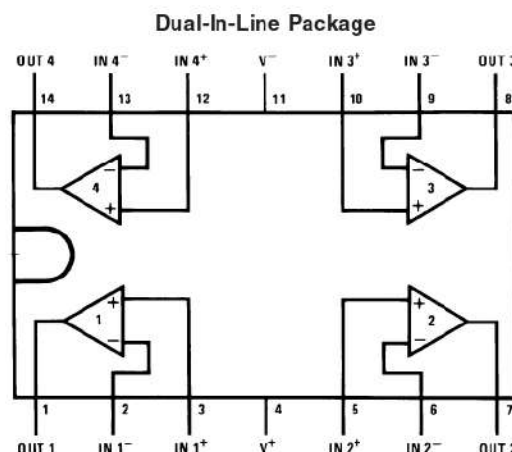
- Internally trimmed offset voltage: 5 mV max
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/μs
- Low supply current: 7.2 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion: $\leq 0.02\%$
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

Simplified Schematic



00564713

Connection Diagram



00564701

Note 1: LF147 available as per JM38510/11906.

Top View

Order Number LF147J, LF147J-SMD, LF347M,
LF347BN, LF347N, LF147J/883,
or JL147 BCA (Note 1)
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 3)	±19V	±15V
Output Short Circuit Duration (Note 4)	Continuous	Continuous
Power Dissipation (Notes 5, 11)	900 mW	1000 mW
T _J max	150°C	150°C
θ _{JA}		
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W

Operating Temperature
Range

Storage Temperature
Range

Lead Temperature

(Soldering, 10 sec.)

Soldering Information

Dual-In-Line Package

Soldering (10 seconds)

Small Outline Package

Vapor Phase (60 seconds)

Infrared (15 seconds)

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 12)

LF147 LF347B/LF347

(Note 6) (Note 6)

–65°C ≤ T_A ≤ 150°C

260°C 260°C

260°C

215°C

220°C

900V

DC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OS}	Input Offset Voltage	R _S =10 kΩ, T _A =25°C Over Temperature		1	5 8		3	5 7		5	10 13	mV mV
ΔV _{OS} /ΔT	Average TC of Input Offset Voltage	R _S =10 kΩ		10			10			10		μV/°C
I _{OS}	Input Offset Current	T _J =25°C, (Notes 7, 8) Over Temperature		25	100 25		25	100 4		25	100 4	pA nA
I _B	Input Bias Current	T _J =25°C, (Notes 7, 8) Over Temperature		50	200 50		50	200 8		50	200 8	pA nA
R _{IN}	Input Resistance	T _J =25°C		10 ¹²			10 ¹²			10 ¹²		Ω
A _{VOL}	Large Signal Voltage Gain	V _S =±15V, T _A =25°C V _O =±10V, R _L =2 kΩ Over Temperature	50	100		50	100		25	100		V/mV V/mV
V _O	Output Voltage Swing	V _S =±15V, R _L =10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V _{CM}	Input Common-Mode Voltage Range	V _S =±15V	±11	+15 –12		±11	+15 –12		±11	+15 –12		V V
CMRR	Common-Mode Rejection Ratio	R _S ≤10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)	80	100		80	100		70	100		dB
I _S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A=25^{\circ}\text{C}$, $f=1\text{ Hz}-20\text{ kHz}$ (Input Referred)		-120			-120			-120		dB
SR	Slew Rate	$V_S=\pm 15\text{V}$, $T_A=25^{\circ}\text{C}$	8	13		8	13		8	13		V/ μs
GBW	Gain-Bandwidth Product	$V_S=\pm 15\text{V}$, $T_A=25^{\circ}\text{C}$	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A=25^{\circ}\text{C}$, $R_S=100\Omega$, $f=1000\text{ Hz}$		20			20			20		nV/ $\sqrt{\text{Hz}}$
i_n	Equivalent Input Noise Current	$T_J=25^{\circ}\text{C}$, $f=1000\text{ Hz}$		0.01			0.01			0.01		pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$A_V=+10$, $R_L=10\text{k}$, $V_O=20\text{ Vp-p}$, $\text{BW}=20\text{ Hz}-20\text{ kHz}$		<0.02			<0.02			<0.02		%

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 5: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} .

Note 6: The LF147 is available in the military temperature range $-55^{\circ}\text{C}\leq T_A\leq 125^{\circ}\text{C}$, while the LF347B and the LF347 are available in the commercial temperature range $0^{\circ}\text{C}\leq T_A\leq 70^{\circ}\text{C}$. Junction temperature can rise to $T_J\text{ max} = 150^{\circ}\text{C}$.

Note 7: Unless otherwise specified the specifications apply over the full temperature range and for $V_S=\pm 20\text{V}$ for the LF147 and for $V_S=\pm 15\text{V}$ for the LF347B/LF347. V_{OS} , I_B , and I_{OS} are measured at $V_{CM}=0$.

Note 8: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J=T_A+\theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

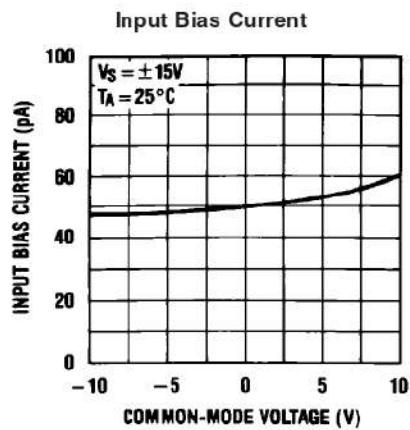
Note 9: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5\text{V}$ to $\pm 15\text{V}$ for the LF347 and LF347B and from $V_S = \pm 20\text{V}$ to $\pm 5\text{V}$ for the LF147.

Note 10: Refer to RETS147X for LF147D and LF147J military specifications.

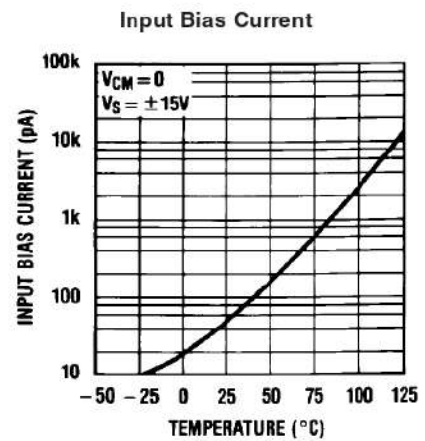
Note 11: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 12: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

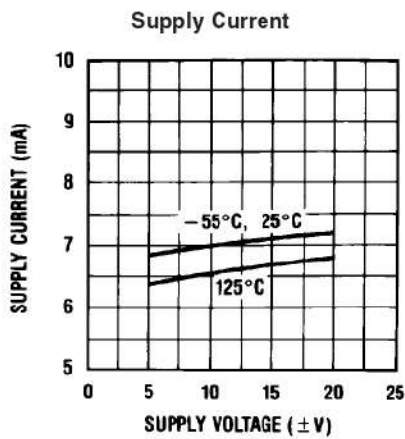
Typical Performance Characteristics



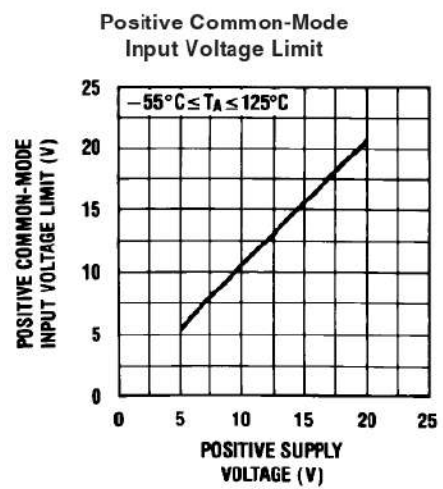
00564714



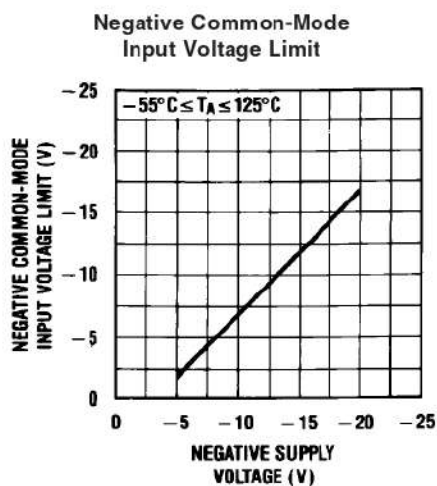
00564715



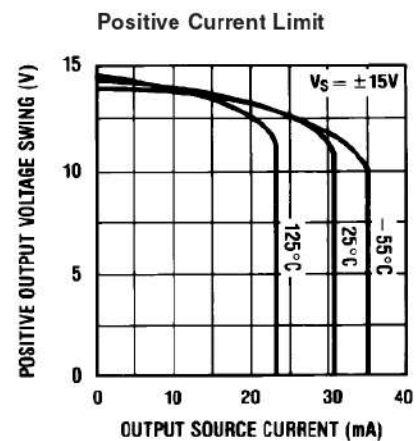
00564716



00564717

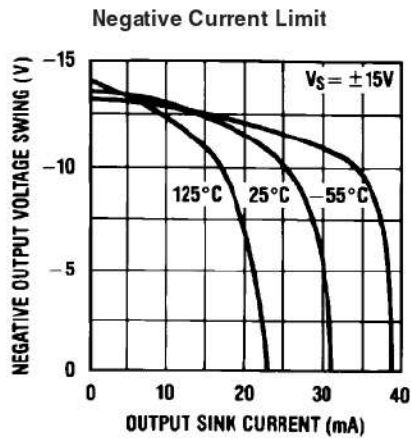


00564718

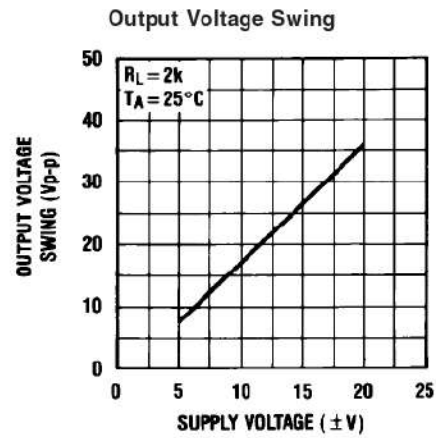


00564719

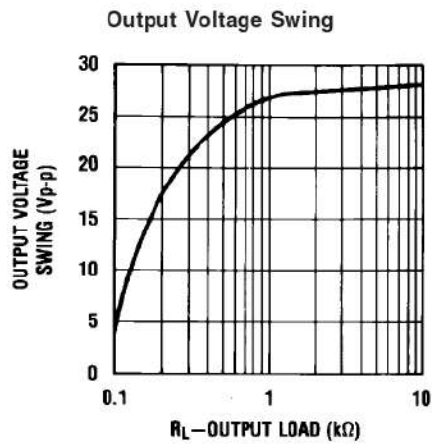
Typical Performance Characteristics (Continued)



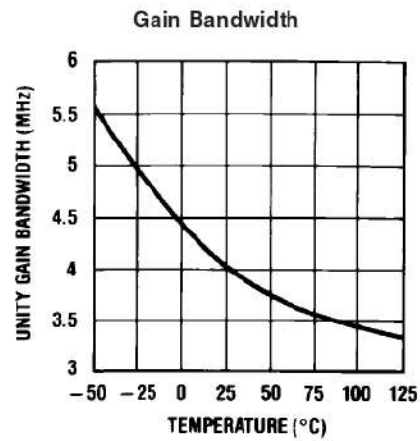
00564720



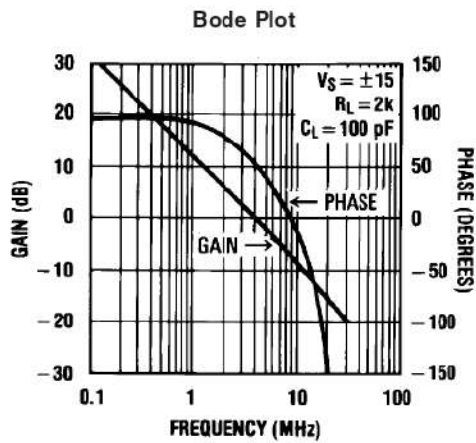
00564721



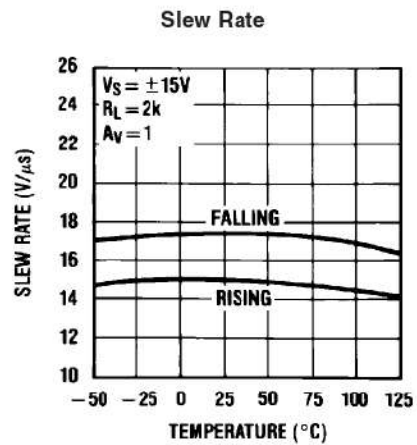
00564722



00564723

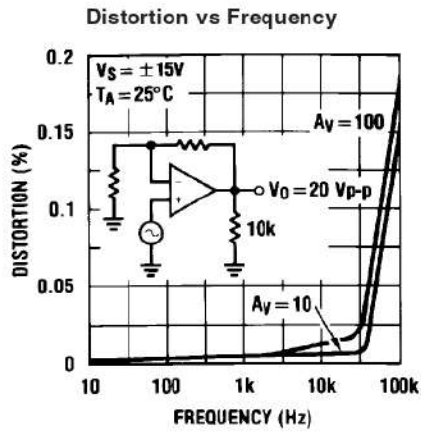


00594724

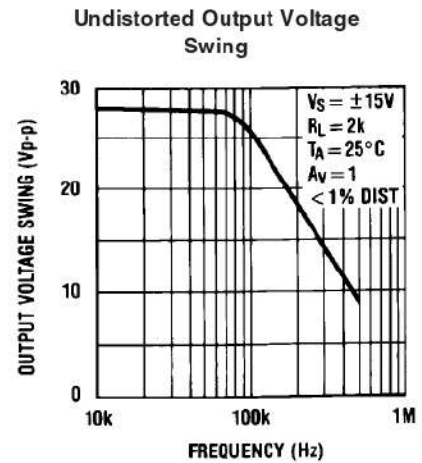


00564725

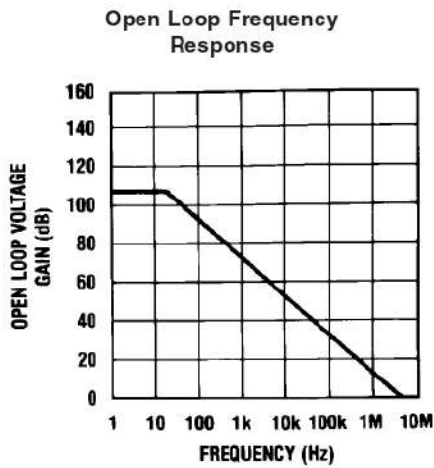
Typical Performance Characteristics (Continued)



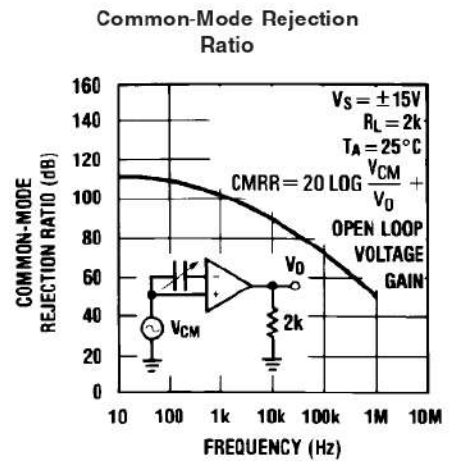
00564726



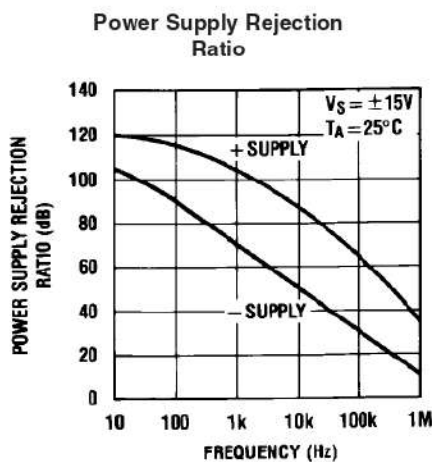
00564727



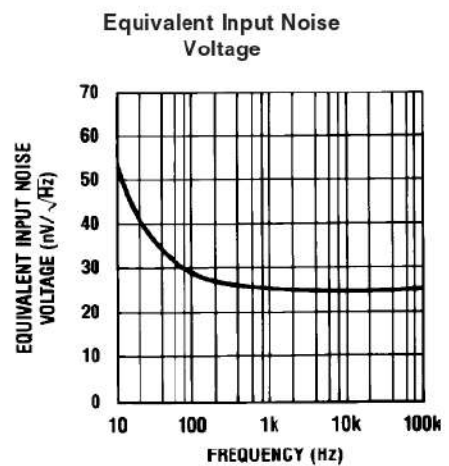
00564728



00564729



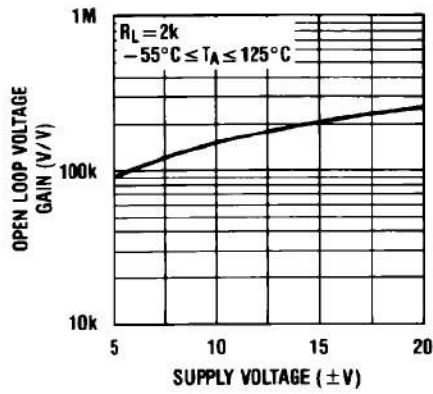
00564730



00564731

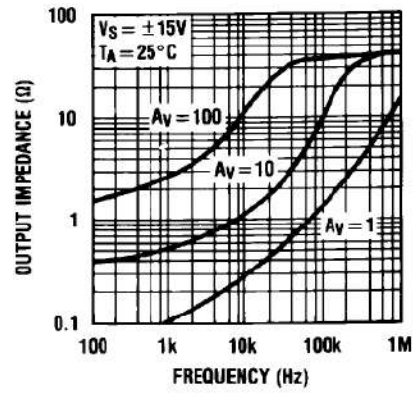
Typical Performance Characteristics (Continued)

Open Loop Voltage Gain



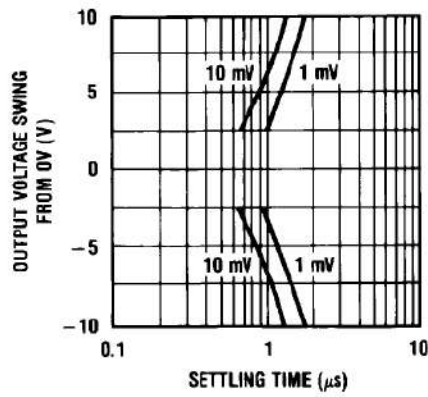
00564732

Output Impedance



00564733

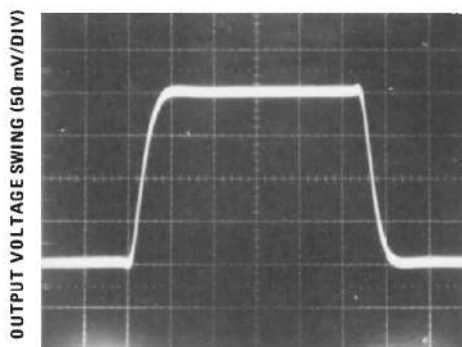
Inverter Settling Time



00564734

Pulse Response $R_L=2\text{ k}\Omega$, $C_L=10\text{ pF}$

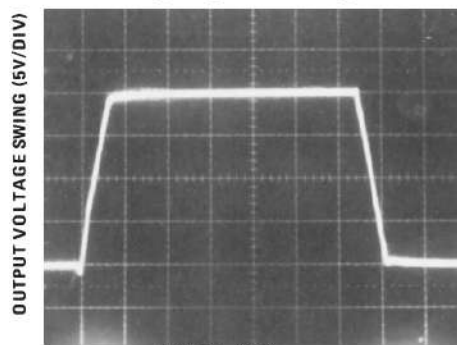
Small Signal Inverting



TIME (0.2 $\mu\text{s/DIV}$)

00564704

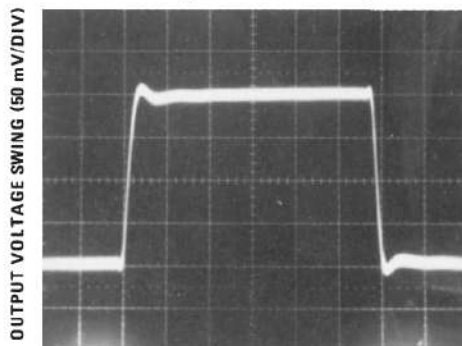
Large Signal Inverting



TIME (2 $\mu\text{s/DIV}$)

00564706

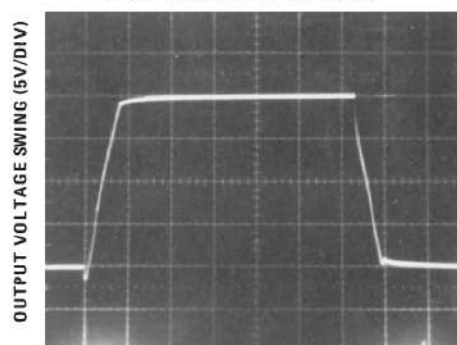
Small Signal Non-Inverting



TIME (0.2 $\mu\text{s/DIV}$)

00564705

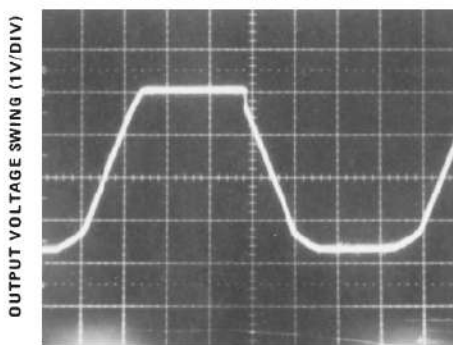
Large Signal Non-Inverting



TIME (2 $\mu\text{s/DIV}$)

00564707

Current Limit ($R_L=100\Omega$)



TIME (5 $\mu\text{s/DIV}$)

00564708

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages

should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 4.5\text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a $2\text{ k}\Omega$ load resistance to $\pm 10\text{V}$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

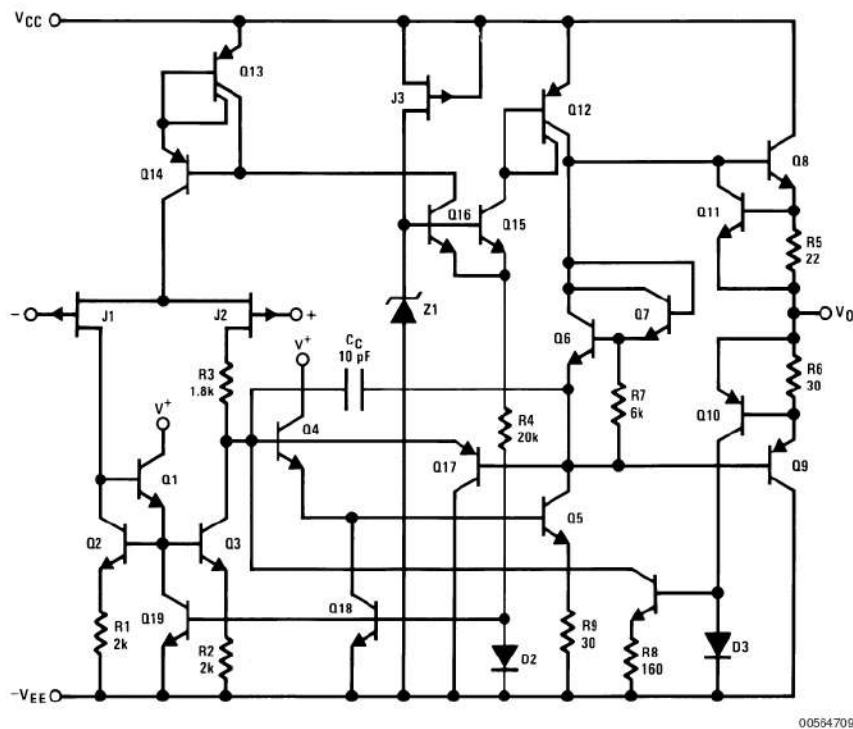
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a

socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

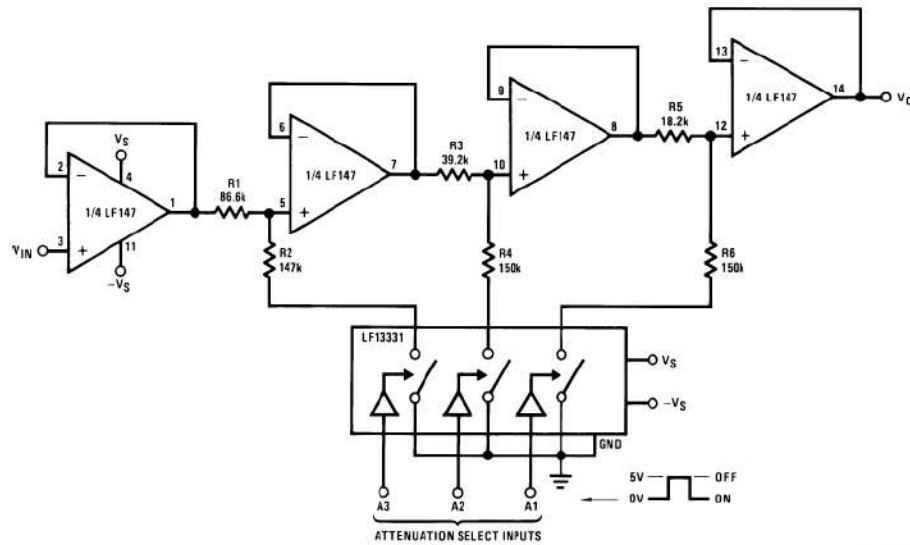
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

Digitally Selectable Precision Attenuator



00564710

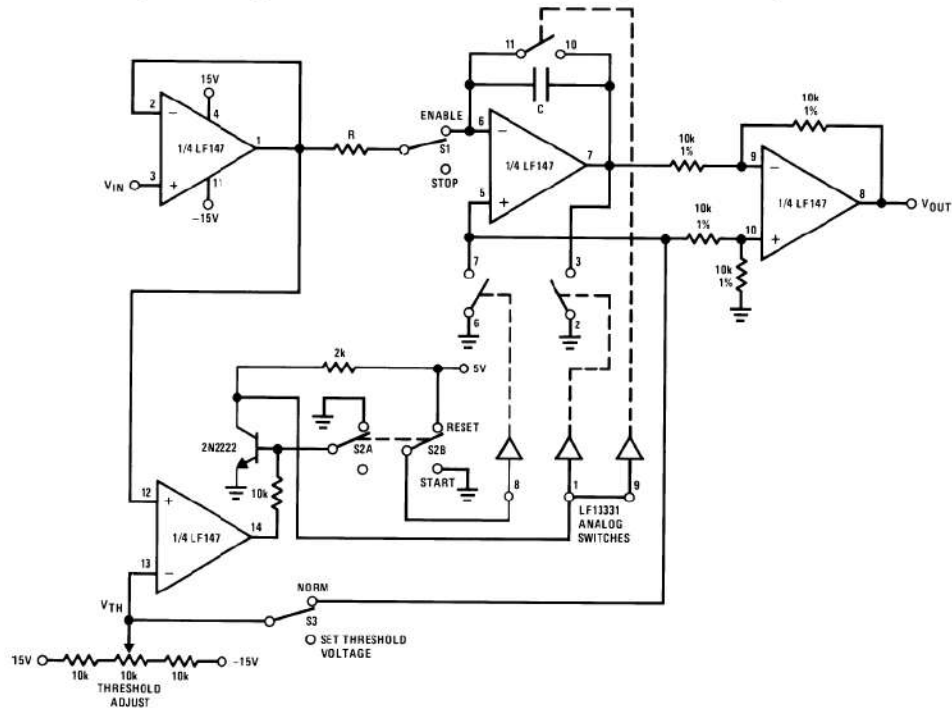
All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	-1 dB
0	1	0	-2 dB
0	1	1	-3 dB
1	0	0	-4 dB
1	0	1	-5 dB
1	1	0	-6 dB
1	1	1	-7 dB

Typical Applications (Continued)

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



0056-4711

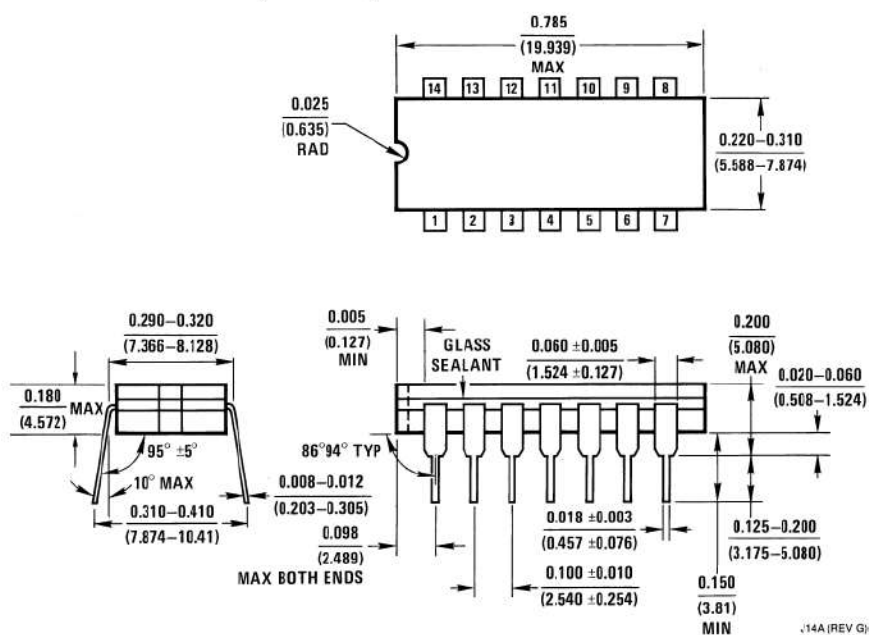
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC} \int_0^t (V_{IN} - V_{TH}) dt$$

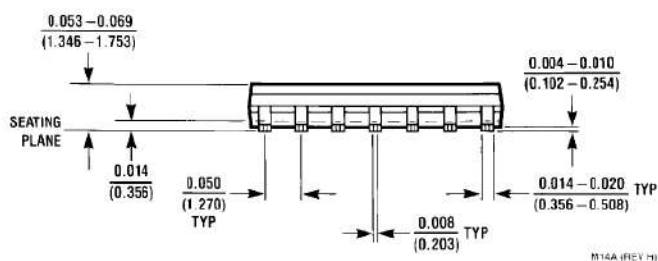
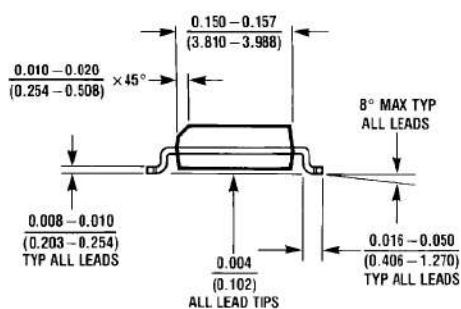
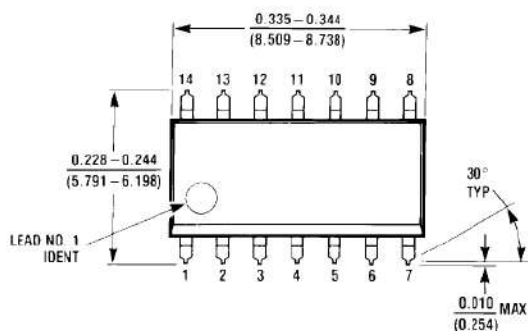
- Output starts when $V_{IN} \geq V_{TH}$
- Switch S_1 permits stopping and holding any output value
- Switch S_2 resets system to zero



- See LM148 data sheet for design equations

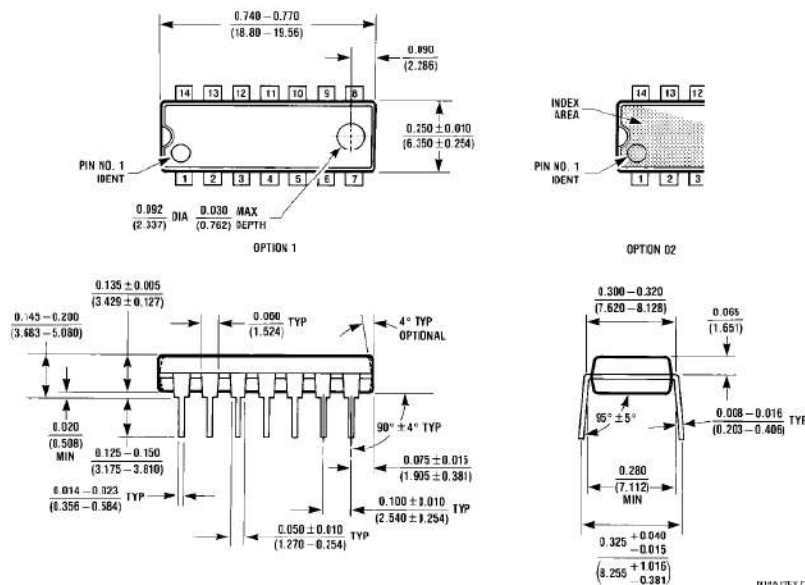
Physical Dimensions inches (millimeters) unless otherwise noted

Ceramic Dual-In-Line Package (J)
Order Number LF147J, LM147J-SMD or LF147J/883
NS Package Number J14A



S.O. Package (M)
Order Number LF347M or LF347MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LF347BN or LF347N
NS Package Number N14A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



National Semiconductor
Americas Customer
Support Center
 Email: new.feedback@nsc.com
 Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
 Fax: +49 (0) 180-530 85 86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +44 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
 Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
 Fax: 81-3-5639-7507
 Email: jpn.feedback@nsc.com
 Tel: 81-3-5639-7560

www.national.com